# Low Cost Fast Dynamic Response Non-isolated PWM Power Switch

## FEATURES

- **Fixed 3.3V Output**
- **Fast Dynamic Response, Meet WIFI Power Supply**
- **Less than 20mW Standby Power**
- **Integrated with Freewheel Diode**
- **Integrated with 500V Power MOSFET and HV Startup Circuit**
- **Up to 45kHz Maximum Frequency**
- **Multi-Mode Control with Audio Noise Free Operation**
- **Supports Buck and Buck-Boost Topology**
- **Good Line and Load Regulation**
- **Built-in Soft Start**
- **Build in Protections:**
  - **Over Load Protection (OLP)**
  - **Cycle-by-Cycle Current Limiting (OCP)**
  - **Abnormal Over Current Protection (AOCP)**
  - **Output OVP**
  - **On-chip OTP**
- **Available with SOP-4 Package**

## APPLICATIONS

- **Smart Lighting / WIFI Power Supply**

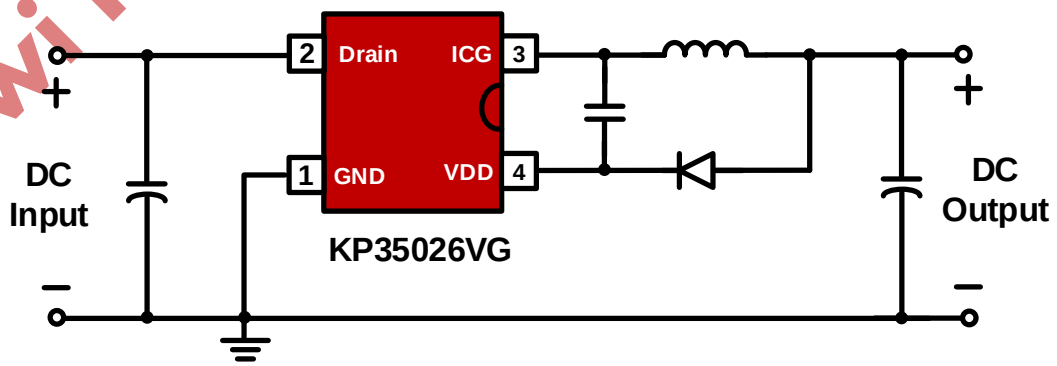
## GENERAL DESCRIPTION

KP35026VG is a high performance Switch Mode Power Supply Switcher for 3.3V low power off-line application with minimum components in typical buck solution. This IC has built-in high break down voltage MOSFET to withstand high surge input.

Unlike conventional PWM control, there's no fixed internal clock in KP35026VG to trigger the GATE driver, the switching frequency is changed according to the load condition. The multi-mode PWM control and fast dynamic response circuit are integrated to achieve high dynamic response and good line/load regulation without audio noise generated. The peak current limit changes according to the real load condition for low standby power in no load.

KP35026VG integrates functions and protections of Under Voltage Lockout (UVLO), Output Over Voltage Protection, Cycle-by-cycle Current Limiting (OCP), On-chip Thermal Shutdown, Over Load Protection (OLP) with Auto Recovery Mode Protection, etc.

## TYPICAL APPLICATION CIRCUIT



## Pin Configuration


**SOP-4**

## Marking Information

Y: Year Code
WW: Week Code, 01-52
Z: Serial Number, 1-9 or A-Z


**SOP-4**

## Typical Output Power Table

| Package | Maximum Load Current @ 85-265 Vac,3.3V |
|---|---|
| SOP-4 | 300mA |

**Note:**

1. Default 3.3V Buck output
2. The practical output power is determined by the output voltage and thermal condition

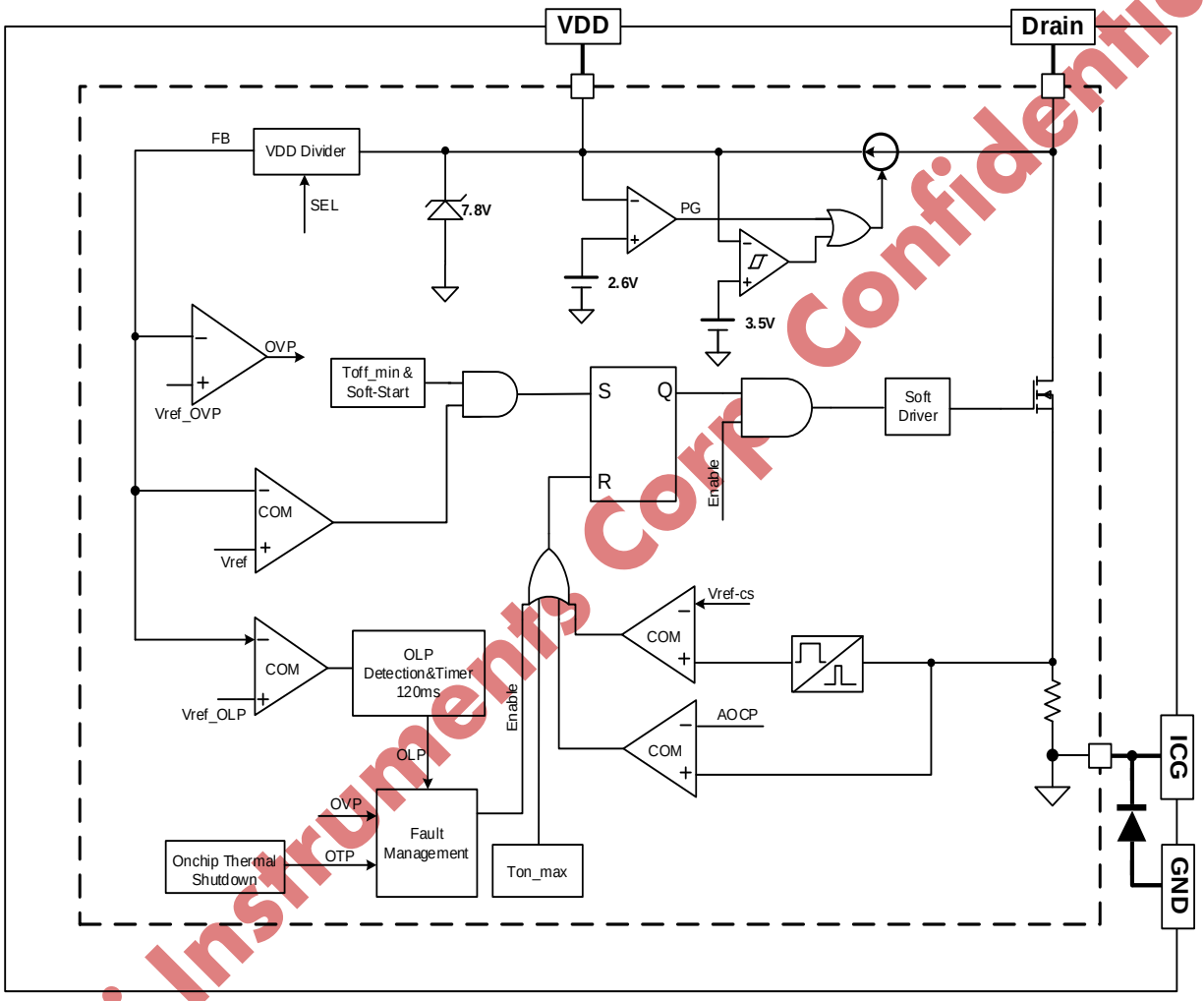
## Pin Description

| Pin Number | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | GND | P | The Ground Reference for the IC |
| 2 | Drain | P | The Power MOSFET Drain |
| 3 | ICG | P | Chip Ground |
| 4 | VDD | P | The Power Supply and the Output Voltage Feedback Pin. For the Normal Operation, a Capacitor with 1μF is Recommended to Connect to this Pin |

## Ordering Information

| Part Number | Description |
|---|---|
| KP35026VGA | SOP-4, Halogen free in T&R, 5000 Pcs / Reel |

## Block Diagram



## Absolute Maximum Ratings (Note 1)

| Parameter | Value | Unit |
|---|---|---|
| Drain - ICG Voltage Range | -0.3 to 500 | V |
| VDD - ICG Voltage Range | -0.3 to 9 | V |
| VDD Pin Clamp Current | 10 | mA |
| $P_{Dmax}$, Power dissipation @$T_A$=50°C (SOP-4) (Note 2) | 0.6 | W |
| Package Thermal Resistance – Junction to Ambient (SOP-4) | 165 | °C/W |
| Maximum Junction Temperature | 160 | °C |
| Storage Temperature Range | -65 to 150 | °C |
| Lead Temperature (Soldering, 10sec.) | 260 | °C |
| ESD Capability, HBM (Human Body Model) | 6000 | V |
| Maximum Internal MOSFET DC Drain Current | 0.6 | A |
| Maximum Internal MOSFET Pulse Drain Current (Continues 100μs) | 2.4 | A |

## Recommended Operation Conditions

| Parameter | Value | Unit |
|---|---|---|
| Operating Junction Temperature | -40 to 125 | °C |
| Operation Switching Frequency | 35 to 45 | kHz |

## Electrical Characteristics (Ta = 25℃, If Not Otherwise Noted)

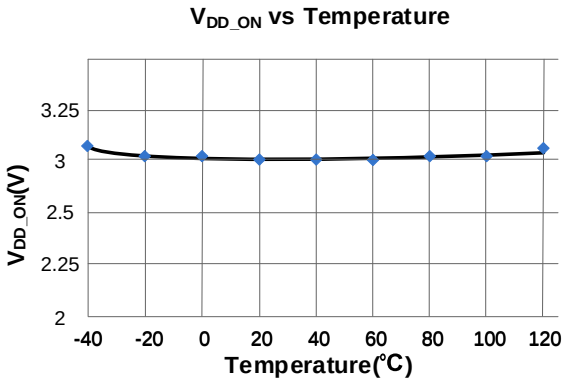
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **High Voltage Startup Section (Drain Pin)** | | | | | | |
| $I_{HV1}$ | HV Current Source1 | Drain=500V, VDD=0V | | 0.6 | | mA |
| $I_{HV2}$ | HV Current Source2 | Drain=500V, VDD=3V | | 6 | | mA |
| $I_{HV\_leakage}$ | HV Leakage Current | Drain=500V, VDD=5V | | 10 | 20 | μA |
| $V_{BR}$ | Power MOSFET Drain Source Breakdown Voltage | | 500 | | | V |
| $R_{dson}$ | Static Drain-Source On Resistance | Vout=3.3V，Ids=50mA | | 17 | | Ω |
| **Supply Voltage Section (VDD Pin)** | | | | | | |
| $V_{DD\_ON}$ | VDD Switch On Threshold | | 3.3 | 3.5 | 3.7 | V |
| $V_{DD\_OFF}$ | VDD Switch Off Threshold | | | 2.6 | | V |
| $V_{DD\_REG}$ | JFET Regulation Voltage | | 3.3 | 3.5 | 3.7 | V |

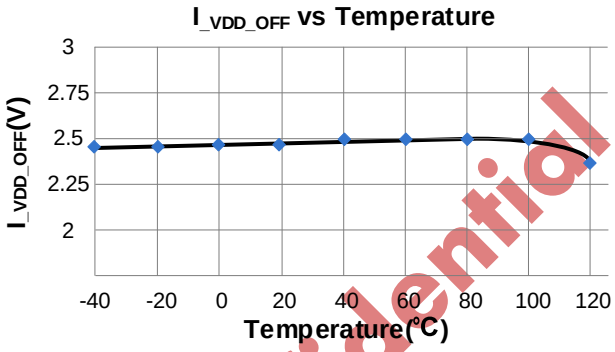
| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{DD\_REF}$ | VDD Feedback Reference Voltage | | 4.15 | 4.24 | 4.33 | V |
| $V_{DD\_Op}$ | VDD Operation Voltage | | | 3.7 | | V |
| $V_{DD\_OVP}$ | VDD OVP Threshol | | | 4.5 | | V |
| $N_{OVP}$ | Over Voltage Debounce Cycle | | | 7 | | |
| $V_{DD\_OLP}$ | VDD OLP Threshold | | | 3.1 | | V |
| $T_{D\_OLP}$ | Over Loading Debounce Time | | | 100 | | ms |
| $V_{DD\_clamp}$ | VDD Clamp Threshold | | 6.5 | 7.1 | 7.7 | V |
| $I_{VDD\_Op}$ | Operation Current | | | 240 | 300 | μA |
| $I_{VDD\_Q}$ | Quiescent Current | No Switching | | 100 | 130 | μA |
| **Current Sense Section** | | | | | | |
| $T_{LEB}$ | Leading Edge Blanking Time | | 200 | 230 | 350 | ns |
| $T_{D\_OCP}$ | Over Current Detection and Control Delay | | | 50 | | ns |
| $I_{OCP}$ | Normal Over Current Protection (OCP) | | 440 | 460 | 480 | mA |
| $I_{AOCP}$ /$I_{OCP}$ | Ratio between Abnormal OCP and normal OCP | | 1.2 | 1.25 | 1.3 | |
| $I_{CS-MIN}$ | Minimum Current Limit | | | 120 | | mA |
| **Timer Section** | | | | | | |
| $T_{off\_min\_norm}$ | Normal Minimum Off time | After Output Entering into Regulation | 20 | 22.5 | 25 | μs |
| $T_{OFF\_nom\_max}$ | Nominal Maximum OFF Time | | | 10 | | ms |
| $T_{ON\_max}$ | Maximum ON Time | | | 17 | | μs |
| $T_{ss}$ | Internal Soft Start Time | | | 3 | | ms |
| $T_{Auto\_Recovery}$ | Protection Auto Recovery Debounce Time | | | 1.2 | | s |
| **On-Chip Thermal Shutdown** | | | | | | |
| $T_{SD}$ | Thermal Shutdown Trigger Point | (Note 2) | | 155 | | °C |

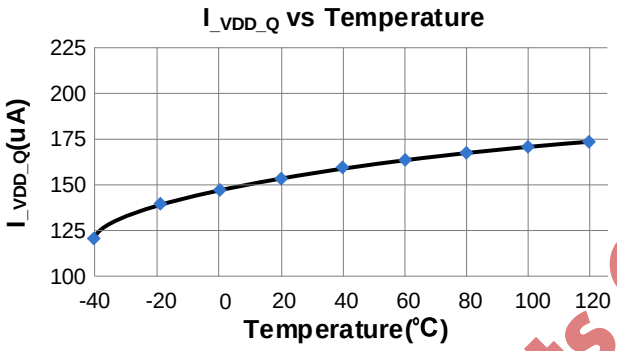
**Note 1.** Stresses listed as the above “Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

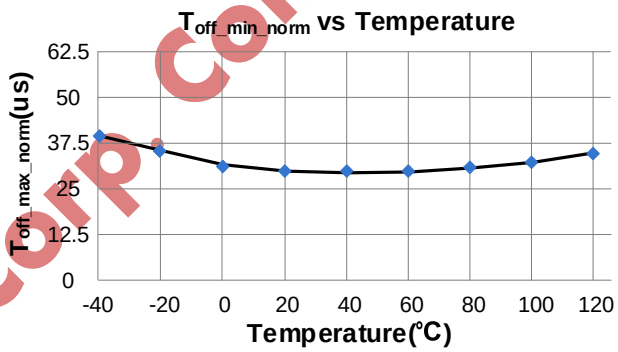
**Note 2.** Guaranteed by design.

## Characterization Plots



## Operation Description

KP35026VG integrates a multi-mode PWM controller with high voltage power MOSFET switch on the IC. It is optimized for off-line non-isolated buck or buck-boost applications in small home appliances, especially WIFI module power supply. KP35026VG utilizes the multi-mode PWM control and fast dynamic response circuit to regulate output with high precision and achieve better dynamic response.

- **Very Low Operation Current**

The standby operating current in KP35026VG is as small as 100μA (typical). The small operating current results in higher efficiency and reduces the VCC hold-up capacitance requirement.

- **High Voltage Start-Up Operation**

In KP35026VG, a 500V high voltage startup cell is integrated. During startup, the HV current source charges the VDD hold up capacitor Cvdd through Drain pin. When VDD reaches turn-on voltage (3.5V typical), the IC begins switching and the IC current consumed increased to 240μA (typical). After the output voltage is established, VDD is powered by output voltage through feedback diode while demagnetization.

- **Constant Voltage Control**

During the power MOSFET off period, KP35026VG samples the VDD pin signal which indicates the output voltage, then using the internal Sample & Hold circuit and constant voltage control circuit to guarantee VDD pin voltage meet the internal reference $V_{REF}$. So that constant output voltage is achieved.

Below equation determines the output voltage:

$$\mathrm{Vo} = \mathrm{VDD} - (V_{freewheel} - V_{feedback})$$

$V_{freewheel}$---Freewheel Diode Voltage

$V_{feedback}$---Feedback Diode Voltage

- **Current Limit and Leading Edge Blanking**

There's a programmable current limit for current sensing voltage, which is changed according to the system switching frequency. When the sampled voltage exceeds the internal threshold, the power MOSFET is turned off for the remainder of that cycle. An internal leading edge blanking circuit is built in.

- **Multi-Mode PWM Control**

To meet the tight requirement of averaged system efficiency and no load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in KP35026VG.

- **Soft Start**

KP35026VG features an internal 3ms (typical) soft start that slowly increases the switching frequency (Toff reduce from 100μs to 22μs linearly) during startup sequence. Every restart attempt is followed by the soft start activation.

- **Output Over Voltage Protection (OVP)**

In KP35026VG, if the sampled FB voltage is larger than 4.5V and lasts for 7 continuous PWM cycles, the IC will enter into Output Over Voltage Protection (Output OVP) mode, in which auto recovery mode will be followed.

- **Over Load Protection (OLP) / Short Load Protection (SLP)**

If over load or short load condition occurs, the

output and the feedback voltage drop down to be lower than $V_{DD\_OLP}$. If this fault is present for more than 100ms (typical), the protection will be triggered, the IC will experience an auto-restart mode (as mentioned below).

- **Abnormal Over Current Protection (AOCP)**

When in heavy load or output short condition, the inductor current may be increased too large. To avoid system components damaged, there's a abnormal over current limit (typically 1.25*OCP). When the current sense voltage is larger than this threshold, the internal power MOSFET is turned off immediately and is to be turned on again after 75μs.

- **On Chip Thermal Shutdown**

KP35026VG integrates thermal shutdown function. When the IC junction temperature is higher than 155 °C, IC shuts down and enters into auto-restart mode (as mentioned below).

- **Enhanced Dynamic Response**

In KP35026VG, the dynamic response performance is optimized to reduce output drop in load transient.

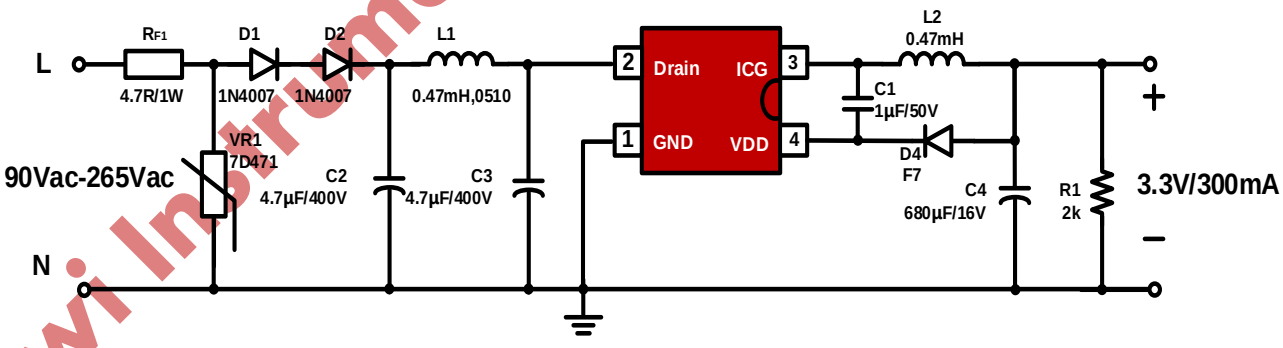
- **Audio Noise Free Operation**

In KP35026VG, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

- **Protections with Auto-Restart**

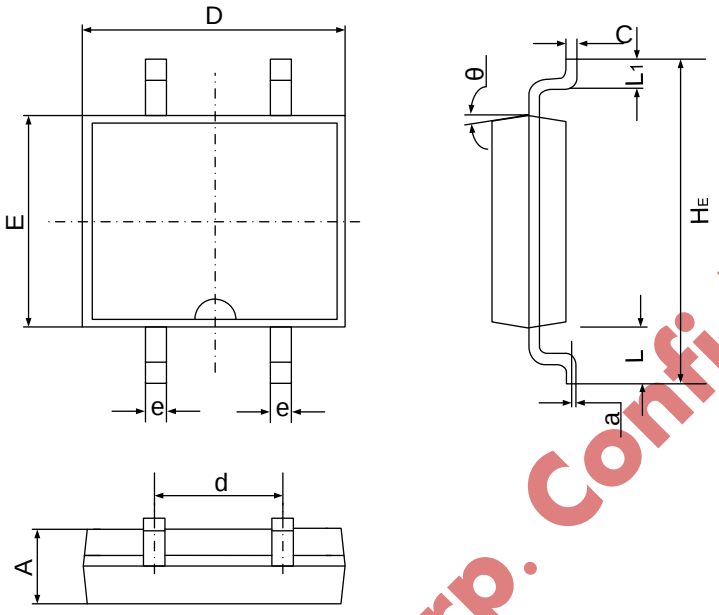
In the event of protections, the IC enters into auto-restart and an internal timer begins counting, wherein the power MOSFET is disabled. When 1.3s had been counted, the IC will reset and start up the system again. However, if the fault still exists, the system will experience the above mentioned process.

## Typical Application Diagram



## Package Dimension

**SOP-4**






| Symbol | Dimensions in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 1.200 | 1.600 | 0.047 | 0.063 |
| a | - | 0.200 | - | 0.008 |
| C | 0.150 | 0.220 | 0.006 | 0.009 |
| D | 4.500 | 5.000 | 0.177 | 0.197 |
| d | 2.300 | 2.700 | 0.091 | 0.106 |
| E | 3.600 | 4.100 | 0.142 | 0.161 |
| e | 0.500 | 0.800 | 0.020 | 0.031 |
| $H_E$ | 6.400 | 7.000 | 0.252 | 0.276 |
| L | 1.300 | 1.700 | 0.051 | 0.067 |
| $L_1$ | 0.500 | 1.100 | 0.020 | 0.043 |
| θ | 7° | | 7° | |

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