Fixed 12V Output, High Performance Low Cost PWM Power Switch

FEATURES

- **Fixed 12V Output**
- **Integrated with 650V Power MOSFET and HV Startup Circuit**
- **Multi-Mode Control**
- **Supports Buck and Buck-Boost Topologies**
- **Good Line and Load Regulation**
- **Built-in Soft Start**
- **Built-in Protections:**
  - **Over Load Protection (OLP)**
  - **Cycle-by-Cycle Current Limiting (OCP)**
  - **Output OVP**
  - **VDD OVP, UVLO & Clamp**
- **Available in SOP-8, DIP-8 Package**

APPLICATIONS

- **Small Home Appliance**
- **Industry Controls**

GENERAL DESCRIPTION

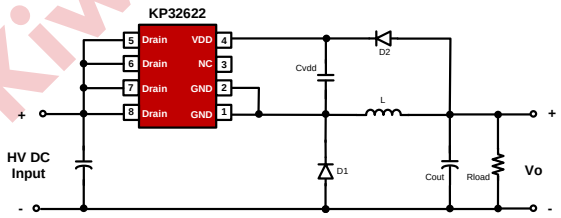
KP32622 is a high performance Switch Mode Power Supply Switcher for low power off-line application with minimum components in typical buck solution. This family has built-in high break down voltage MOSFET to withstand high surge input.

Unlike conventional PWM control, there's no fixed internal clock in KP32622 family to trigger the GATE driver, the switching frequency is changed according to the load condition. The multi-mode PWM control is integrated to simplify circuit design and achieve good line and load regulation. The peak current limit changes according to the real load condition for low standby power in no load.

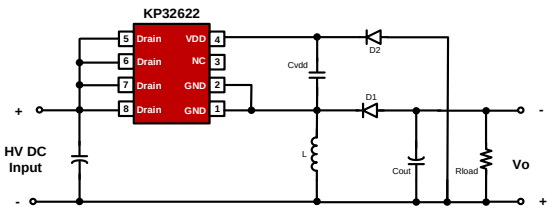
KP32622 integrates functions and protections of Under Voltage Lockout (UVLO), Cycle-by-cycle Current Limiting (OCP), Output OVP, On-chip Thermal Shutdown, Over Load Protection (OLP), VDD OVP with Auto Recovery Mode Protection, etc.

TYPICAL APPLICATION CIRCUIT

BUCK



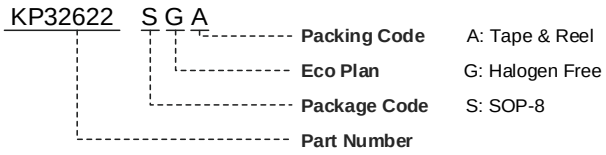
BUCKBOOST



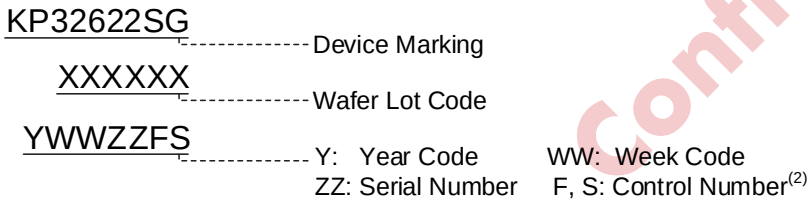
Ordering Information

Order Number(1)	Package	Eco Plan	MSL Rating	Packing	Device Marking
KP32622SGA	SOP-8	Halogen Free	3	T&R, 4000 Pcs/Reel	KP32622SG
KP32622DP	DIP-8	Pb Free	3	Tube, 50 Pcs/Tube	KP32622DP

(1)

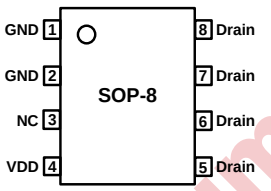


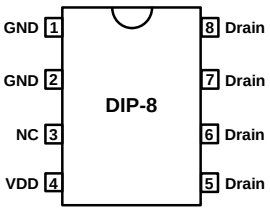
Marking Information

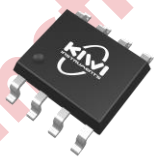


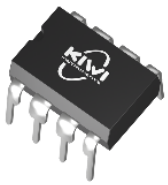
(2) Wafer Lot Code, Year Code, Week Code, Serial Number, and Control Number are numbers or letters

Pin Configuration









Pin Number	Pin Name	I/O(3)	Description
1,2	GND	G	The Ground Reference for the IC
3	NC	-	No Connection
4	VDD	P	The Power Supply and the Output Voltage Feedback Pin. For the Normal Operation, a Capacitor with 1μF is Recommended to Connect to this Pin
5,6,7,8	Drain	P	The Power MOSFET Drain

(3) P - Power; G – GND

Typical Output Power Table(4)

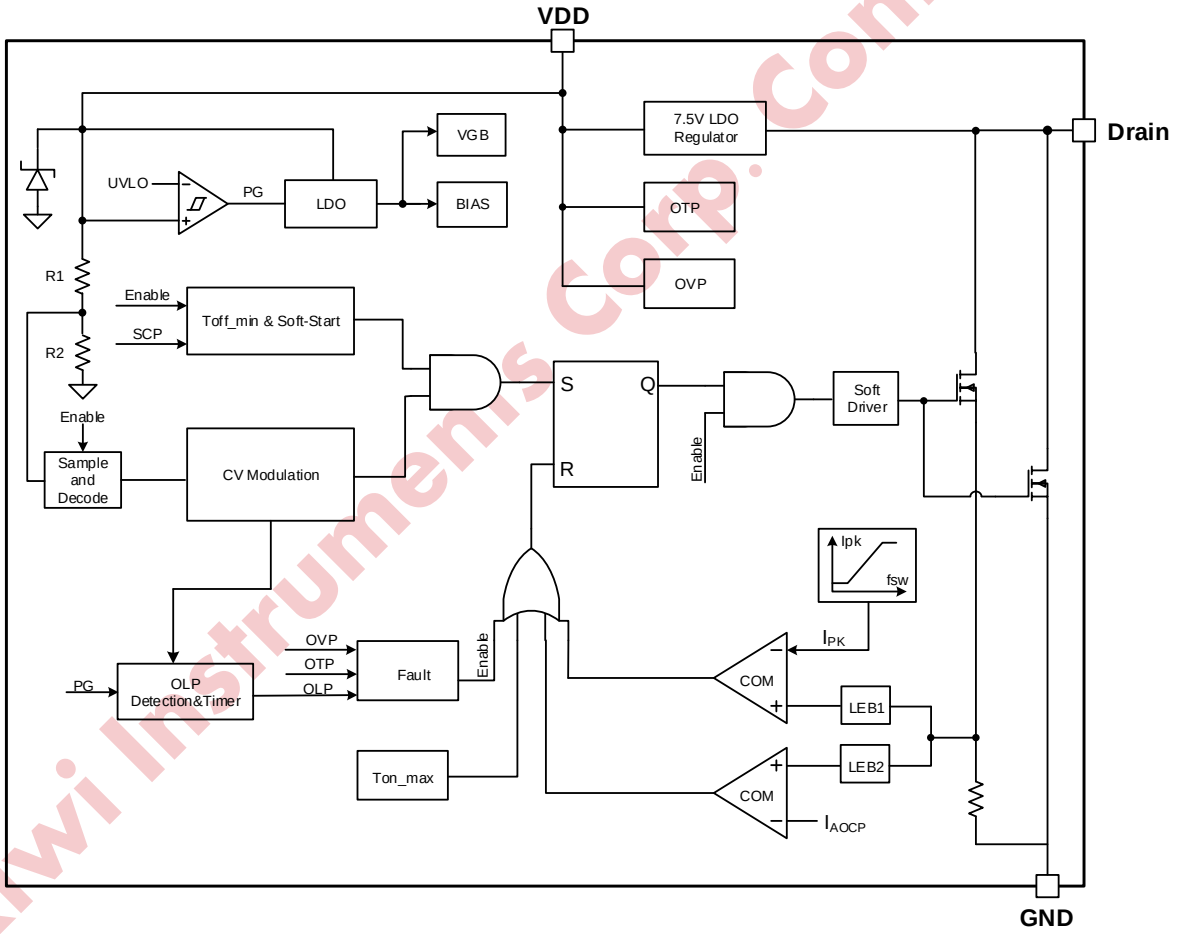
Part Number	R_{dson}	Input Voltage	Package	Steady Load (12V) (5)	Peak Load (12V) (6)
KP32622	4Ω	85-265Vac	SOP-8	450mA	700mA
			DIP-8	500mA	700mA

(4) Maximum output power is constrained by IC maximum junction temperature and determined by ambient temperature and PCB. The system actual maximum output power is determined by the test.

(5) Steady load means maximum load which hold above 2hours at 75°C half-sealed environment.

(6) Peak load means maximum load which hold above 1min at 75°C half-sealed environment.

Block Diagram



Absolute Maximum Ratings(7)

Parameter	Value	Unit
Drain Pin Voltage Range	-0.3 to 650	V
VDD Supply Voltage	-0.3 to 30	V
θ_{JA}, Thermal Resistance---Junction to Ambient (SOP-8)	165	˚C/W
θ_{JA}, Thermal Resistance---Junction to Ambient (DIP-8)	105	˚C/W
Maximum Junction Temperature	150	˚C
Storage Temperature Range	-65 to 150	˚C
Lead Temperature (Soldering, 10sec.)	260	˚C
Maximum Internal MOSFET DC Drain Current	2	A
Maximum Internal MOSFET Pulse Drain Current (Duration below 100μs)	8	A

(7) Exceeding the limits listed in the list may cause permanent damage to the IC. The limit parameters are only used to identify the stress registration, and the IC may not work properly outside the recommended operating conditions. Excessive exposure to outside recommended operating conditions may affect IC reliability.

ESD Rating

Paramter		Value	Unit
V_{ESD}	Human Body Model - HBM (8)	4500	V

(8) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing requirements with a standard ESD control process.

Recommended Operation Conditions

Parameter	Value	Unit
Operating Junction Temperature	-40 to 125	˚C
Operation Switching Frequency	40 to 60	kHz

Electrical Characteristics (TA = 25˚C, if not otherwise noted)

符号	参数	测试条件	最小	典型	最大	单位
高压启动部分 (HV 管脚)						
I_{HV}	HV Charging Current	Drain=650V, VDD=0V		2		mA
$I_{HV\_leakage}$	HV Leakage Current	Drain=650V, VDD=12V			25	μA

V_{BR}	Power MOSFET Drain Source Breakdown Voltage		650			V
R_{dson}	Static Drain-Source On Resistance			4		Ω
供电部分 (VDD 管脚)						
V_{DD_ON}	VDD Under Voltage Lockout Exit			8.7		V
V_{DD_OFF}	VDD Under Voltage Lockout Enter			7.2		V
V_{DD_Reg1}	VDD Regulation Voltage			12.6		V
I_{VDD_st}	Start-up Current	No switching		200		μA
I_{VDD_Q}	Quiescent Current			200		μA
V_{DD_OVP}	VDD OVP Threshold			16		V
T_{D_OVP}	VDD OVP Debounce Cycle			7		cycle
V_{DD_Clamp}	VDD Clamp Votage	IVDD=10mA		30		V
V_{DD_OLP}	VDD OLP Voltage			8.5		V
T_{D_OLP}	VDD OLP Debounce Time			120		ms
计时部分						
$T_{OFF\_min\_norm}$	Normal Minimum OFF time			16		μs
$T_{OFF\_max\_nom}$	Nominal Maximum OFF Time			2.3		ms
$T_{OFF\_max\_FDR}$	Maximum OFF Time in Fast Dynamic Response Mode			420		μs
T_{ON_max}	Maximum ON Time			12		μs
T_{ss}	Internal Soft Start Time			30		ms
$T_{Auto\_Recovery}$	Protection Auto Recovery Debounce Time			1.5		s
过热保护						
T_{SD}	Thermal Shutdown Trigger Point (9)			150		℃
内部电流检测输入部分						
T_{LEB}	Leading Edge Blank			350		ns
T_{D_OCP}	OCP Delay			100		ns
I_{PK}	Internal Peak Current			1.0		A
I_{AOCP}	Abnormal Peak Current			1.3		A

(9) Parameters depend on design and pass functional testing during mass production.

Operation Description

KP32622 integrates a high voltage power MOSFET switch and a multi-mode PWM controller. It is optimized for 12V fixed off-line non-isolated buck or buck-boost applications in small home appliances and linear regulator replacement. The IC utilizes the multi-mode PWM control to regulate output with high precision and lowest components count.

● Very Low Operation Current

The standby operating current in KP32622 is as small as 200μA (typical). The small operating current results in higher efficiency and reduces the VCC hold-up capacitance requirement.

● High Voltage Start-Up Operation

In KP32622, a 650V high voltage startup cell is integrated. During startup, the internal startup circuit is enabled and a HV current source charges the VDD hold up capacitor Cvdd through Drain pin, as shown in “Block Diagram”. When VDD reaches UVLO turn-on voltage (8.7V typical), the IC begins switching. The VDD is charged by the output through the feedback diode in steady state, which result in less than 100mW standby power with the combination of high voltage startup cell.

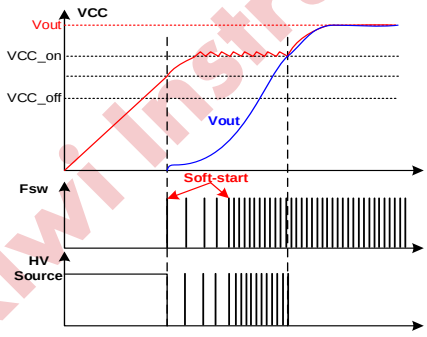


Fig.1

● Current Limit and Leading Edge Blanking

There’s a programmable current limit for current sensing voltage from internal CS sense circuit, which is changed according to the system switching frequency. When the sampled voltage exceeds the internal threshold, the power MOSFET is turned off for the remainder of that cycle. An internal leading edge blanking circuit is built in. During this blanking period (350ns, typical), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the GATE driver.

● Soft Start

KP32622 features an internal 30ms (typical) soft start that slowly increases the switching frequency during startup sequence (Toff decrease from 100μs to 16μs). Every restart attempt is followed by the soft start activation.

● Multi-Mode PWM Control

To meet the tight requirement of averaged system efficiency and no load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in KP32622 which is shown in the Fig 2.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 100mW.

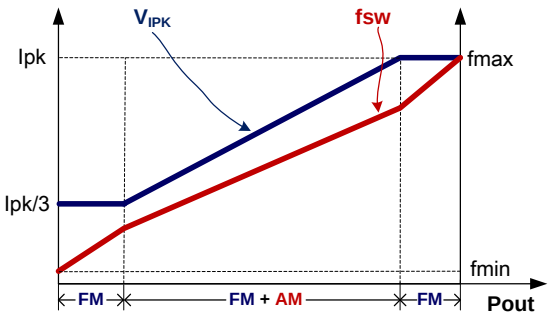


Fig.2

- **Over Load Protection (OLP) / Short Load Protection (SLP)**

If over load or short load condition occurs, the output voltage drops down to be lower than V_{DD_OLP}. If this fault is present for more than 120ms (typical), the protection will be triggered, the IC will experience an auto-restart mode (as mentioned below).

- **Abnormal Over Current Protection (AOCP)**

When in heavy load or output short condition, the inductor current may be increased too large. To avoid system components damaged, there's a abnormal over current limit circuit. When the internal CS voltage is larger than this threshold, the internal power MOSFET is turned off immediately and is to be turned on again after 120μs.

- **On Chip Thermal Shutdown**

KP32622 integrates thermal shutdown function. When the IC junction temperature is higher than 150 ˚C, IC shuts down and enters into auto-restart mode (as mentioned below).

- **Enhanced Dynamic Response**

In KP32622, the dynamic response performance is optimized to reduce output drop in load transient.

- **VDD Over Voltage Protection (OVP) and Zener Clamp**

When VDD voltage higher than V_{DD_OVP} (typically 16V), the IC will stop switching. This will cause VDD fall down to be lower than V_{DD_OFF} (typically 7.2V) and then the system will restart up again. An internal 30V (typical) zener clamp is integrated to prevent the IC from damage.

- **Protections with Auto-Restart**

In the event of protections, the IC enters into auto-restart and an internal timer begins counting, wherein the power MOSFET is disabled. When 1.5s had been counted, the IC will reset and start up the system again. However, if the fault still exists, the system will experience the above mentioned process.

- **Soft Totem-Pole Gate Driver**

KP32622 has a soft totem-pole gate driver with optimized EMI performance.

Typical Reference Design

Inductor Calculation

In order to balance the thermal affection, recommend KP32622 work in DCM mode. Detail calculation shows below:

$$L=(Vo+Vf)*Io\_olp/\eta/(1/2*Ipk^2*Fsw\_max)$$

Vo：Output Voltage;

Vf：Forward voltage on freewheeling diode; Io_olp：Output Over Current, typical 1.1-1.2 times of normal Output Current;
η：system efficiency, typical 0.8;

Ipk：Peak inductor current;

Fsw_max：Default set 40-50kHz;

Take KP32622DP as example，set output as 12V-400mA：

Set Io_olp=1.2*Io=0.48A; Vf=0.7V; η=0.8; Ipk=1.0A; Fsw_max=50kHz;

L=(12V+0.7V)*0.48A/0.8/(1/2*1.0A/1.0A/50kHz)=0.30mH.

Choose L=0.30mH & Isaturation>1.3A (I_{AOCP}) as the specific inductor parameter demand.

Input and Output Capacitor Selection

Output Capacitor Selection: for normal application, output capacitor is choose between 470μF-680μF according to actual output voltage ripple.

Input Capacitor Selection: for normal application, output capacitor is choose between 10μF-15μF according to load variation.

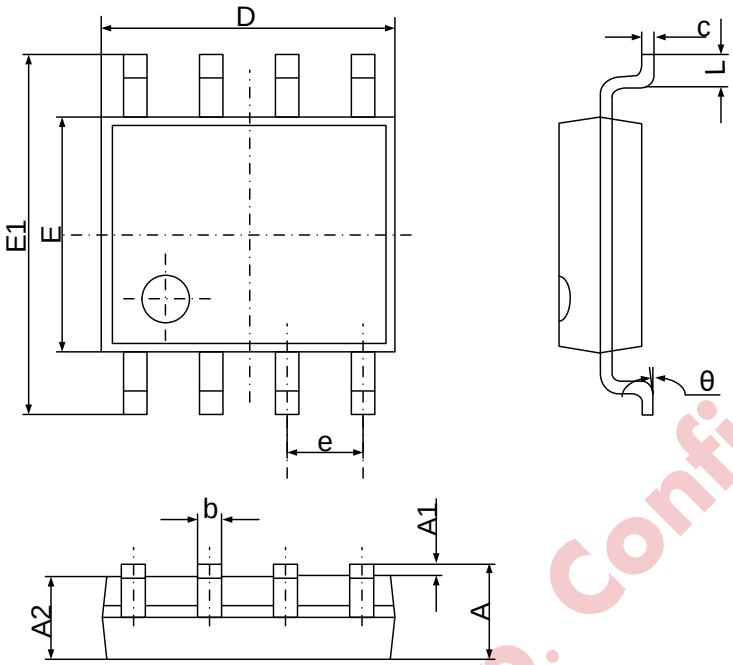
Dummy Load Selection

Dummy Load Selection: heavy dummy load could suppress the output voltage from floating up, but too heavy dummy load would enlarge the standby power loss; take balance among load regulation and standby power loss.

2-6k dummy load is recommended in KP32622 system for good output regulation and low dummy load power loss (~20mW).

Package Dimension

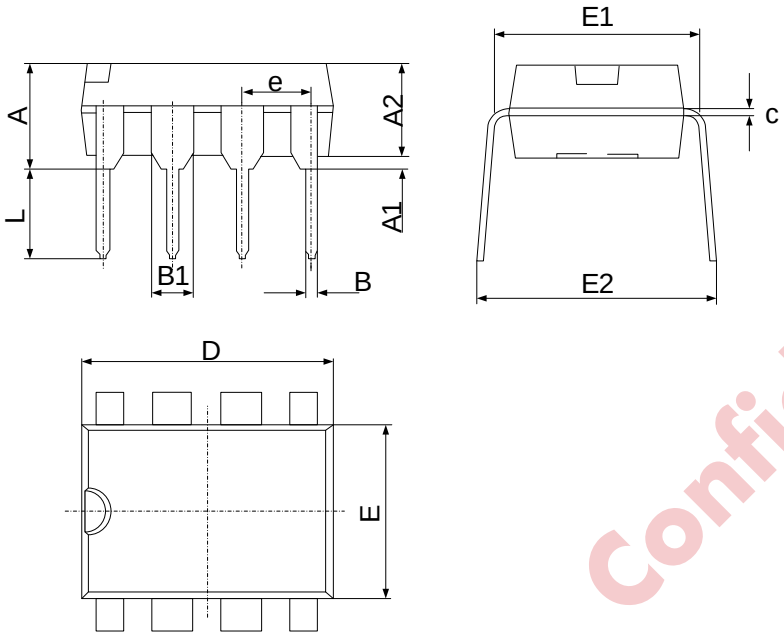
SOP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

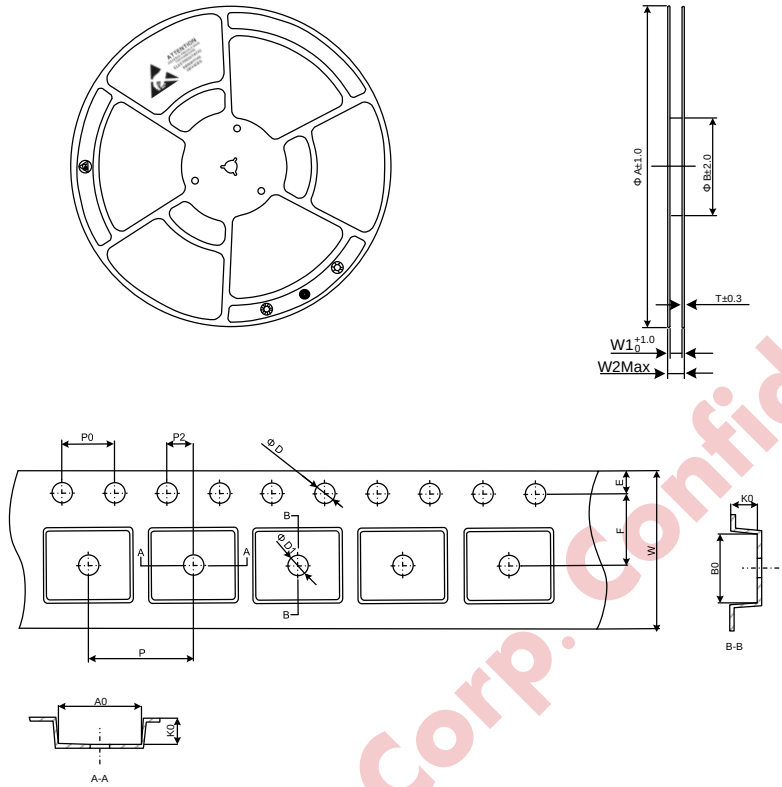
Package Dimension

DIP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	3.600	4.150	0.142	0.163
A1	0.510	-	0.020	-
A2	3.150	3.400	0.124	0.134
B	0.380	0.560	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
c	0.200	0.350	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.500	0.244	0.256
E1	7.620 (REF)		0.300 (REF)	
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	7.620	9.300	0.300	0.366

Tape and Reel Information



Reel Dimensions (mm)				
A	**B (Inner Diameter)**	**W1**	**W2 Max**	**T**
330	100	12.4	18.4	1.5

Tape Dimensions			
Symbol	**Dimensions (mm)**	**Symbol**	**Dimensions (mm)**
E	1.75±0.10	W	12.00±0.10
F	5.50±0.10	P	8.00±0.10
P2	2.00±0.10	A0	6.60±0.10
D	$1.50^{+0.1}_{-0}$	B0	5.30±0.10
D1	1.55±0.05	K0	1.90±0.10
P0	4.00±0.10		

Packing Quantity				
Package	**Pcs/Reel**	**Reels/Box**	**Boxes/Carton**	**Pcs/Carton**
SOP-8	4000	2	8	64000

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