Integrated 500V MOSFET Adjustable Output Voltage Off-line PWM Power Switch

FEATURES

- **Integrated with 500V Power MOSFET and HV Startup Circuit**
- **Optimize Audible Noise, Improve System Stability**
- **Multi-Mode Control with Audio Noise Free Operation**
- **Supports Buck and Buck-Boost Topologies**
- **Default 12V Output with FB Floated**
- **Less than 50mW Standby Power**
- **Green Mode Operation for High Efficiency**
- **Good Line and Load Regulation**
- **Built-in Soft Start**
- **Build in Protections:**
  - **Over Load Protection (OLP)**
  - **Cycle-by-cycle Current Limiting (OCP)**
  - **Output OVP**
  - **VDD OVP, UVLO & Clamp**
- **Available in SOP-8, DIP-8 Package**

APPLICATIONS

- **Small Home Appliance**

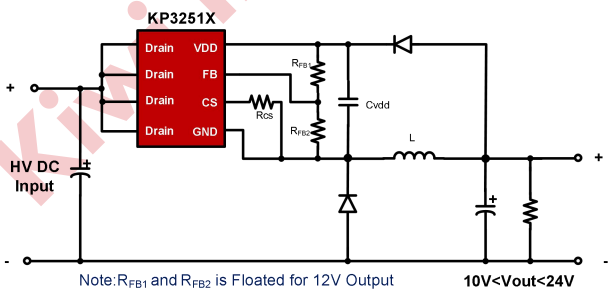
GENERAL DESCRIPTION

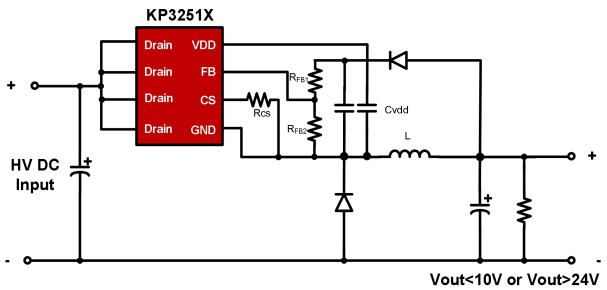
KP3251X family is a high performance Switch Mode Power Supply Switcher for low power off-line application with minimum components in typical buck solution. This family has built-in high break down voltage MOSFET to withstand high surge input.

Unlike conventional PWM control, there's no fixed internal clock in KP3251X family to trigger the GATE driver, the switching frequency is changed according to the load condition. The multi-mode PWM control is integrated to simplify circuit design and achieve good line and load regulation without audio noise generated. The peak current limit changes according to the real load condition for low standby power in no load.

KP3251X integrates functions and protections of Under Voltage Lockout (UVLO), Cycle-by-cycle Current Limiting (OCP), Output OVP, On-chip Thermal Shutdown, Over Load Protection (OLP), VDD OVP with Auto Recovery Mode Protection, etc.

TYPICAL APPLICATION CIRCUIT

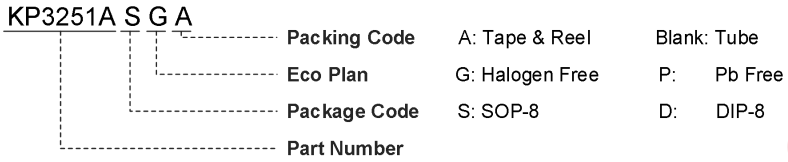




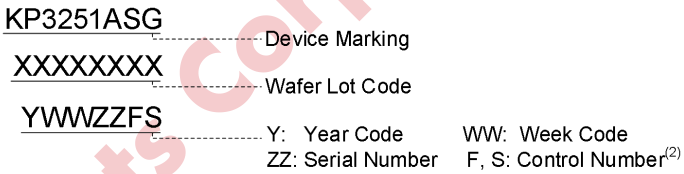
Ordering Information

Order Number[1]	Package	Eco Plan	MSL Rating	Packing	Device Marking
KP3251ASGA	SOP-8	Halogen Free	3	T&R, 4000 Pcs/Reel	KP3251ASG
KP32511SGA	SOP-8	Halogen Free	3	T&R, 4000 Pcs/Reel	KP32511SG
KP32512SGA	SOP-8	Halogen Free	3	T&R, 4000 Pcs/Reel	KP32512SG
KP32512DP	DIP-8	Pb Free	3	Tube, 50 Pcs/Tube	KP32512DP
KP32513SGA	SOP-8	Halogen Free	3	T&R, 4000 Pcs/Reel	KP32513SG
KP32514DP	DIP-8	Pb Free	3	Tube, 50 Pcs/Tube	KP32514DP

(1)

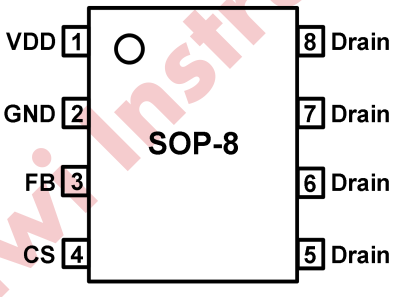


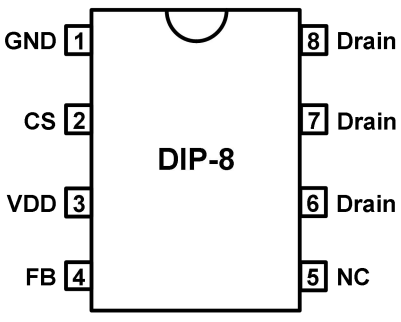
Marking Information

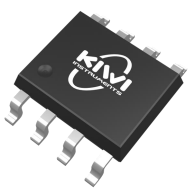


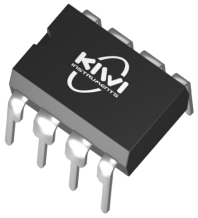
(2) Wafer Lot Code, Year Code, Week Code, Serial Number, and Control Number are numbers or letters

Pin Configuration









Pin Number (SOP-8)	Pin Number (DIP-8)	Pin Name	I/O(3)	Description
1	3	VDD	P	The Power Supply and the Output Voltage Feedback Pin. For the normal operation, a capacitor with 1μF is recommended to connect to this pin
2	1	GND	G	The Ground Reference for the IC
3	4	FB	I	Feedback Input. Left Open for Default 12V Output
4	2	CS	I	Current Sensing Input
5, 6, 7, 8	6, 7, 8	Drain	P	The Power MOSFET Drain
-	5	NC	-	No Function Pin and Left Floating in Application

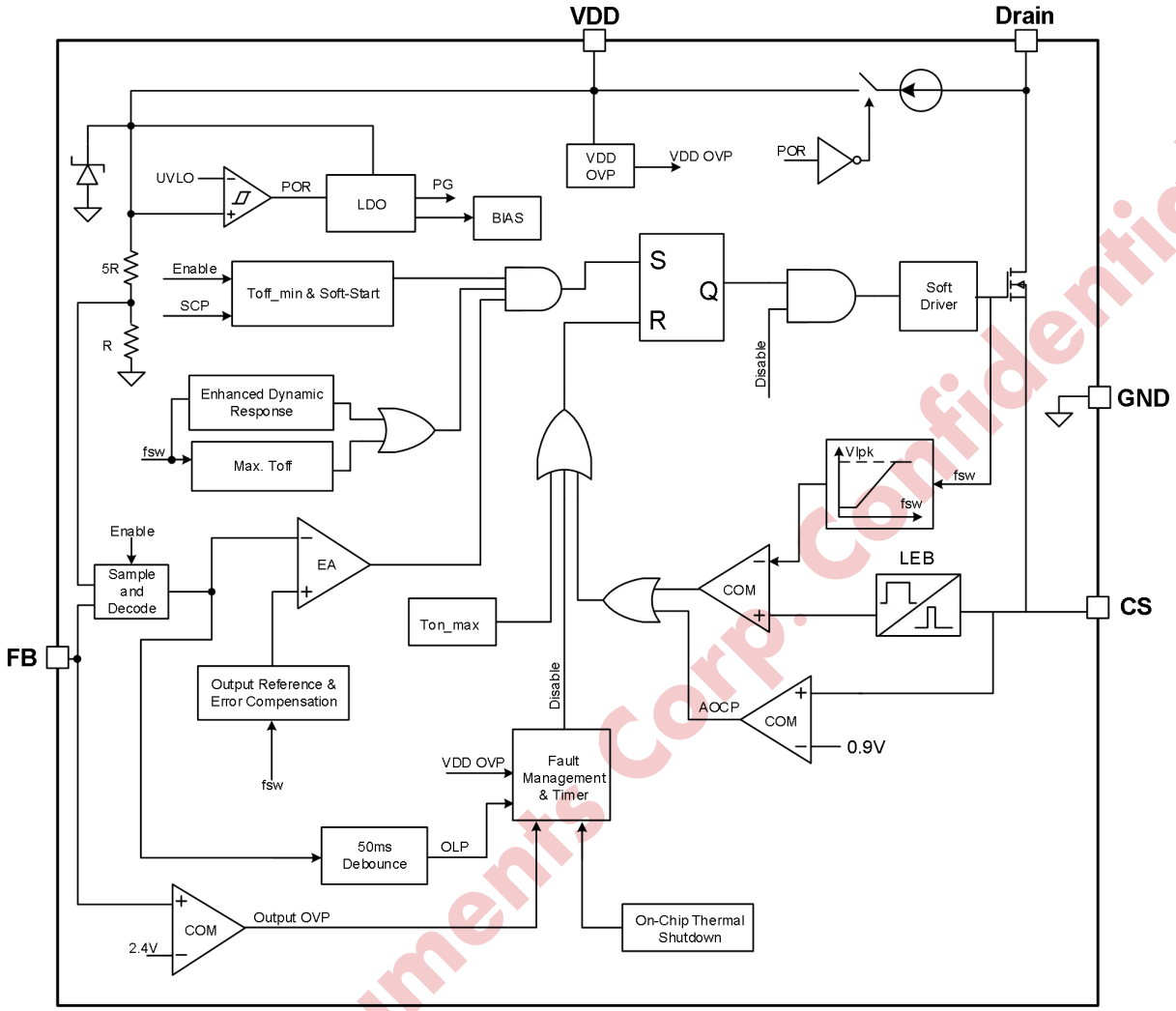
(3) P - Power; I - Input; G - GND

Typical Output Power Table

Part Number	Package	R_{dson}	Vo	Load Current @85-265Vac, BUCK(4)
KP3251A	SOP-8	18Ω	>2V	Io<250mA
KP32511	SOP-8	9Ω	>2V	200mA<Io<400mA
KP32512	SOP-8/DIP-8	5.4Ω	>2V	350mA<Io<700mA
KP32513	SOP-8	2.45Ω	>2V	500mA<Io<800mA
KP32514	DIP-8	1.6Ω	>2V	650mA<Io<900mA

(4) Maximum output power is constrained by IC maximum junction temperature and determined by ambient temperature and PCB. The system actual maximum output power is determined by the test.

Block Diagram



Absolute Maximum Ratings(5)

Parameter		Value	Unit
Drain Pin Voltage Range		-0.3 to 500	V
VDD Supply Voltage		-0.3 to 30	V
FB, CS Voltage Range		-0.3 to 7	V
θ_{JA}, Thermal Resistance---Junction to Ambient (SOP-8)(6)		165	˚C/W
θ_{JA}, Thermal Resistance---Junction to Ambient (DIP-8)(6)		105	˚C/W
Maximum Junction Temperature		150	˚C
Storage Temperature Range		-65 to 150	˚C
Lead Temperature (Soldering, 10sec.)		260	˚C
Maximum Internal MOSFET DC Drain Current	KP3251A	0.5	A
	KP32511	1	A
	KP32512	2	A
	KP32513	3	A
	KP32514	4	A
Maximum Internal MOSFET Pulse Drain Current (Duration below 100μs)	KP3251A	2	A
	KP32511	4	A
	KP32512	8	A
	KP32513	12	A
	KP32514	16	A

(5) Exceeding the limits listed in the list may cause permanent damage to the IC. The limit parameters are only used to identify the stress registration, and the IC may not work properly outside the recommended operating conditions. Excessive exposure to outside recommended operating conditions may affect IC reliability.

(6) Measured on 4-Layer PCB by JEDEC51-2 Integrated Circuits Thermal Test Method Environmental Conditions – Natural Convection.

ESD Rating

Parameter		Value	Unit
V_{ESD}	Human Body Model – HBM (7)	5000	V

(7) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing requirements with a standard ESD control process.

Recommended Operation Conditions

Parameter	Value	Unit
Operating Junction Temperature	-40 to 125	℃
Operation Switching Frequency	40 to 60	kHz

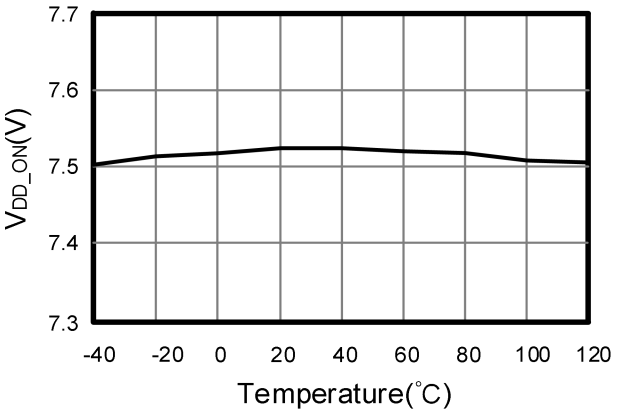
Electrical Characteristics (TA = 25℃, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power MOSFET Section (Drain Pin)						
I_{Drian_st}	Drain Charging Current	Drain=40V, VDD=6V		1.3		mA
$I_{Drain\_leakage}$	Drain Leakage Current	Drain=500V, VDD=12V			100	μA
V_{BR}	Power MOSFET Drain Source Breakdown Voltage		500			V
R_{dson}	Static Drain-Source On Resistance	KP3251A		18	20	Ω
		KP32511		9	11	Ω
		KP32512		5.4	6.5	Ω
		KP32513		2.45	3.0	Ω
		KP32514		1.6	2.2	Ω
Supply Voltage Section (VDD Pin)						
V_{DD_ON}	VDD Under Voltage Lockout Exit		6.4	7.5	8.6	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter			6.7		V
V_{DD_Reg1}	VDD Regulation Voltage	FB is Floating	12.4	12.6	12.8	V
I_{VDD_st}	Start-up Current	No Switching		180		μA
I_{VDD_Q}	Quiescent Current			200		μA
V_{DD_OVP}	VDD OVP Threshold		26.4	28.5	30.6	V
V_{DD_Clamp}	VDD Clamp Votage	IVDD=10mA		30		V
Feedback Section (FB Pin)						
V_{FB_REF}	Internal Error Amplifier (EA) Reference Input		1.97	2.0	2.03	V
V_{FB_OVP}	Output Over Voltage Protection (Output OVP) Threshold			2.4		V
V_{FB_OLP}	Output Over Load Protection (Output OLP) Threshold			1.7		V
T_{D_OLP}	Over Loading Debounce Time			120		ms

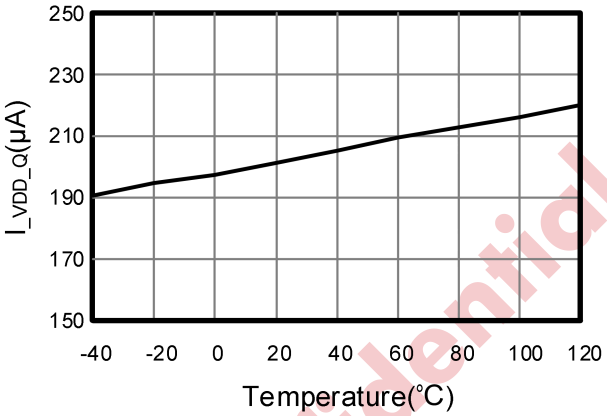
Current Sense Input Section (CS Pin)						
T_{LEB}	Leading Edge Blanking Time			350		ns
T_{D_OCP}	Over Current Detection and Control Delay			100		ns
V_{IPK}	Normal Peak Current Limit		0.49	0.55	0.61	V
V_{AOCP}	Abnormal Over Current Protection Threshold			0.9		V
Timer Section						
$T_{OFF\_min\_norm}$	Normal Minimum OFF Time		14.5	16	17.5	μs
$T_{OFF\_max\_nom}$	Nominal Maximum OFF Time			1.4		ms
$T_{OFF\_max\_FDR}$	Maximum OFF Time in Fast Dynamic Response Mode			420		μs
T_{ON_max}	Maximum ON Time		6	12	31	μs
T_{ss}	Internal Soft Start Time			3		ms
$T_{Auto\_Recovery}$	Protection Auto Recovery Debounce Time			1.2		s
On-Chip Thermal Shutdown						
T_{SD}	Thermal Shutdown Trigger Point(8)			150		℃
T_{HYS}	Thermal Shutdown Hysteresis(8)			20		℃

(8) Parameters depend on design and pass functional testing during mass production.

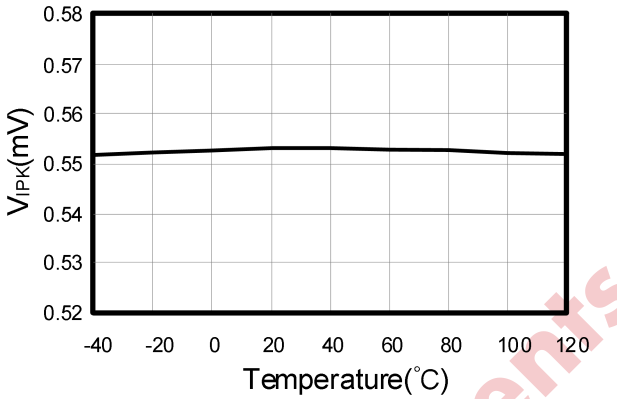
Typical Characteristic



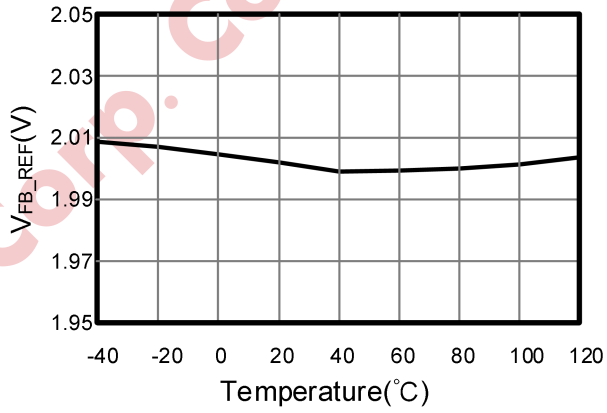
V_{DD_ON} vs Temperature



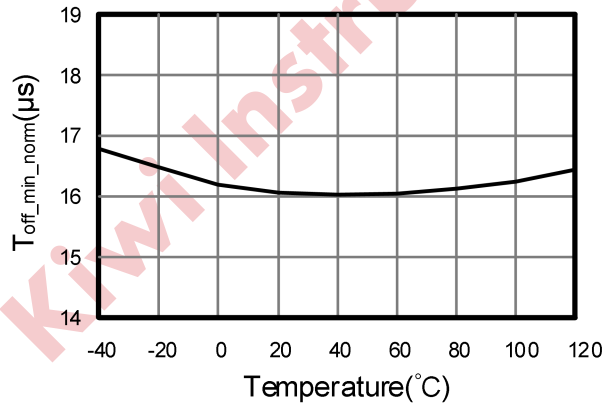
I_{VDD_Q} vs Temperature



V_{IPK} vs Temperature



V_{FB_REF} vs Temperature



$T_{off\_min\_norm}$ vs Temperature

Operation Description

KP3251X family integrates a high voltage power MOSFET switch and a multi-mode PWM controller. It is optimized for off-line non-isolated buck or buck-boost applications in small home appliances and linear regulator replacement. The IC utilizes the multi-mode PWM control to regulate output with high precision and lowest components count.

● Very Low Operation Current

The standby operating current I_{VDD_Q} in KP3251X is as small as 200μA (typical). The small operating current results in higher efficiency and reduces the VCC hold-up capacitance requirement.

● High Voltage Start-Up Operation with Less than 50mW Standby Power

In KP3251X, a 500V high voltage startup cell is integrated. During startup, the internal startup circuit is enabled and a HV current source charges the VDD hold up capacitor Cvdd through Drain pin, as shown in “Block Diagram”. When VDD reaches UVLO turn-on voltage V_{DD_ON} (typically 7.5V), the IC begins switching. The VDD is charged by the output through the feedback diode in steady state, which result in less than 50mW standby power with the combination of high voltage startup cell.

● Current Limit and Leading Edge Blanking

There’s a programmable current limit for current sensing voltage from CS Pin, which is changed according to the system switching frequency. When the sampled voltage exceeds the internal threshold, the power MOSFET is turned off for the remainder of that cycle. An internal leading edge blanking circuit is built in. During this blanking period (typically 300ns), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the GATE driver.

● Multi-Mode PWM Control

To meet the tight requirement of averaged system efficiency and no load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in KP3251X which is shown in the Fig 1.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 50mW.

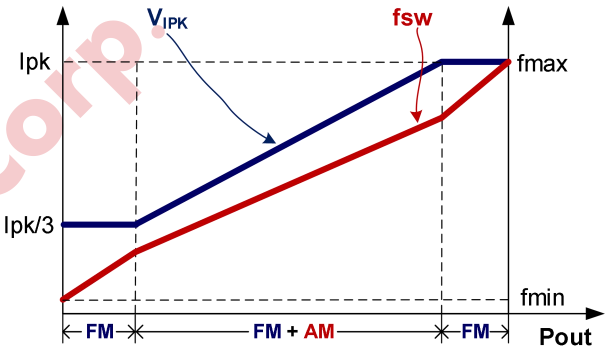


Fig.1

● Constant Voltage Control

During the power MOSFET off period, KP3251X samples the FB pin signal which indicates the output voltage, then using the internal Sample & Hold circuit and constant voltage control circuit to guarantee FB pin voltage meet the internal reference V_{FB_REF} (typically 2.0V). So that constant output voltage is achieved.

Below equation approximately determines the output voltage:

$$Vo = 2.0V * \frac{Rup + Rdown}{Rdown}$$

Since the sampling of FB is affected by the

isolation diode, it is necessary to adjust the FB voltage dividing resistance in practical application.

- **Soft Start**

KP3251X features an internal 4ms (typical) soft start that slowly increases the switching frequency during startup sequence. Every restart attempt is followed by the soft start activation.

- **Output Over Voltage Protection (OVP)**

In KP3251X, if the sampled FB voltage is larger than V_{FB_OVP} (typically 2.4V) and lasts for three continuous PWM cycles, the IC will enter into Output Over Voltage Protection (Output OVP) mode, in which auto recovery mode will be followed.

- **Over Load Protection (OLP) /Short Load Protection (SLP)**

If over load or short load condition occurs, the output and the feedback voltage drop down to be lower than V_{FB_OLP} (typically 1.7V). If this fault is present for more than T_{D_OLP} (typically 120m), the protection will be triggered, the IC will experience an auto-restart mod.

- **Abnormal Over Current Protection (AOCP)**

When in heavy load or output short condition, the inductor current may be increased too large. To avoid system components damaged, there's a abnormal over current limit (typically 0.9V) for CS Pin. When the CS voltage is larger than this threshold, the internal power MOSFET is turned off immediately and is to be turned on again after 48μs.

- **On Chip Thermal Shutdown**

KP3251X integrates thermal shutdown function. When the IC junction temperature is higher than T_{SD} (typically 150 ˚C), IC shuts down and enters into auto-restart mode.

- **Enhanced Dynamic Response**

In KP3251X, the dynamic response performance is optimized to reduce output drop in load transient.

- **Audio Noise Free Operation**

In KP3251X, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

- **VDD Over Voltage Protection (OVP) and Zener Clamp**

When VDD voltage higher than V_{DD_OVP} (typically 28.5V), the IC will stop switching. This will cause VDD fall down to be lower than V_{DD_OFF} (typically 6.7V) and then the system will restart up again. An internal 30V (typical) zener clamp is integrated to prevent the IC from damage.

- **Protections with Auto-Restart**

In the event of protections, the IC enters into auto-restart and an internal timer begins counting, wherein the power MOSFET is disabled. When $T_{Auto\_Recovery}$ (typically 1.2s) had been counted, the IC will reset and start up the system again. However, if the fault still exists, the system will experience the above mentioned process.

- **Soft Totem-Pole Gate Driver**

KP3251X has a soft totem-pole gate driver with optimized EMI performance.

Application Information

- **PCB Layout Guidelines**

Good PCB layout is very important to KP3251X's operation, which helps to improve system reliability, EMI and thermal performance. Follow below guidelines to optimize performance.

(1) Power Loop Routing:

As shown in fig.2, minimize the power loop area of ① and ② as small as possible. Power loop ① is formed by input capacitor–IC–inductor–output capacitor. Power loop ② is formed by inductor–output capacitor–freewheeling diode. Make sure these two loop area reduce to its minimum.

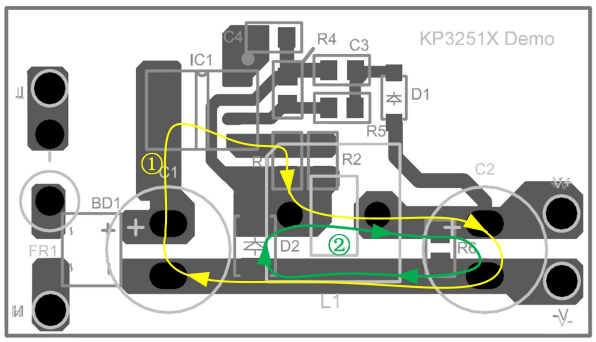


Fig.2

(2) Feedback Routing:

As shown in fig.3, the feedback loop③ is formed by inductor–feedback diode – FB divided resistor//FB capacitor – IC. This loop is most important to system operation. Make sure these guidelines below been checked when layout: a) Put the feedback loop out of the main power loop ① and ②, and minimize this loop area as small as possible; b) Do not route FB pin line too long, and do not route this line beneath the IC, or system may not operation normally; c) Put the components (FB divided resistor and FB capacitor) of this loop close to IC as much as possible, and far away from the power inductor; d) Place the output feedback point at the positive of the output capacitor, and do not route this line beneath the power inductor or freewheeling diode in case high-frequency noise coupled; e) Make sure signal ground of FB line and IC are connected first, then connect to power ground of inductor through a single point.

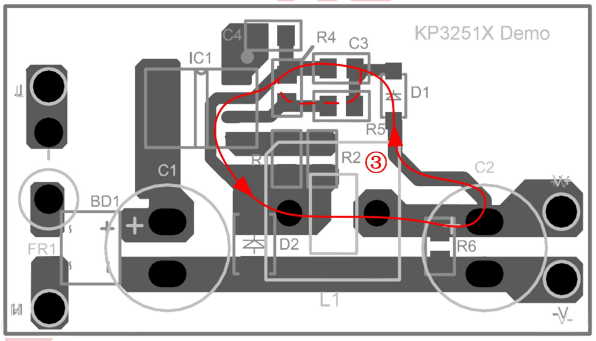


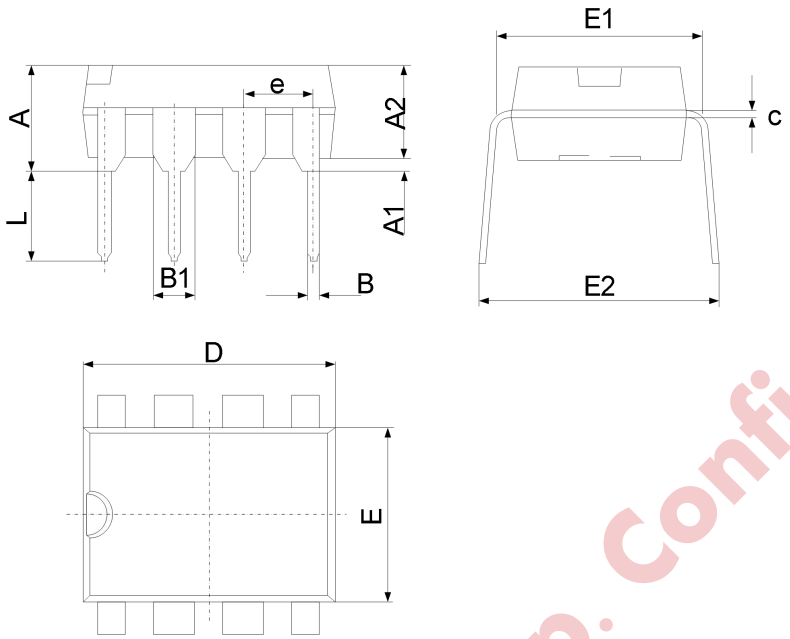
Fig.3

(3) Additional Notes:

a) When π filter circuit is added after the bridge, make sure power inductor far away from the π filter inductor; b) Connect the drain pin of KP3251X to a large cooper area to improve thermal performance if possible.

Package Dimension

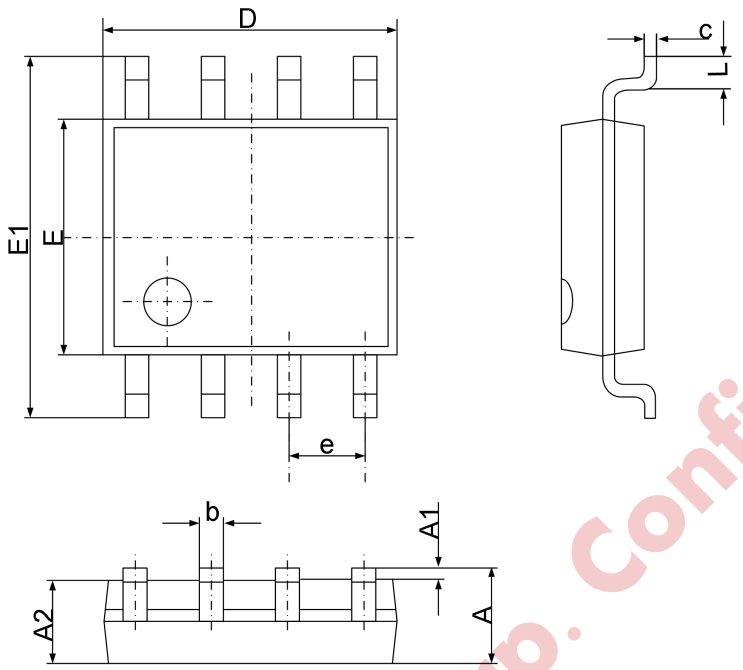
DIP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	3.600	4.150	0.142	0.163
A1	0.510	-	0.020	-
A2	3.150	3.400	0.124	0.134
B	0.380	0.560	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
c	0.200	0.350	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.500	0.244	0.256
E1	7.620 (REF)		0.300 (REF)	
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	7.620	9.300	0.300	0.366

Package Dimension

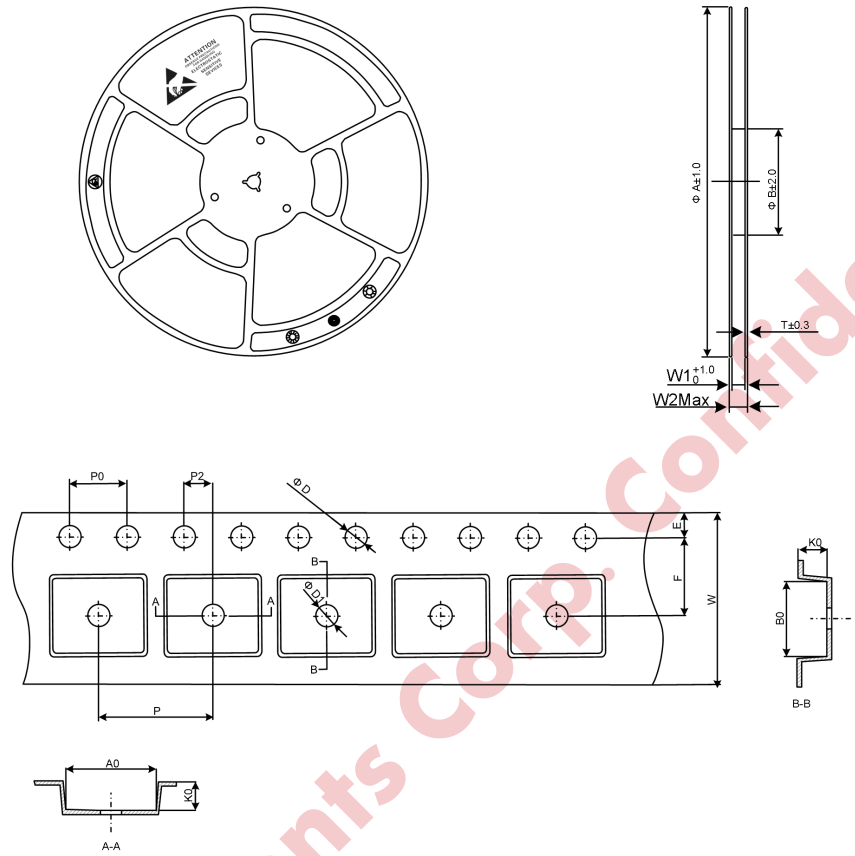
SOP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050

Tape and Reel Information

SOP-8



Reel Dimensions (mm)				
A	**B (Inner Diameter)**	**W1**	**W2 Max**	**T**
330	100	12.4	18.4	1.5

Tape Dimensions			
Symbol	**Dimensions (mm)**	**Symbol**	**Dimensions (mm)**
E	1.75±0.10	W	12.00±0.10
F	5.50±0.10	P	8.00±0.10
P2	2.00±0.10	A0	6.60±0.10
D	$1.50^{+0.1}_{-0}$	B0	5.30±0.10
D1	1.55±0.05	K0	1.90±0.10
P0	4.00±0.10		

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