

Fixed 12V Output, High Performance Low Cost PWM Power Switch

FEATURES

- Fixed 12V Output
- Integrated with 650V Power MOSFET and HV Startup Circuit
- Optimize Audible Noise, Improve System Stability
- Multi-Mode Control with Audio Noise Free Operation
- Supports Buck and Buck-Boost Topologies
- Green Mode Operation for High Efficiency
- Good Line and Load Regulation
- Built-in Soft Start
- Build in Protections:
 - Over Load Protection (OLP)
 - Cycle-by-Cycle Current Limiting (OCP)
 - Output OVP
 - VDD OVP, UVLO & Clamp
- Available with SOP-8/DIP-7 Package

APPLICATIONS

- Small Home Appliance
- Industry Controls

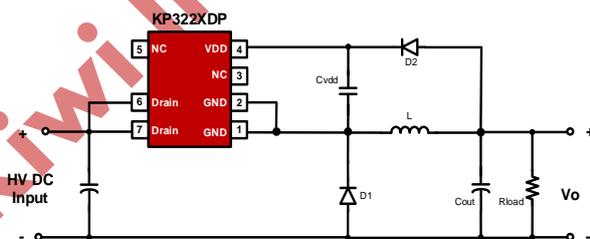
GENERAL DESCRIPTION

KP322X family is a high performance Switch Mode Power Supply Switcher for low power off-line application with minimum components in typical buck solution. This family has built-in high break down voltage MOSFET to withstand high surge input.

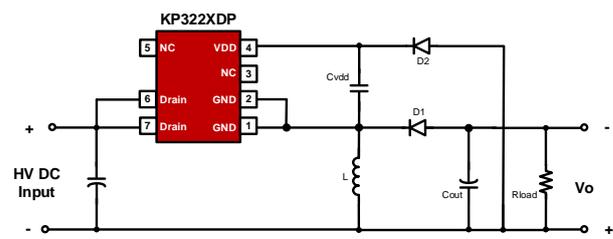
Unlike conventional PWM control, there's no fixed internal clock in KP322X family to trigger the GATE driver, the switching frequency is changed according to the load condition. The multi-mode PWM control is integrated to simplify circuit design and achieve good line and load regulation without audio noise generated. The peak current limit changes according to the real load condition for low standby power in no load.

KP322X integrates functions and protections of Under Voltage Lockout (UVLO), Cycle-by-cycle Current Limiting (OCP), Output OVP, On-chip Thermal Shutdown, Over Load Protection (OLP), VDD OVP with Auto Recovery Mode Protection, etc.

TYPICAL APPLICATION CIRCUIT

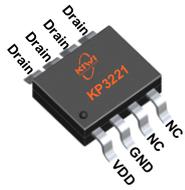


BUCK

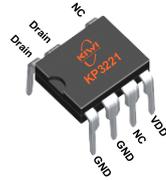


BUCKBOOST

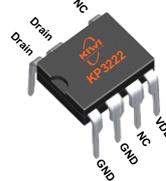
Pin Configuration



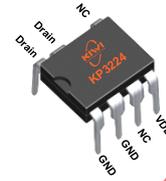
SOP-8



DIP-7



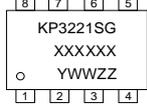
DIP-7



DIP-7

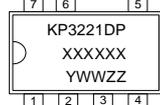
Marking Information

XXXXXX: Wafer lot Code
 Y: Year Code
 WW: Week Code, 01-52
 ZZ: Serial Number, 01-99 or A0-ZZ



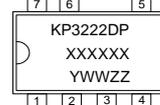
SOP-8

XXXXXX: Wafer lot Code
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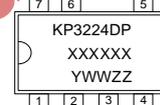
DIP-7

XXXXXX: Wafer lot Code
 Y: Year Code
 WW: Week Code, 01-52
 ZZ: Serial Number, 01-99 or A0-ZZ



DIP-7

XXXXXX: Wafer lot Code
 Y: Year Code
 WW: Week Code, 01-52
 ZZ: Serial Number, 01-99 or A0-ZZ



DIP-7

Typical Output Power Table

Part Number	Package	R _{dson}	Input Voltage	Steady Load (12V)	Peak Load (12V)
KP3221SG	SOP-8	10Ω	150-265Vac	300mA	400mA
			85-265Vac	250mA	350mA
KP3221DP	DIP-7	10Ω	150-265Vac	300mA	400mA
			85-265Vac	250mA	350mA
KP3222DP	DIP-7	4.0Ω	150-265Vac	500mA	700mA
			85-265Vac	400mA	600mA
KP3224DP	DIP-7	2.0Ω	150-265Vac	600mA	800mA
			85-265Vac	500mA	700mA

Note:

1. Default for Buck Converter Application
2. Steady load means maximum load which hold above 2hours at 75°C half-sealed environment.
3. Peak load means maximum load which hold above 1min at 75°C half-sealed environment.

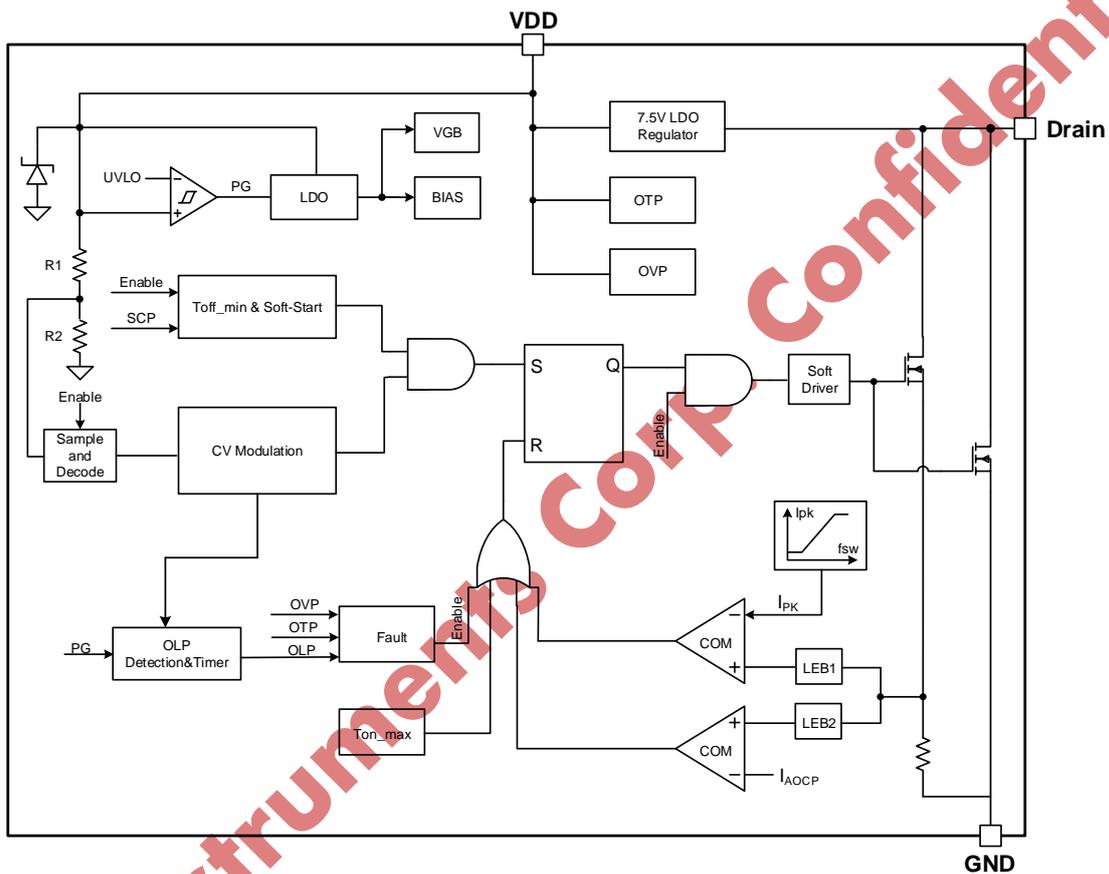
Pin Description

SOP-8	DIP-7	Pin Name	I/O	Description
2	1,2	GND	P	The ground reference for the IC
3,4	3	NC	/	No Connection
1	4	VDD	I	The power supply and the output voltage feedback pin. For the normal operation, a capacitor with 1μF is recommended to connect to this pin
	5	NC	/	No Connection
5,6,7,8	6,7	Drain	P	The Power MOSFET Drain

Ordering Information

Part Number	Description
KP3221SGA	SOP-8, Halogen free, in T&R, 4000Pcs/Reel
KP3221DP, KP3222DP, KP3224DP	DIP-7, Halogen free, 50 Pcs/Tube

Block Diagram



Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit	
Drain Pin Voltage Range	-0.3 to 650	V	
VDD DC Supply Voltage	-0.3 to 30	V	
VDD DC Clamp Current	10	mA	
Package Thermal Resistance – Junction to Ambient (SOP-8)	165	°C/W	
Package Thermal Resistance – Junction to Ambient (DIP-7)	105	°C/W	
Maximum Junction Temperature	160	°C	
Storage Temperature Range	-65 to 150	°C	
Lead Temperature (Soldering, 10sec.)	260	°C	
ESD Capability, HBM (Human Body Model)	4.5	kV	
Maximum Internal MOSFET DC Drain Current	KP3221	1	A
	KP3222	2	A
	KP3224	4	A
Maximum Internal MOSFET Pulse Drain Current (Continues 100µs)	KP3221	4	A
	KP3222	8	A
	KP3224	16	A

Recommended Operation Conditions

Parameter	Value	Unit
Operating Junction Temperature	-40 to 125	°C
Operation Switching Frequency	40 to 60	kHz

Electrical Characteristics (Ta = 25°C, If Not Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High Voltage Startup Section (HV Pin)						
I _{HV}	HV Charging Current	Drain=40V, VDD=6V	0.9	1.7	2.1	mA
I _{HV_leakage}	HV Leakage Current	Drain=650V, VDD=20V			50	µA
Supply Voltage Section (VDD Pin)						
V _{DD_ON}	VDD Under Voltage Lockout Exit			8.7		V

V _{DD_OFF}	VDD Under Voltage Lockout Enter		6.1	7.2	8.1	V
V _{DD_Reg1}	VDD Regulation Voltage	FB is floating	12.4	12.6	12.8	V
I _{VDD_st}	Start-up Current	No switching		220		μA
I _{VDD_Op}	Operation Current	Fsw=60kHz		800		μA
I _{VDD_Q}	Quiescent Current		115	220	275	μA
V _{DD_OVP}	VDD OVP Threshold		14.8	16	17.2	V
T _{D_OVP}	VDD OVP Debounce Cycle			5		cycle
V _{DD_Clamp}	VDD Clamp Voltage	I _{VDD} =10mA	28	30	32	V
V _{DD_OLP}	VDD OLP Voltage			8.5		V
T _{D_OLP}	VDD OLP Debounce Time			120		ms
Timer Section						
T _{OFF_min_norm}	Normal Minimum OFF time		14.5	16	17.5	μs
T _{OFF_max_nom}	Nominal Maximum OFF Time			2.3		ms
T _{OFF_max_FDR}	Maximum OFF Time in Fast Dynamic Response Mode			420		μs
T _{ON_max}	Maximum ON Time		9	12	15	μs
T _{SS}	Internal Soft Start Time			3		ms
T _{Auto_Recovery}	Protection Auto Recovery Debounce Time			1.5		s
On-Chip Thermal Shutdown						
T _{SD}	Thermal Shutdown Trigger Point	(Note 2)		150		°C
Internal Current Sense Section						
T _{LEB}	Leading Edge Blank			350		ns
T _{D_OCP}	OCP Delay			100		ns
I _{PK}	Internal Peak Current	KP3221	0.53	0.58	0.63	A
		KP3222	1.0	1.1	1.2	A
		KP3224	1.53	1.7	1.87	A
I _{AOCP}	Abnormal Peak Current	KP3221		0.87		A
		KP3222		1.65		A
		KP3224		2.55		A



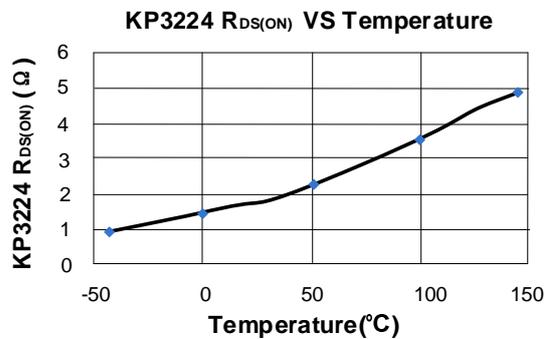
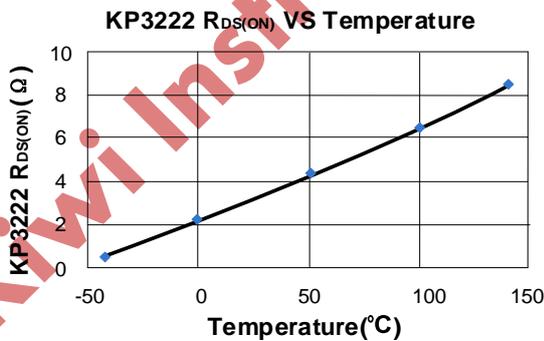
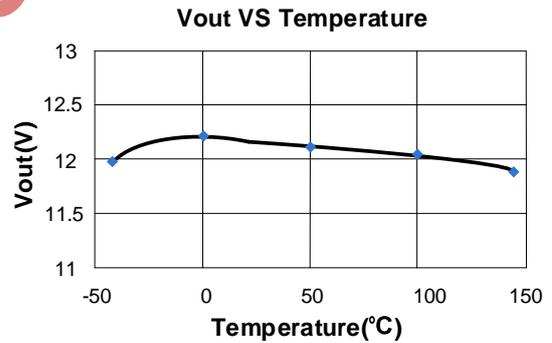
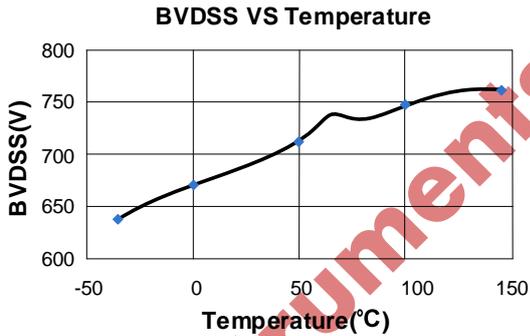
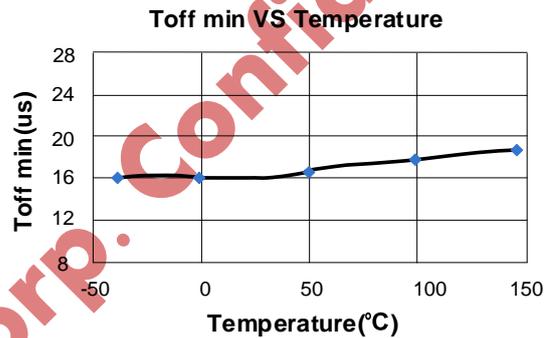
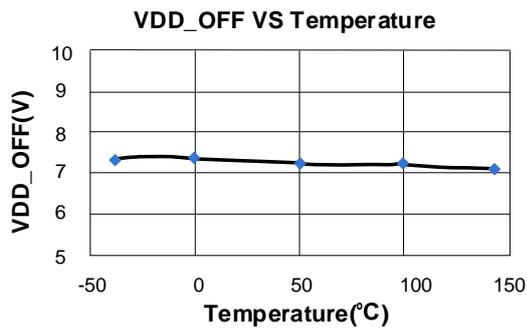
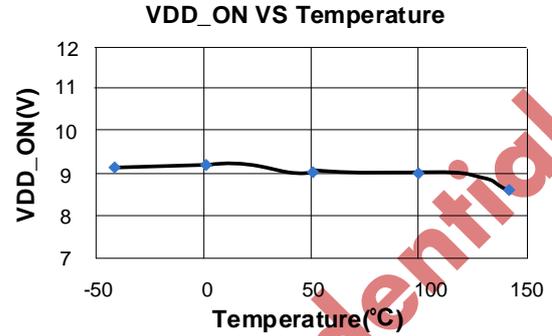
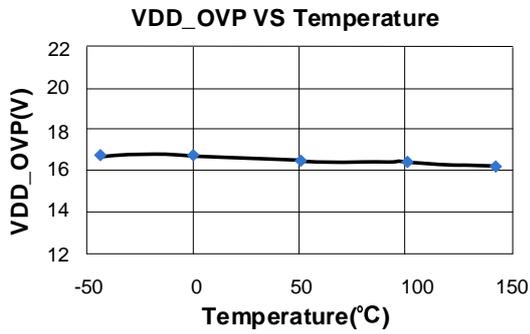
Power MOSFET Section (Drain Pin)						
V_{BR}	Power MOSFET Drain Source Breakdown Voltage		650			V
R_{dson}	Static Drain-Source On Resistance	KP3221		10		Ω
		KP3222		4		Ω
		KP3224		2		Ω

Note 1. Stresses listed as the above “Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Guaranteed by design.

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Characterization Plots



Operation Description

KP322X family integrates a high voltage power MOSFET switch and a multi-mode PWM controller. It is optimized for 12V fixed off-line non-isolated buck or buck-boost applications in small home appliances and linear regulator replacement. The IC utilizes the multi-mode PWM control to regulate output with high precision and lowest components count.

- **Very Low Operation Current**

The standby operating current in KP322X is as small as 200 μ A (typical). The small operating current results in higher efficiency and reduces the VCC hold-up capacitance requirement.

- **High Voltage Start-Up Operation**

In KP322X, a 650V high voltage startup cell is integrated. During startup, the internal startup circuit is enabled and a HV current source charges the VDD hold up capacitor C_{vdd} through Drain pin, as shown in "Block Diagram". When VDD reaches UVLO turn-on voltage (7.5V typical), the IC begins switching and the IC current consumed increased to 0.8mA (typical). The VDD is charged by the output through the feedback diode in steady state, which result in less than 100mW standby power with the combination of high voltage startup cell.

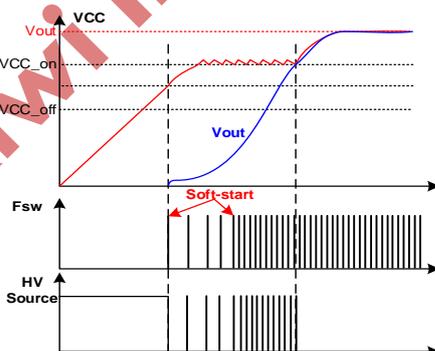


Fig.1

- **Current Limit and Leading Edge Blanking**

There's a programmable current limit for current sensing voltage from internal CS sense circuit, which is changed according to the system switching frequency. When the sampled voltage exceeds the internal threshold, the power MOSFET is turned off for the remainder of that cycle. An internal leading edge blanking circuit is built in. During this blanking period (300ns, typical), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the GATE driver.

- **Soft Start**

KP322X features an internal 3ms (typical) soft start that slowly increases the switching frequency during startup sequence (T_{off} decrease from 100 μ s to 30 μ s). Every restart attempt is followed by the soft start activation.

- **Multi-Mode PWM Control**

To meet the tight requirement of averaged system efficiency and no load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in KP322X which is shown in the Fig 2.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 100mW.

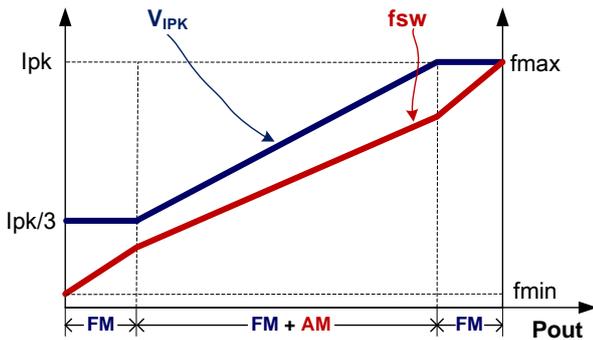


Fig.2

- **Over Load Protection (OLP) / Short Load Protection (SLP)**

If over load or short load condition occurs, the output voltage drops down to be lower than V_{DD_OLP} . If this fault is present for more than 120ms (typical), the protection will be triggered, the IC will experience an auto-restart mode (as mentioned below).

- **Abnormal Over Current Protection (AOCP)**

When in heavy load or output short condition, the inductor current may be increased too large. To avoid system components damaged, there's a abnormal over current limit circuit. When the internal CS voltage is larger than this threshold, the internal power MOSFET is turned off immediately and is to be turned on again after 120 μ s.

- **On Chip Thermal Shutdown**

KP322X integrates thermal shutdown function. When the IC junction temperature is higher than 150 $^{\circ}$ C, IC shuts down and enters into auto-restart mode (as mentioned below).

- **Enhanced Dynamic Response**

In KP322X, the dynamic response performance is optimized to reduce output drop in load transient.

- **Audio Noise Free Operation**

In KP322X, the optimized combination of frequency modulation and internal CS current modulation algorithm can provide audio noise free operation from full loading to zero loading.

- **VDD Over Voltage Protection (OVP) and Zener Clamp**

When VDD voltage higher than V_{DD_OVP} (typically 16V), the IC will stop switching. This will cause VDD fall down to be lower than V_{DD_OFF} (typically 7V) and then the system will restart up again. An internal 30V (typical) zener clamp is integrated to prevent the IC from damage.

- **Protections with Auto-Restart**

In the event of protections, the IC enters into auto-restart and an internal timer begins counting, wherein the power MOSFET is disabled. When 1.5s had been counted, the IC will reset and start up the system again. However, if the fault still exists, the system will experience the above mentioned process.

- **Soft Totem-Pole Gate Driver**

KP322X has a soft totem-pole gate driver with optimized EMI performance.

Typical Reference Design

● Inductor Calculation

In order to balance the thermal affection, recommend KP322X work in DCM mode. Detail calculation shows below:

$$L=(V_o+V_f)*I_{o_olp}/\eta/(1/2*I_{pk}^2*F_{sw_max})$$

V_o : Output Voltage;

V_f : Forward voltage on freewheeling diode ;

I_{o_olp} : Output Over Current, typical 1.1-1.2 times of normal Output Current;

η : system efficiency, typical 0.8;

I_{pk} : Peak inductor current, change with different IC Part;

F_{sw_max} : Default set 40-50kHz;

Take KP3282DP as example, set output as 18V-400mA:

Set $I_{o_olp}=1.2*I_o=0.48A$; $V_f=0.7V$; $\eta=0.8$;
 $I_{pk}=1.1A$; $F_{sw_max}=50kHz$;

$$L=(18V+0.7V)*0.48A/0.8/(1/2*1.1A/1.1A/50kHz)=0.37mH.$$

Choose $L=0.37mH$ & $I_{sat}>1.65A$ (KP3282 laocp) as the specific inductor parameter demand.

Blow shows the proper L value according to different part and spec

IC	KP3221 SGA	KP3221 DP	KP3222 DP	KP3224 DP
Spec	12V-250mA	12V-250mA	12V-500mA	12V-600mA
L Value	0.7-1.6mH	0.7-1.6mH	0.4-0.5mH	0.2-0.3mH
Isat.	>0.87A	>0.87A	>1.65A	>2.55A

Meanwhile, large value inductor offers more power but leads to much heat dissipation due to deep CCM Mode; Small value inductor could reduce the size of inductor but LEB limit the minimum value. Detail shows below:

IC	KP3221 SGA	KP3221 DP	KP3222 DP	KP3224 DP
Lmin	0.5mH	0.5mH	0.26mH	0.2mH

● Input and Output Capacitor Selection

Output Capacitor Selection: for normal application, output capacitor is choose between 330 μ F-680 μ F according to actual output voltage ripple.

Input Capacitor Selection: for normal application, output capacitor is choose between 10 μ F-20 μ F according to load variation.

● Dummy Load Selection

Dummy Load Selection: heavy dummy load could suppress the output voltage from floating up, but too heavy dummy load would enlarge the standby power loss; take balance among load regulation and standby power loss.

8-10k dummy load is recommended in KP322X system for good output regulation and low dummy load power loss (~20mW)

Typical Application Diagram

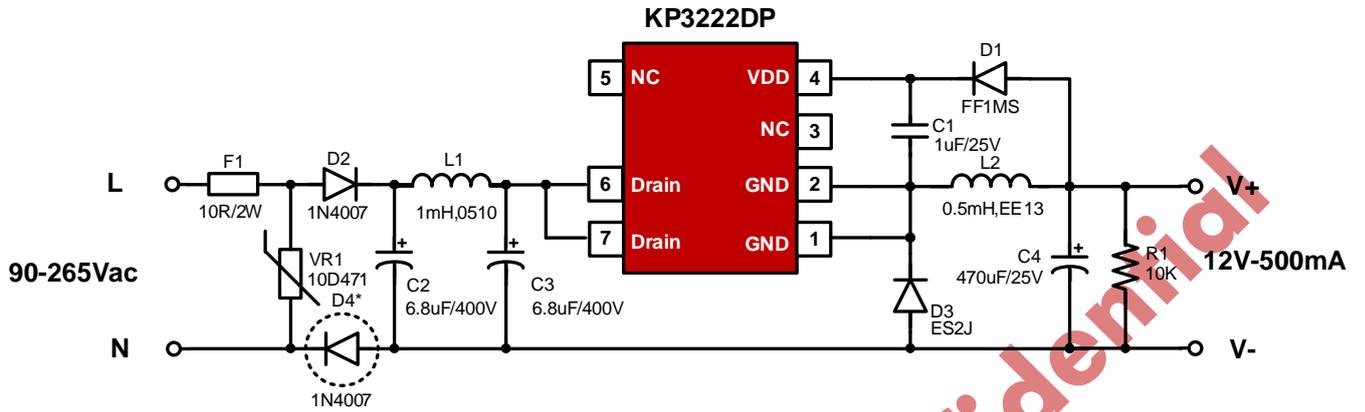
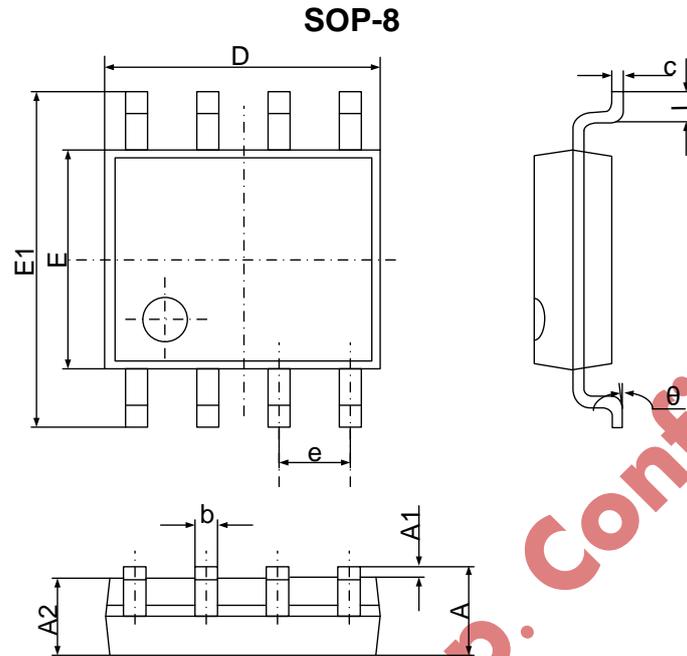
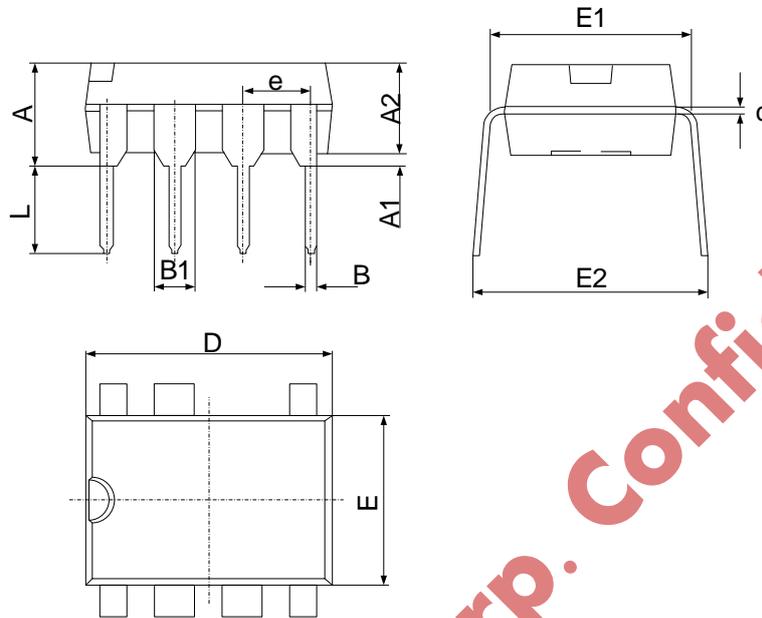


Fig.3 Typical Diagram

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Package Dimension


Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Dimension (Continued)
DIP-7


Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	3.600	4.150	0.142	0.163
A1	0.510	-	0.020	-
A2	3.150	3.400	0.124	0.134
B	0.380	0.560	0.015	0.022
B1	1.520 (BSC)		0.060 (BSC)	
c	0.200	0.350	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.500	0.244	0.256
E1	7.620 (REF)		0.300 (REF)	
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	7.620	9.300	0.300	0.366



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