Fixed 5V Output, High Performance Low Cost PWM Power Switch

FEATURES

- **Fixed 5V Output**
- **Integrated with 650V Power MOSFET and HV Startup Circuit**
- **Multi-Mode Control with Audio Noise Free Operation**
- **Supports Buck and Buck-Boost Topologies**
- **Less than 100mW Standby Power Loss**
- **Excellent Line and Load Regulation**
- **Built-in Soft Start**
- **Build in Protections:**
  - **Over Load Protection (OLP)**
  - **Cycle-by-Cycle Current Limiting (OCP)**
  - **Output Over Voltage Protection (OVP)**
  - **FB Abnormal Protection**
  - **Abnormal Over Current Protection (AOCP)**
  - **Over Temperature Protection (OTP)**
- **Available with SOP-8 Package**

APPLICATIONS

- **Auxiliary Power Supply**
- **Smart Home Appliance**

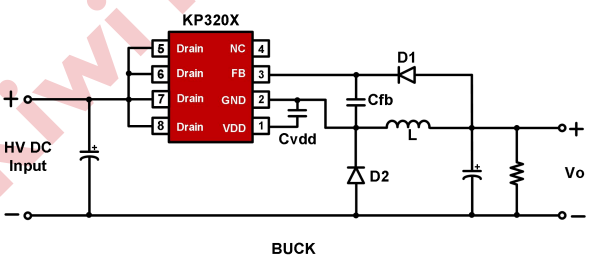
GENERAL DESCRIPTION

KP320X family is a high performance PWM power switch for low power off-line application with minimum components in typical buck solution. This family has built-in high break down voltage MOSFET to withstand high surge input.

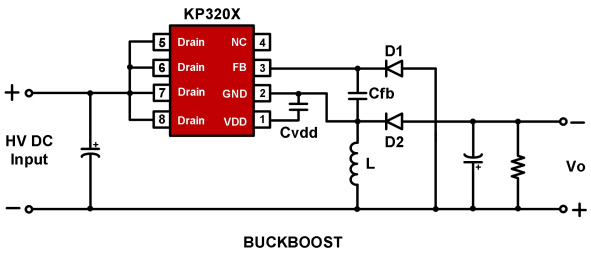
Unlike conventional PWM control, there's no fixed internal clock in KP320X to trigger the gate driver. The switching frequency is changed according to the load condition. The multi-mode PWM control is integrated to simplify circuit design and achieve good line and load regulation without audio noise generated. The peak current limit changes according to the real load condition for low standby power in no load.

KP320X integrates functions and protections of Under Voltage Lockout (UVLO), Cycle-by-cycle Current Limiting (OCP), Output Over Voltage Protection (OVP), Over Temperature Protection (OTP), FB Abnormal Protection, Over Load Protection (OLP) etc.

TYPICAL APPLICATION CIRCUIT

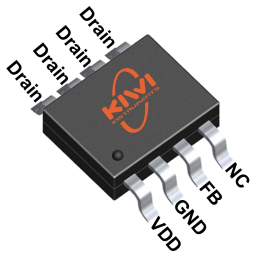


BUCK



BUCKBOOST

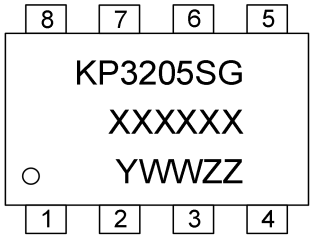
Pin Configuration



SOP-8

Marking Information

XXXXXX: Wafer Lot Code
Y: Year Code
WW: Week Code, 01-52
ZZ: Serial Number, 01-99 or A0-ZZ



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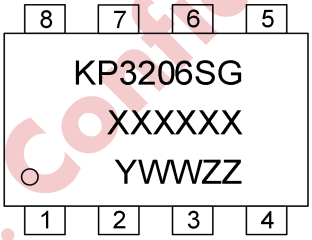


SOP-8

Typical Output Power Table (1)

Product	Package	R_{dson}	Output Current @85-265Vac, 5V
KP3205	SOP-8	20Ω	Io<250mA
KP3206	SOP-8	3.85Ω	Io<500mA

(1) Default for Buck Converter Application, and the practical output power is determined by the output voltage and thermal condition.

Pin Description

Pin Number	Pin name	I/O(2)	Description
1	VDD	I/O	The power supply pin
2	GND	G	The ground of the chip
3	FB	I	The output voltage feedback pin
4	NC	-	No Connection
5, 6, 7, 8	Drain	P	The Power MOSFET Drain

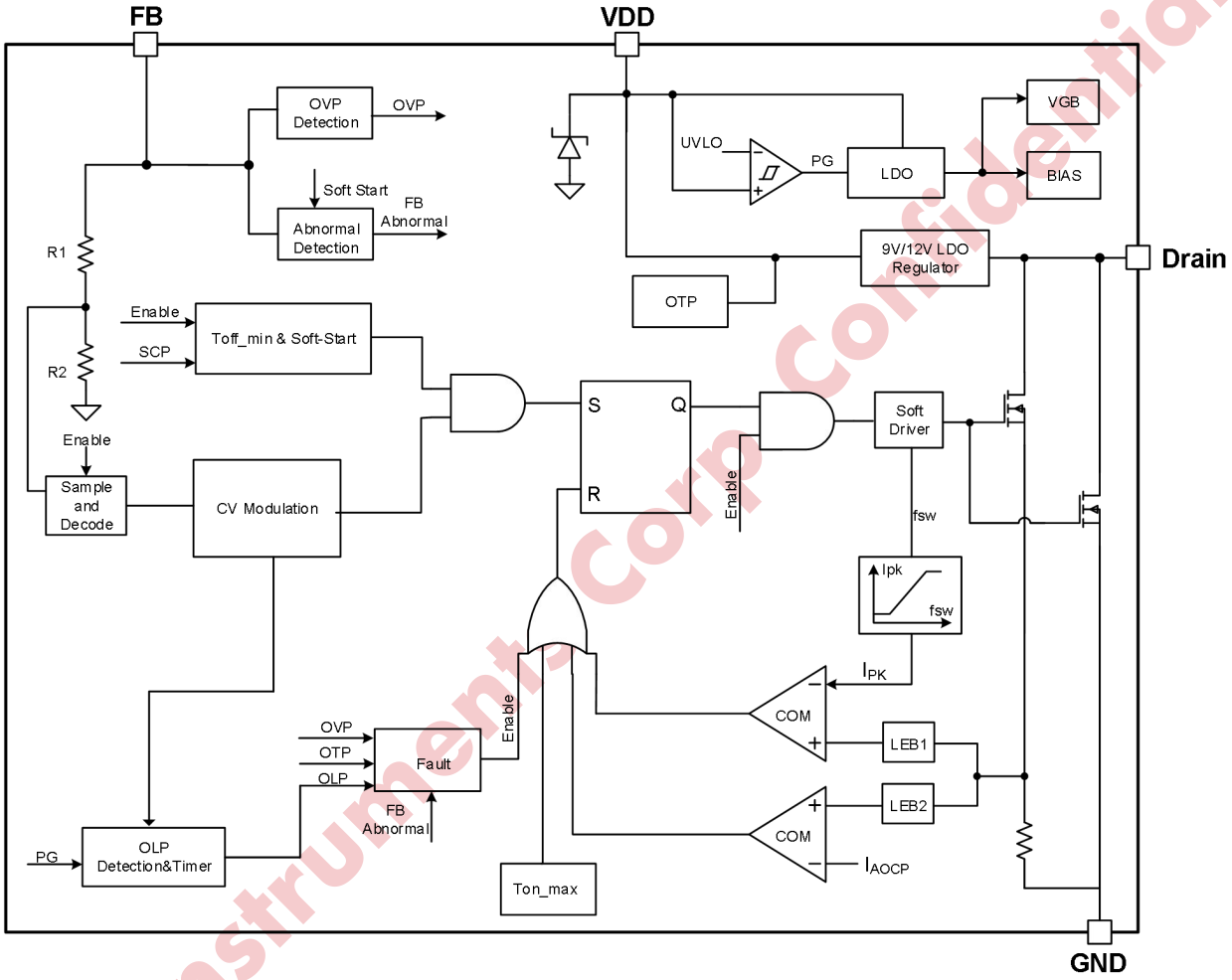
(2) I – Input; P - Power; G – Ground; I/O - Input/Output

Ordering Information

Part Number [3]	Description
KP3205SGA	SOP-8, Halogen Free in T&R, 4000 Pcs/Reel
KP3206SGA	SOP-8, Halogen Free in T&R, 4000 Pcs/Reel

(3) Suffix "A" – Tape & Reel.

Block Diagram



Absolute Maximum Ratings (4)

Parameter		Value	Unit
Drain - GND Voltage Range		-0.3 to 650	V
VDD - GND Voltage Range		-0.3 to 30	V
VDD Pin Clamp Current		10	mA
FB - GND Voltage Range		-0.3 to 8.5	V
Package Thermal Resistance – Junction to Ambient (SOP-8)		165	°C/W
Maximum Junction Temperature		150	°C
Storage Temperature Range		-65 to 150	°C
Lead Temperature (Soldering, 10sec.)		260	°C
ESD Capability, HBM (Human Body Model) (5)		3	kV
ESD Capability, CDM (Charged Device Model) (6)		2	kV
Maximum Internal MOSFET DC Drain Current	KP3205	0.6	A
	KP3206	2	A
Maximum Internal MOSFET Pulse Drain Current (Continues 100μs)	KP3205	2.4	A
	KP3206	8	A

(4) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(5) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(6) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operation Conditions

Parameter	Value	Unit
Operating Ambient Temperature	-40 to 125	℃
Operation Switching Frequency	40 to 60	kHz

Electrical Characteristics (Ta = 25℃, If Not Otherwise Noted)

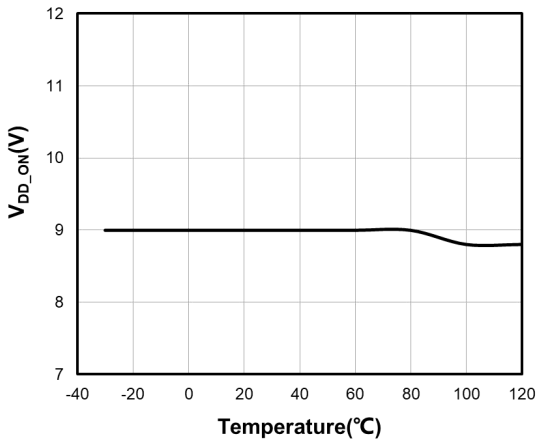
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
High Voltage Startup Section (Drain Pin)						
I_{Drain}	Drain Charging Current	Drain = 650V, VDD = 0V		2		mA

$I_{Drain\_leakage}$	Drain Leakage Current	Drain = 650V, VDD = 12V			100	μA
V_{BR}	Power MOSFET Drain Source Breakdown Voltage		650	690		V
R_{dson}	Static On Resistance	KP3205		20		Ω
		KP3206		3.85		Ω
Supply Voltage Section (VDD Pin)						
V_{DD_ON}	VDD Under Voltage Lockout Exit		7.4	9.0	10.6	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter		6.1	7.0	8.1	V
V_{DD_Reg}	VDD Regulation Voltage			12		V
I_{VDD_st}	VDD Start-up Current		90	180	260	μA
I_{VDD_Q}	VDD Quiescent Current	No switching	110	200	280	μA
V_{DD_Clamp}	VDD Clamp Voltage	IVDD = 5mA	27.8	30	32.2	V
Feedback Section (FB Pin)						
V_{FB_REF}	Internal Error Amplifier (EA) Reference Input		5.35	5.5	5.65	V
V_{FB_OVP}	Output Over Voltage Protection (OVP) Threshold			6.8		V
T_{D_OVP}	OVP Debounce Cycle			5		cycle
V_{FB_OLP}	Output Over Load Protection (OLP) Threshold			3.6		V
T_{D_OLP}	Over Loading Debounce Time			120		ms
V_{FB_abn}	Feedback Diode Floating Detection Voltage @ Soft Start			160		mV
V_{FB_st}	FB Abnormal Detection Voltage @ Startup			140		mV
Internal Current Sense Section						
T_{LEB}	Leading Edge Blank			350		ns
I_{LIMIT}	Peak Power MOS Current	KP3205	0.3	0.34	0.38	A
		KP3206	1.05	1.2	1.35	A
$I_{cs\text{-}min}$	Minimum Power MOS Current	KP3205		90		mA
		KP3206		320		mA
I_{AOCP}	Abnormal Peak Power MOS Current	KP3205		0.44		A
		KP3206		1.56		A
Timer Section						
$T_{OFF\_min\_norm}$	Normal Minimum OFF time		14.5	16	17.5	μs
$T_{OFF\_max\_nom}$	Nominal Maximum OFF Time			2.3		ms

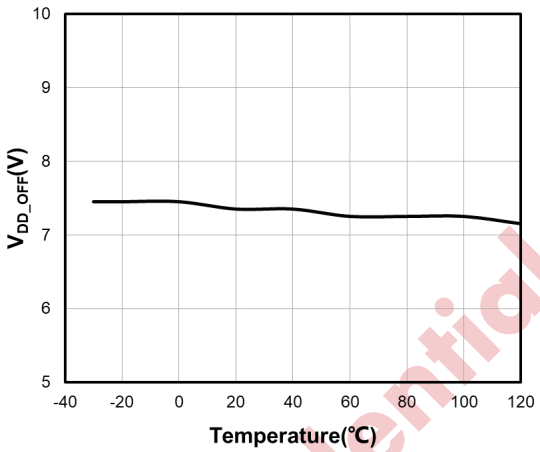
T_{ON_max}	Maximum ON Time		9.9	12	14.4	μs
T_{ss}	Internal Soft Start Time			8		μs
$T_{Auto\_Recovery}$	Auto Recovery Debounce Time			1.2		ms
On-Chip Thermal Shutdown						
T_{SD}	Thermal Shutdown Trigger Point(7)			150		˚C
T_{hy}	Thermal Shutdown Hysteresis(7)			20		˚C

(7) Guaranteed by design.

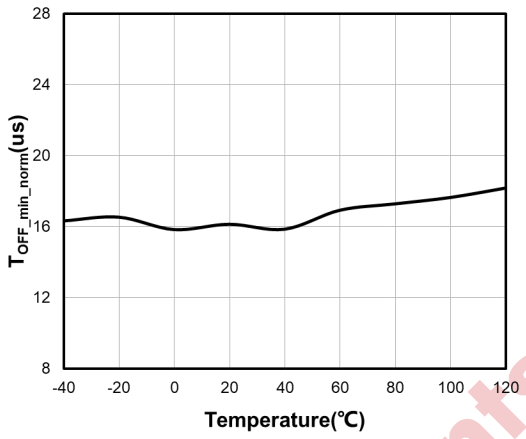
Typical Characteristic



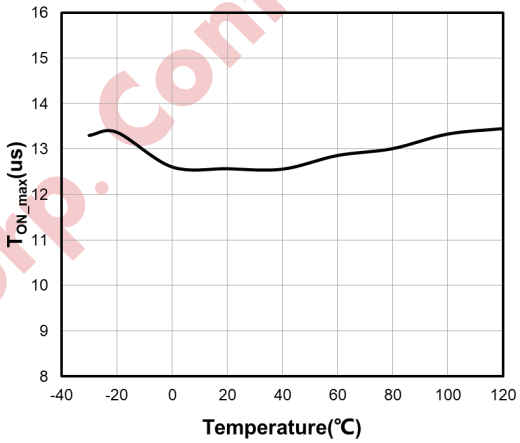
V_{DD_ON} vs Temperature



V_{DD_OFF} vs Temperature



$T_{OFF\_min\_norm}$ vs Temperature



T_{ON_max} vs Temperature

Operation Description

KP320X family integrates a high voltage power MOSFET switch and a multi-mode PWM controller. It is optimized for 5V fixed off-line non-isolated buck or buck-boost applications in small home appliances and linear regulator replacement. The IC utilizes the multi-mode PWM control to regulate output with high precision and lowest components count.

● Very Low Operation Current

The standby operating current (I_{VDD_Q}) in KP320X is as small as 200μA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

● High Voltage Start-Up Operation and Ultra Low Standby Power (<100mW)

In KP320X, a 650V high voltage startup cell is integrated. During startup, the internal startup circuit is enabled and a HV current source charges the VDD hold up capacitor Cvdd through Drain pin, as shown in “Block Diagram”. The IC begins to work until Cvdd rises to V_{DD_ON} (9V, typical). The VDD is still charged by the JFET to V_{DD_REG}(12V typical), which means less than 100mW standby power with the combination of high voltage startup cell.

● Current Limit (OCP) and Leading Edge Blanking (LEB)

There’s a programmable current limit for current sensing voltage from internal CS sense circuit, which is changed according to the system switching frequency. When the sampled voltage exceeds the internal threshold, the power MOSFET is turned off for the remainder of that cycle. An internal leading edge blanking circuit is built in. During this blanking period T_{LEB} (350ns, typical), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the gate driver.

● Soft Start

KP320X features an internal T_{SS} (8ms, typical) soft start that slowly increases the switching frequency during startup sequence (Toff decrease from 100μs to 16μs). Every restart attempt is followed by the soft start activation.

● Multi-Mode PWM Control

To meet the tight requirement of averaged system efficiency and no-load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in KP320X which is shown in the Fig 1.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 100mW.

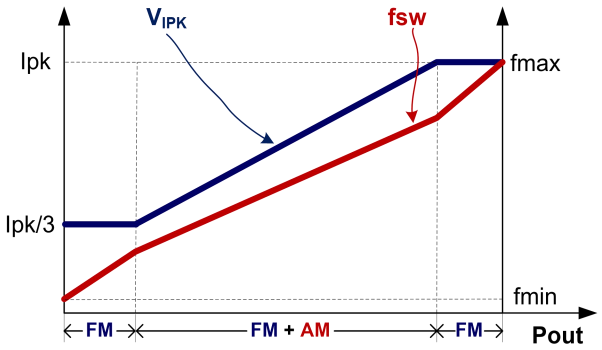


Fig.1

● Over Load Protection (OLP) / Short Load Protection (SLP)

If over load or short load condition occurs, the output feedback voltage drops down to be lower than V_{DD_OLP} (3.6V, typical). If this fault is present for more than T_{D_OLP} (120ms, typical), the protection will be triggered, and the IC will experience an auto-restart mode (as mentioned below).

- **Abnormal Over Current Protection (AOCP)**

When in heavy load or output short condition, the inductor current may be increased too large. To avoid system components damaged, there's an abnormal over current limit circuit I_{AOCP}. When the internal CS voltage is larger than this threshold, the internal power MOSFET is turned off immediately and is to be turned on again after 100μs.

- **Over Temperature Protection (OTP)**

KP320X integrates thermal shutdown function. When the IC junction temperature is higher than T_{SD} (150 ˚C , typical), IC shuts down and enters auto-restart mode (as mentioned below).

- **Enhanced Dynamic Response**

In KP320X, the dynamic response performance is optimized to reduce output drop in load transient.

- **Audio Noise Free Operation**

In KP320X, the optimized combination of frequency modulation and internal CS current modulation algorithm can provide audio noise free operation from full loading to zero loading.

- **Over Voltage Protection (OVP)**

When FB voltage higher than V_{FB_OVP} (6.8V, typical), the IC will stop switching. Then the system will experience an auto-restart mode.

- **VDD Zener Clamp (V_{DD_Clamp})**

An internal 30V (typical) zener clamp is integrated to prevent the IC from damage.

- **FB Abnormal Detection**

KP320X integrates FB abnormal detection to avoid system damage due to FB float or short during startup. When FB is float or short, IC shuts down immediately during startup, so that output voltage would maintain at a relatively low value in case of damaging the system.

- **Protections with Auto-Restart**

In the event of protections (OLP/OTP/OVP/FB Abnormal Detection), the IC enters into auto-restart and an internal timer begins counting, wherein the power MOSFET is disabled. When $T_{Auto\_Recovery}$ (1.2s, typical) had been counted, the IC will reset and start up the system again. However, if the fault still exists, the system will experience the above-mentioned process.

Application Information

● PCB Layout Guidelines

PCB layout design has a significant impaction on the performance of power supply， which helps KP320X to improve system reliability, EMC and thermal performance. Follow below guidelines to optimize performance.

1. The main power loop (Loop1) should be as small as possible, and the trace should be wide for better efficiency performance.
2. Feedback Routing (Loop2): a) Put the feedback loop out of the main power loop， and minimize this loop area as small as possible; b) Do not route FB pin line too long and beneath the IC, or system may not operation normally; c) Put the components of this loop close to IC as much as possible, and far away from the power inductor; d) Place the output feedback point at the positive of the output capacitor, and do not route this line beneath the power inductor or freewheeling diode in case high-frequency noise coupled; e) Make sure signal ground of FB line and IC are connected firstly, then connect to power ground of inductor through a single point.
3. Place VDD capacitor close to the IC to ensure the VDD loop (Loop3) is small.
4. Additional Notes: a) When π filter circuit is added after the bridge, make sure power inductor far away from the π filter inductor; b) Connect the drain pin of KP320X to a large cooper area to improve thermal performance if possible.

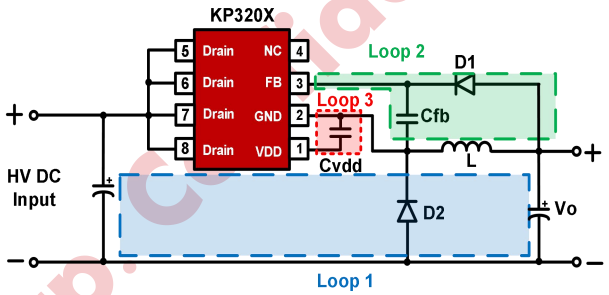
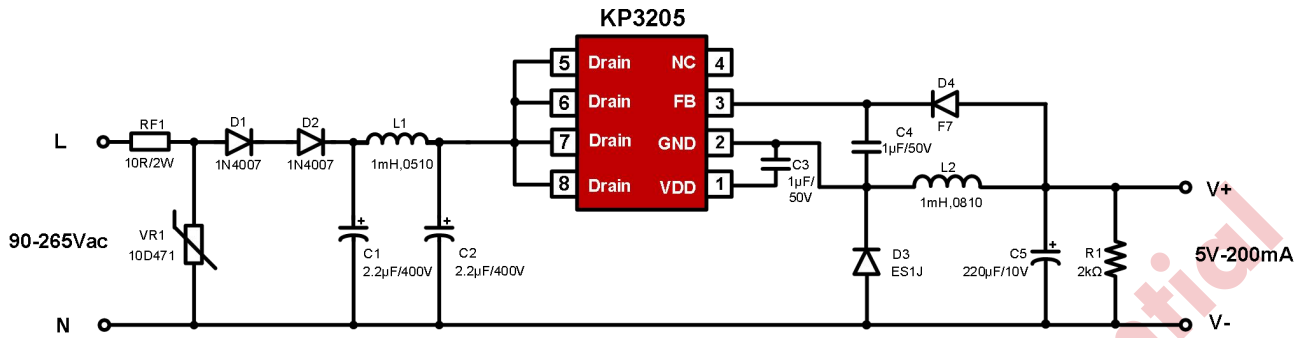


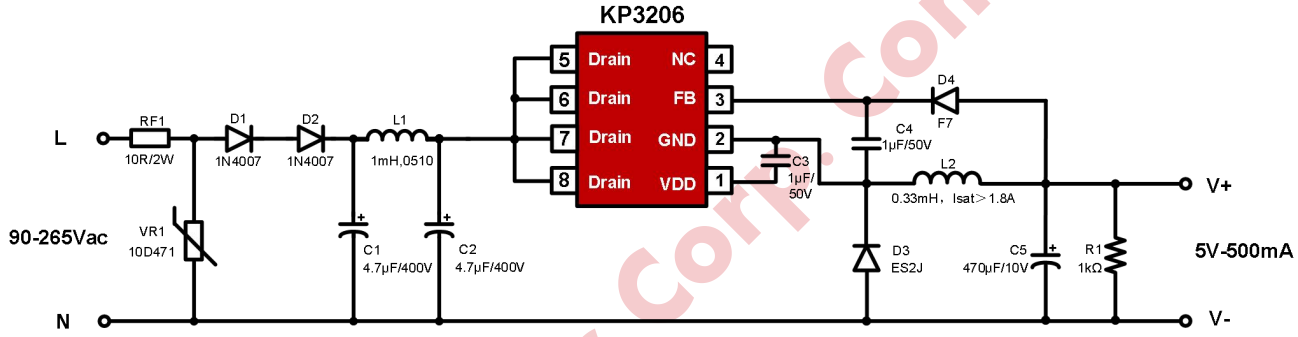
Fig.2

Typical Application Diagram

- **Non-Isolated Buck (5V-200mA, KP3205)**

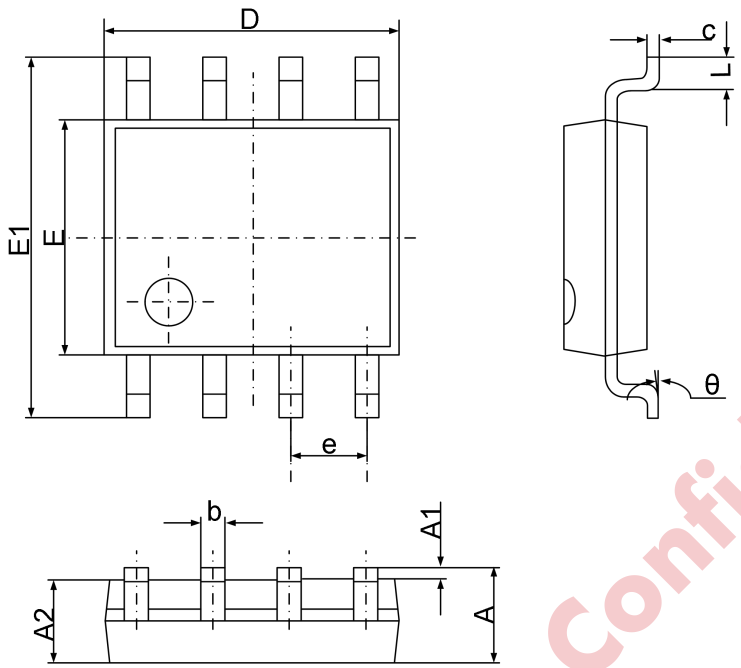


- **Non-Isolated Buck (5V-500mA, KP3206)**



Package Dimension

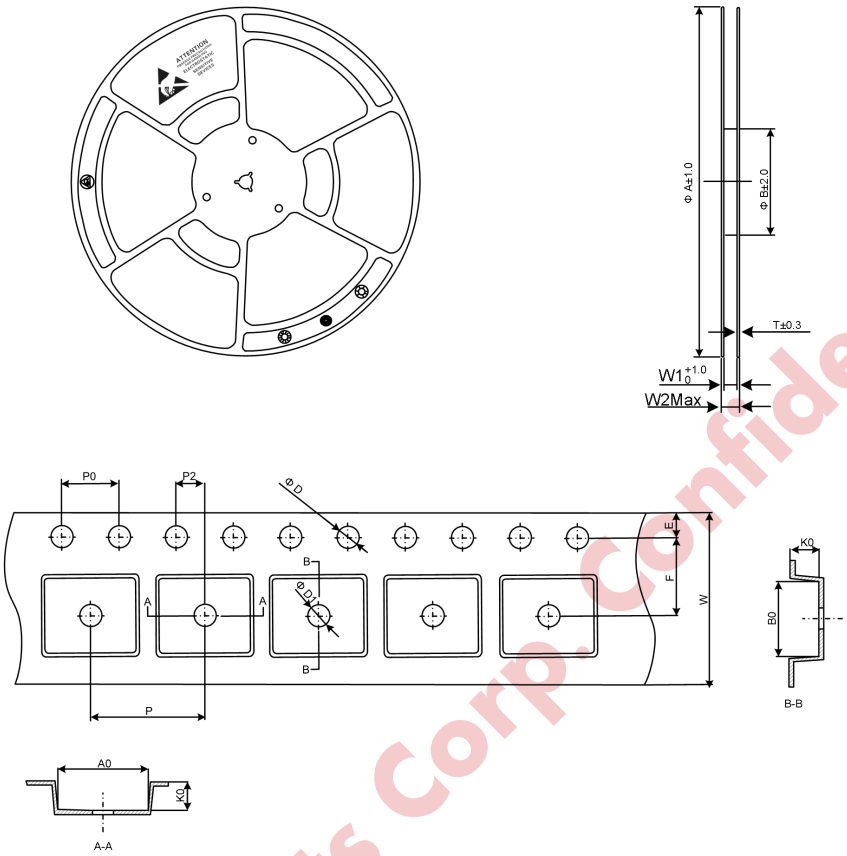
SOP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Tape and Reel Information

SOP-8



Reel Dimensions (mm)				
A	**B (Inner Diameter)**	**W1**	**W2 Max**	**T**
330	100	12.4	18.4	1.5

Tape Dimensions			
Symbol	**Dimensions (mm)**	**Symbol**	**Dimensions (mm)**
E	1.75±0.10	W	12.00±0.10
F	5.50±0.10	P	8.00±0.10
P2	2.00±0.10	A0	6.60±0.10
D	$1.50^{+0.1}_{-0}$	B0	5.30±0.10
D1	1.55±0.05	K0	1.90±0.10
P0	4.00±0.10		

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