High Performance Low Cost Off-line PWM Power Switch

FEATURES

- **Integrated with 700V Power MOSFET and HV Startup Circuit**
- **Multi-Mode Control with Audio Noise Free Operation**
- **Supports Flyback, Buck and Buck-Boost Topologies**
- **Support Ultra-low Input Voltage (>20V)**
- **Less than 100mW Standby Power**
- **Up to 30kHz Maximum Frequency**
- **Good Line and Load Regulation**
- **Built-in Soft Start**
- **Build in Protections:**
  - **Over Load Protection (OLP)**
  - **Cycle-by-Cycle Current Limiting (OCP)**
  - **Output OVP**
  - **On-chip OTP**
- **Available with SOP-8/SOT23-5 Package**

APPLICATIONS

- **Small Home Appliances**

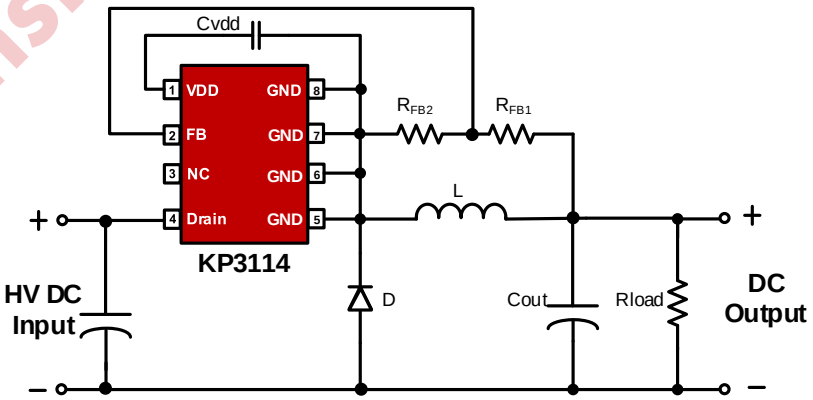
GENERAL DESCRIPTION

KP3114 is a high performance Switch Mode Power Supply Switcher for low power off-line application with minimum components in typical buck solution. This IC has built-in high break down voltage MOSFET to withstand high surge input.

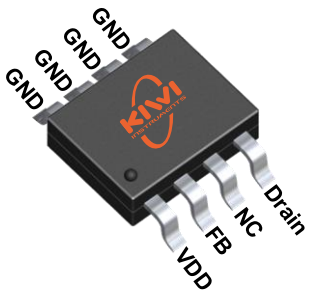
Unlike conventional PWM control, there's no fixed internal clock in KP3114 to trigger the GATE driver, the switching frequency is changed according to the load condition. The multi-mode PWM control is integrated to simplify circuit design and achieve good line and load regulation without audio noise generated. The peak current limit changes according to the real load condition for low standby power in no load.

KP3114 integrates functions and protections of Under Voltage Lockout (UVLO), Cycle-by-cycle Current Limiting (OCP), Output OVP, On-chip Thermal Shutdown, Over Load Protection (OLP) with Auto Recovery Mode Protection, etc.

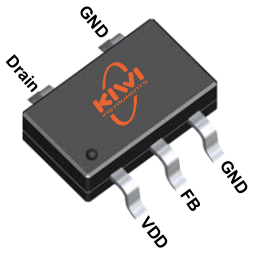
TYPICAL APPLICATION CIRCUIT



Pin Configuration



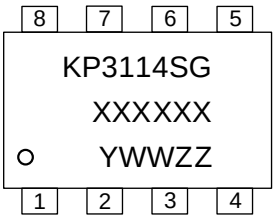
SOP-8



SOT23-5

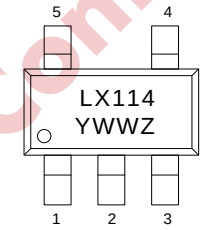
Marking Information

XXXXXX: Wafer Lot Code
Y: Year Code
WW: Working Week, 01-52
ZZ: Serial Number, 01-99 or A0-ZZ



SOP-8

LX114: KP3114
Y: Year Code
WW: Working Week, 01-52
ZZ: Serial Number, 1-9 or A-Z



SOT23-5

Typical Output Power Table

Product	Package	Rdson	Output Voltage (1)	Output Current @85-265Vac，BUCK@85℃(2)
KP3114	SOP-8	20Ω	>2V	Io<250mA
KP3114	SOT23-5	20Ω	>2V	Io<200mA

(1) Default for Buck Converter Application.

(2) The practical output power is determined by the output voltage and thermal conditions.

Pin Description

Pin Number (SOP-8)	Pin Number (SOT23-5)	Pin Name	I/O(3)	Description
1	1	VDD	P	The Power Supply and the Output Voltage Feedback Pin. For the normal Operation, a Capacitor with 1μF is Recommended to Connect to this Pin
2	2	FB	I	Feedback Input
3	/	NC	/	No Connection
4	5	DRAIN	P	The Power MOSFET Drain
5,6,7,8	3,4	GND	G	The Ground Reference for the IC

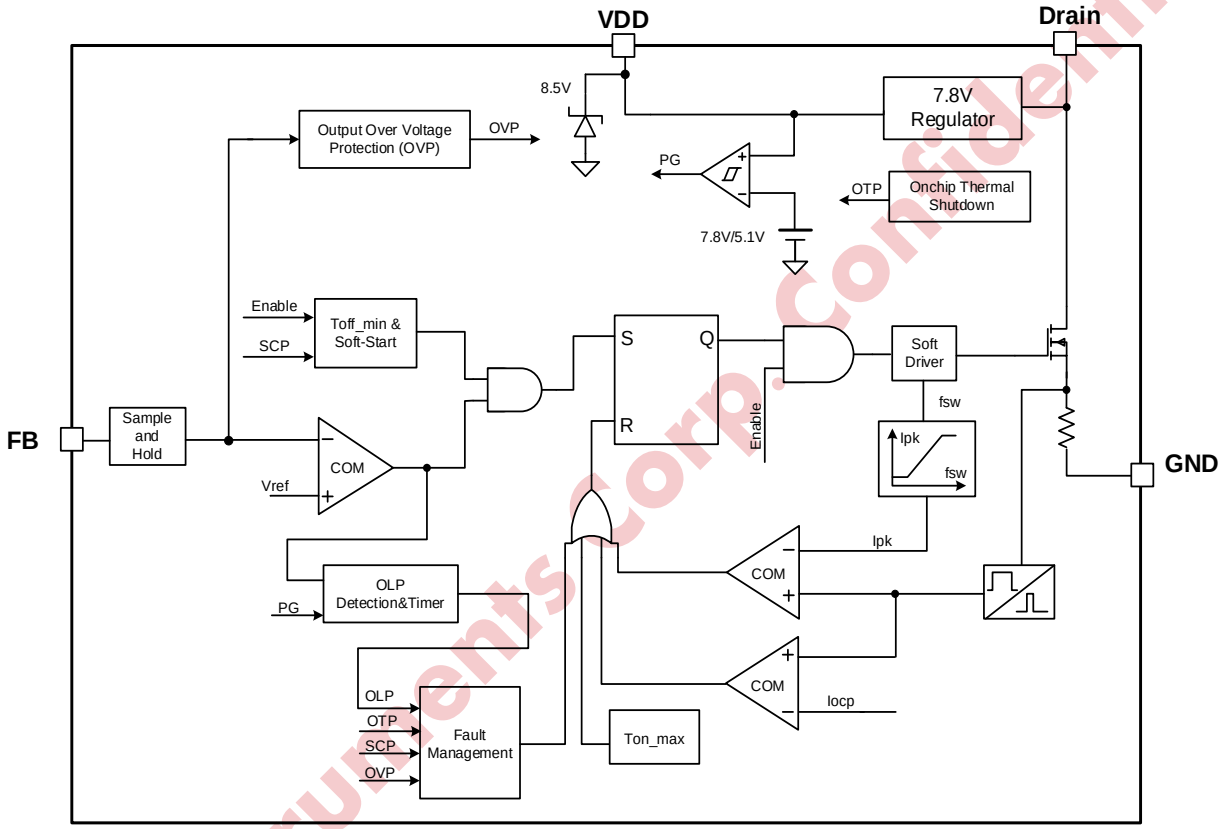
(3) I - Input; P – Power; G - GND.

Ordering Information

Part Number(4)	Description
KP3114SGA	SOP-8, Halogen free in T&R, 4000Pcs/Reel
KP3114LGA	SOT23-5, Halogen free in T&R, 3000 Pcs/Reel

(4) Suffix "A" – Tape & Reel.

Block Diagram



Absolute Maximum Ratings (5)

Parameter	Value	Unit
Drain – GND Voltage Range	-0.3 to 700	V
VDD – GND Voltage Range	-0.3 to 9	V
VDD Pin Clamp Current	10	mA
FB – GND Voltage Range	-0.3 to 9	V
Package Thermal Resistance – Junction to Ambient (SOP-8)	165	˚C/W
Package Thermal Resistance – Junction to Ambient (SOT23-5)	250	˚C/W
Maximum Junction Temperature	160	˚C
Storage Temperature Range	-65 to 150	˚C
Lead Temperature (Soldering, 10sec)	260	˚C
ESD Capability, HBM (Human Body Model) (6)	4000	V
Maximum Internal MOSFET DC Drain Current	0.5	A
Maximum Internal MOSFET Pulse Drain Current (Duration below 100μs)	2	A

(5) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(6) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Recommended Operation Conditions

Parameter	Value	Unit
Operating Junction Temperature	-40 to 125	˚C
Operation Switching Frequency	20 to 30	kHz

Electrical Characteristics (Ta = 25˚C, If Not Otherwise Noted)

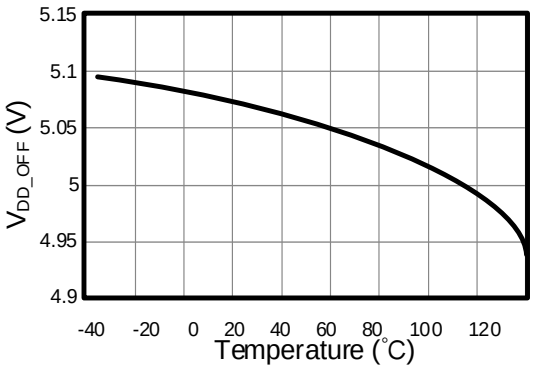
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High Voltage Startup Section (Drain Pin)						
I_{HV1}	HV Charging Current1	Drain=700V, VDD=0V	0.26	0.6	2.1	mA
I_{HV2}	HV Charging Current2	Drain=700V, VDD=4V		5		mA
$I_{HV\_leakage}$	HV Leakage Current	Drain=700V, VDD=8.5V		9	81	μA
V_{BR}	HV MOSFET Breakdown Voltage		700			V

R_{dson}	Static Drain-Source On Resistance		18	20	28	Ω
Supply Voltage Section (VDD Pin)						
V_{DD_ON}	VDD Under Voltage Lockout Exit		7.4	7.8	8.1	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter		3.9	5.1	6.1	V
V_{CLAMP}	VDD Clamp Voltage	I_{CLAMP}=2mA		8.5		V
I_{VDD_Q}	Quiescent Current	No Switching	85	150	260	μA
Feedback Section (FB Pin)						
V_{FB_REF}	Internal Error Amplifier (EA) Reference Input		1.739	1.78	1.811	V
V_{FB_OVP}	Output Over Voltage Protection (Output OVP) Threshold			2.6		V
N_{FB_OVP}	OVP Debounce Cycle			3		
V_{FB_OLP}	Output Over Load Protection (Output OLP) Threshold			1.66		V
T_{D_OLP}	Over Loading Debounce Time			150		ms
Current Sense Section						
T_{LEB}	Leading Edge Blanking Time			380		ns
T_{D_OCP}	Over Current Detection and Control Delay			50		ns
I_{OCP}	Over Current Detection Value		405	420	435	mA
I_{AOCP} /I_{OCP}	AOCP/OCP Ratio			1.33		
Timer Section						
$T_{OFF\_min\_norm}$	Normal Minimum OFF time	Stable state	27	30	35	μs
$T_{OFF\_max\_nom}$	Nominal Maximum OFF Time		1.24	2	2.55	ms
$T_{OFF\_max\_FDR}$	Maximum OFF Time in Fast Dynamic Response Mode			420		μs
T_{ON_max}	Maximum ON Time		26	37	57	μs
T_{ss}	Internal Soft Start Time			3		ms
$T_{Auto\_Recovery}$	Protection Auto Recovery Debounce Time			1.2		s
On-Chip Thermal Shutdown						
T_{SD}	Thermal Shutdown Trigger Point (7)			155		˚C

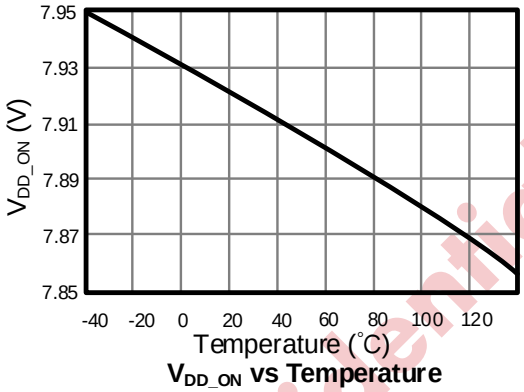
(7) Guaranteed by design.

.

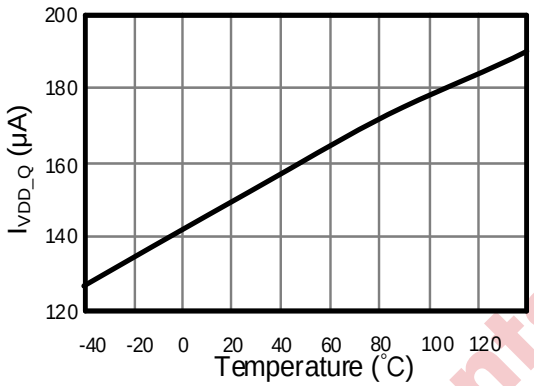
Typical Characteristic



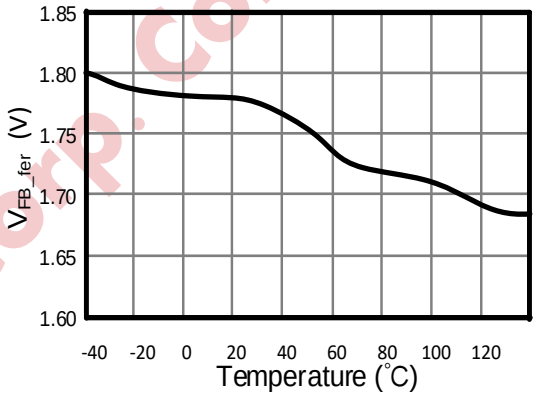
V_{DD_OFF} vs Temperature



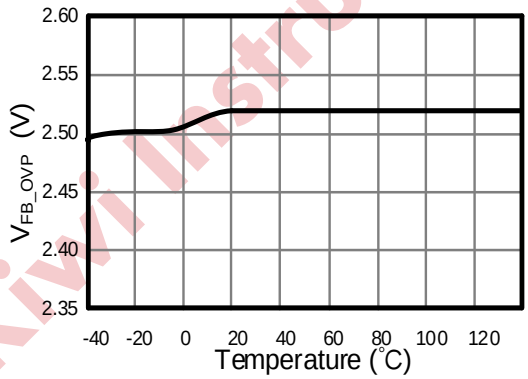
V_{DD_ON} vs Temperature



I_{VDD_Q} (µA) vs Temperature



V_{FB_ref} vs Temperature



V_{FB_OVP} vs Temperature

Operation Description

KP3114 integrates a multi-mode PWM controller with high voltage power MOSFET switch on the IC. It is optimized for off-line non-isolated buck or buck-boost applications in small home appliances and linear regulator replacement. The IC utilizes the multi-mode PWM control to regulate output with high precision and lowest components count.

• Very Low Operation Current

The standby operating current in KP3114 is as small as I_{VDD_Q} (typically 150μA). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

• High Voltage Start-Up Operation

In KP3114, a 700V high voltage startup cell is integrated. During startup, the internal startup circuit is enabled and a HV current source charges the VDD hold up capacitor Cvdd through Drain pin, as shown in “Block Diagram”. When VDD reaches V_{DD_ON} (typically 7.8V), the IC begins switching. The VDD is always charged by the high voltage startup cell in steady state.

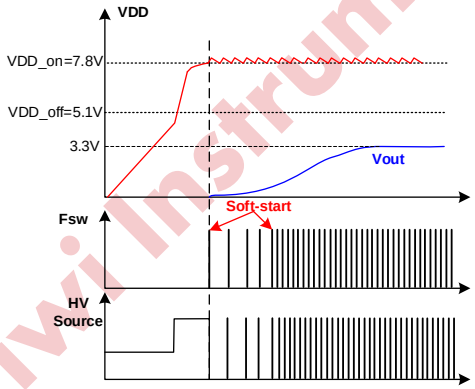


Fig.1

• Constant Voltage Control

During the power MOSFET off period, KP3114 samples the FB pin signal which indicates the output voltage, then using the internal Sample & Hold circuit and constant voltage control circuit to guarantee FB pin voltage meet the internal reference V_{FB_REF} (typically 1.78V). So system can achieve constant output voltage.

Below equation approximately determines the output voltage:

$$\mathrm{Vo} = 1.78V * \frac{\mathrm{Rup} + \mathrm{Rdown}}{\mathrm{Rdown}} - V_F$$

VF---Freewheeling Diode Voltage. This parameter is offset by the forward current in practical application.

R_{down}---Down Divider Resistor. Affected by PCB board material and layout parasitic parameter. Suggest R_{down} value is no more than 30kΩ.

R_{up}---Up Divider Resistor. Limited by MOSFET on-state forward clamp current and ESD reverse clamp capability. Suggest R_{up} value is no less than 30kΩ.

• Current Limit and Leading Edge Blanking

There’s a programmable current limit for current sensing voltage, which is changed according to the system switching frequency. When the sampled voltage exceeds the internal threshold, the power MOSFET is turned off for the remainder of that cycle. An internal leading edge blanking circuit is built in. During this blanking period (typically 380ns), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the GATE driver.

• Multi-Mode PWM Control

To meet the tight requirement of averaged system efficiency and no load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in KP3114 which is shown in the Fig 2.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction.

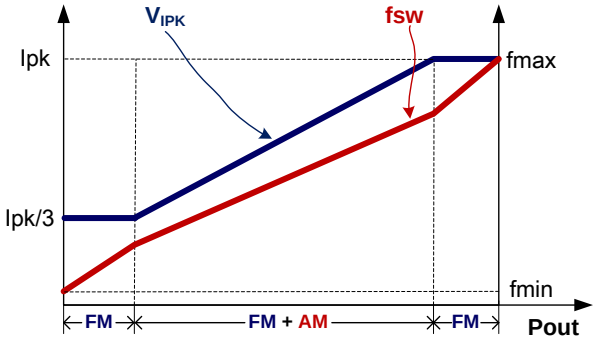


Fig.2

Soft Start

KP3114 features an internal T_{ss} (typically 3ms) soft start that slowly increases the switching frequency (Toff reduce from 100μs to 30μs linearly) during startup sequence. Every restart attempt is followed by the soft start activation.

Output Over Voltage Protection (OVP)

In KP3114, if the sampled FB voltage is larger than V_{FB_OVP} (typically 2.6V) and lasts for seven continuous PWM cycles, the IC will enter into Output Over Voltage Protection (Output OVP) mode, in which auto recovery mode will be followed.

Over Load Protection (OLP) / Short Load Protection (SLP)

If over load or short load condition occurs, the output and the feedback voltage drop down to be lower than V_{FB_OLP} (typically 1.66V). If this fault is present for more than T_{D_OLP} (typically 150ms), the protection will be triggered, the IC will experience an auto-restart mode (as mentioned below).

Abnormal Over Current Protection (AOCP)

When in heavy load or output short condition, the inductor current may be increased too large. To avoid system components damaged, there's a abnormal over current limit (typically 1.33*OCP). When the current sense voltage is larger than this threshold, the internal power MOSFET is turned off immediately and is to be turned on again after 60us.

On Chip Thermal Shutdown

KP3114 integrates thermal shutdown function. When the IC junction temperature is higher than T_{SD} (typically 155˚C) and enters into auto-restart mode (as mentioned below).

Enhanced Dynamic Response

In KP3114, the dynamic response performance is optimized to reduce output drop in load transient.

Audio Noise Free Operation

In KP3114, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

Protections with Auto-Restart

In the event of protections, the IC enters into auto-restart and an internal timer begins counting, wherein the power MOSFET is disabled. When $T_{Auto\_Recovery}$ (typically 1.2s) has been counted, the IC will reset and start up the system again. However, if the fault still exists, the system will experience the above mentioned process.

Soft Totem-Pole Gate Driver

KP3114 has a soft totem-pole gate driver with optimized EMI performance.

Application Information

● PCB Layout Guidelines

PCB layout design has a significant impaction on the performance of power supply，which helps KP3114 to improve system reliability, EMC and thermal performance. Follow below guidelines to optimize performance.

1. The main power loop (Loop1) should be as small as possible, and the trace should be wide for better efficiency performance.
2. Feedback Routing (Loop2): a) Put the feedback loop out of the main power loop，and minimize this loop area as small as possible; b) Do not route FB pin line too long and beneath the IC, or system may not operation normally; c) Put the components of this loop close to IC as much as possible, and far away from the power inductor; d) Place the output feedback point at the positive of the output capacitor, and do not route this line beneath the power inductor or freewheeling diode in case high-frequency noise coupled; e) Make sure signal ground of FB line and IC are connected firstly, then connect to power ground of inductor through a single point.

   Place VDD capacitor close to the IC to ensure the VDD loop (Loop3) is small.
3. Additional Notes: a) When π filter circuit is added after the bridge, make sure power inductor far away from the π filter inductor; b) Connect the GND pin of KP3114 to a large cooper area to improve thermal performance if possible.

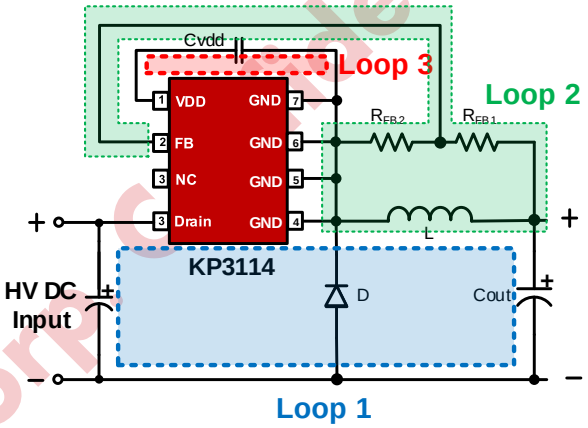
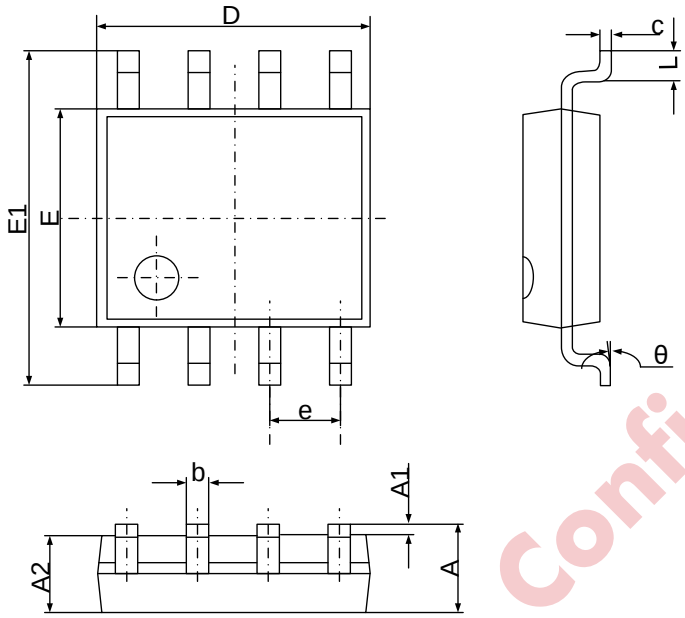


Fig.3

Package Dimension

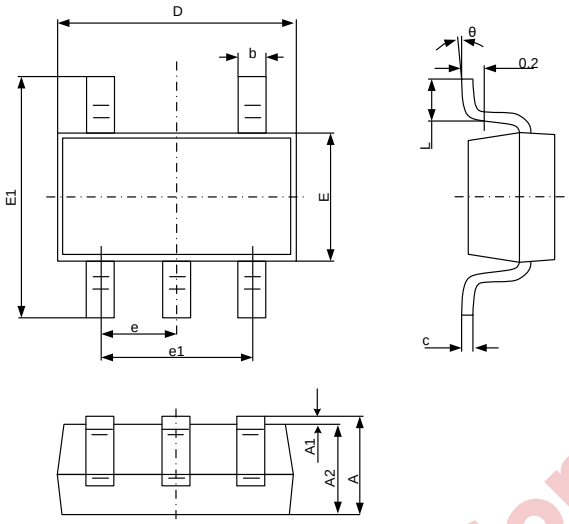
SOP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Dimension

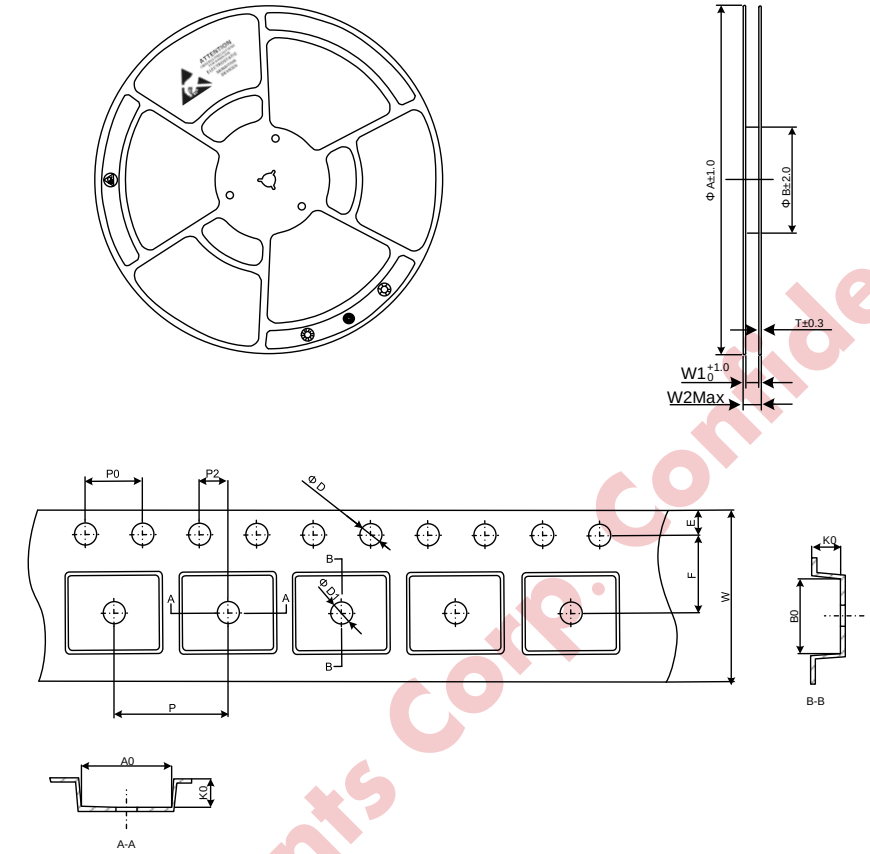
SOT23-5



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	-	1.350	0.035	0.047
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.220	0.004	0.009
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Tape and Reel Information

SOP-8



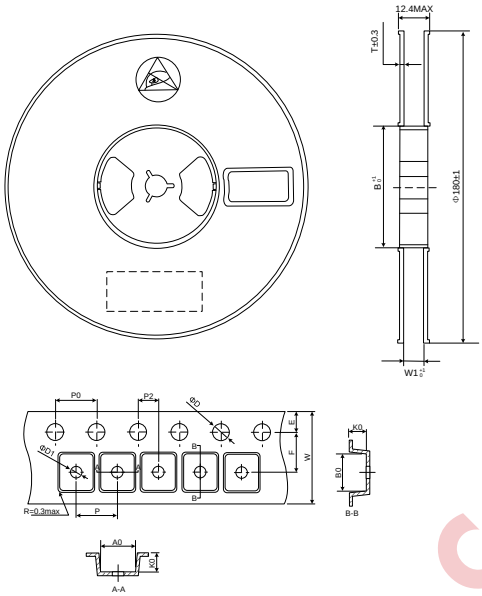
Reel Dimensions (mm)				
A	**B (Inner Diameter)**	**W1**	**W2 Max**	**T**
330	100	12.4	18.4	1.5

Tape Dimensions			
Symbol	**Dimensions (mm)**	**Symbol**	**Dimensions (mm)**
E	1.75±0.10	W	12.00±0.10
F	5.50±0.10	P	8.00±0.10
P2	2.00±0.10	A0	6.60±0.10
D	$1.50^{+0.1}_{-0}$	B0	5.30±0.10
D1	1.55±0.05	K0	1.90±0.10
P0	4.00±0.10		

Packing Quantity				
Package	**Pcs/Reel**	**Reels/Box**	**Boxes/Carton**	**Pcs/Carton**
SOP-8	4000	2	8	64000

Tape and Reel Information

SOT23-5



Reel Dimensions (mm)		
B	**W1**	**T**
54.4	8.6	1.5

Tape Dimensions			
Symbol	**Dimensions (mm)**	**Symbol**	**Dimensions (mm)**
E	1.75±0.10	W	8.00±0.10
F	3.50±0.05	P	4.00±0.10
P2	2.00±0.05	A0	3.26±0.10
D	1.55±0.05	B0	3.30±0.10
D1	1.0 Min	K0	1.05±0.10
P0	4.00±0.10		

Packing Quantity				
Package	**Pcs/Reel**	**Reels/Box**	**Boxes/Carton**	**Pcs/Carton**
SOT23-5	3000	10	4	120000

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