

### BF7515CM44-LJTXSPEC V1.3

Home appliance 8-bit general-purpose MCU

## 1. BF7515CM44-LJTX MCU General Description

#### 1.1. Features

Ø Core: 1T 8051

Operating frequency: 12MHz, 8MHz, 4MHz, 1MHz

o Clock error:  $\pm 1\%$  @ -20°C $\sim 65$  °C, 5V

 $\pm 3\%$  @ -40°C ~105°C, 5V

Ø Memory (FLASH)

o CODE: 63K Bytes

o DATA: 1K Bytes +2\*512 Bytes

o SRAM: 256 Bytes(data)+4K Bytes(xdata)

o Support 2K/4K/8K BOOT function area

O Clock Source, Reset and Power Management

o Internal low-speed clock LIRC: 32kHz,

Clock error:  $\pm 25\%$ @ 25°C, ,5 $\pm 3^{5}\%$  @ -40°C ~1 05°C,

o Internal high-speed RC oscillator: 1MHz

o External crystal oscillator: 32768Hz/4MHz

o 8 resets, brown-out reset voltage (Bor):

2.3V/2.8V/3.3V/3.7V/4.2V

o Low voltage detection: 2.7V/3.0V/3.3V/3.6V/3.8V/

4.0V/4.2V/4.4V

Ø IC

o Both support built-in pull-up resistor 35k

o High current sink port (PB0~PB7)

o Support IO function remapping

o Support external interrupt function, INT0~3 (rise-edge, falling-edge, double-edge) and INT4(rise-edge, falling-edge) share

interrupt source

Communication Module

o 3\*UART Communication Module

o 1\*IIC slave mode, support 100/400kHz

o 1\*SPI, support up to 2MHz communication

Ø 16-Bit PWM

 PWM0 supports 5 channels, the same period and duty cycle, configurable polarity

2 1 3

o PWM1 supports 5 channels, the same period and duty cycle,

configurable polarity

o PWM2 supports 1 channel output

PWM3 supports 1 channel output

**Ø** Operating Voltage: 2.7V ~ 5.5V

Operating Temperature: -40°C 1 ~0 5°C

o Enhanced industrial grade, in line with JESD industrial grade

reliability certification standards

12-bit High-precision ADCUp to 42 analog input channels

o Reference voltage: VCC/2V/4V

Ø Interrupt

o Two-level interrupt priority selectable

o ADC, LED, LCD, INT0/1/2/3/4,LVDT,Timer0~3, WDT,

UART0/1/2, IIC, PWM0/1, SPI Interrupt

5 🛭 Timer

o 16-bit Timer0/1/3, 32-bit Timer2

o Timer2 clock source: LIRC32k, XTAL32768Hz/4MHz

o Watchdog timer, overflow time 18ms to 2.304s

Ø LED Driver

o Support 4x5, 5x6, 6x7, 7x8 dot matrix driver

o LED0~LED7 scan order can be configured

o Row and column matrix drive: duty cycle 1/8~8/8

o LED drive matrix: max 8COM x 8SEG

Ø LCD Driver

o 4 COM x 28 SEG (1/4 duty cycle, 1/3 bias)

o 5 COM x 27 SEG (1/5 duty cycle, 1/3 bias)

o 6 COM x 26 SEG (1/6 duty cycle, 1/3 or 1/4 bias)

o 8 COM x 24 SEG (1/8 duty cycle, 1/4 bias)

Low power management

o Idle mode 0 and Idle mode 1

Idle mode 1, po wer con sum pti on 1

Two-wire programming and single-wire debugging

Package

o LOFP44

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#### 1.2. Overview

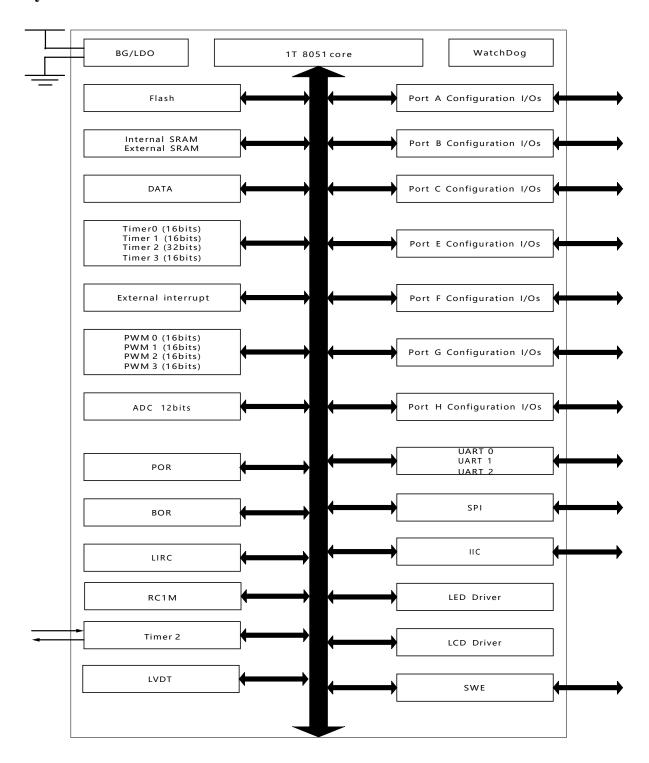
The BF7515CM44-LJTX uses the high speed 8051 core with 1T instruction cycle, based on standard 8051 instruction pipeline structure. Compared to the standard 8051 (12T) instruction cycle, it has the quicker running speed, compatibility standard 8051 instruction.

The BF7515CM44-LJTX includes external watchdog, LED serial dot matrix driver, LCD display driver, IIC, UART, SPI, low voltage detection, power-down reset, 4 independent 16bit PWM modules, Timer0, Timer1, Timer2, Timer3, 12bit successive approximation ADC, low power management, etc.

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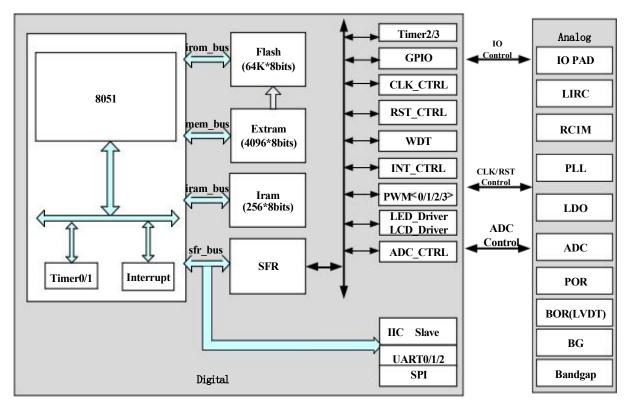


## 1.3. System Architecture



System architecture

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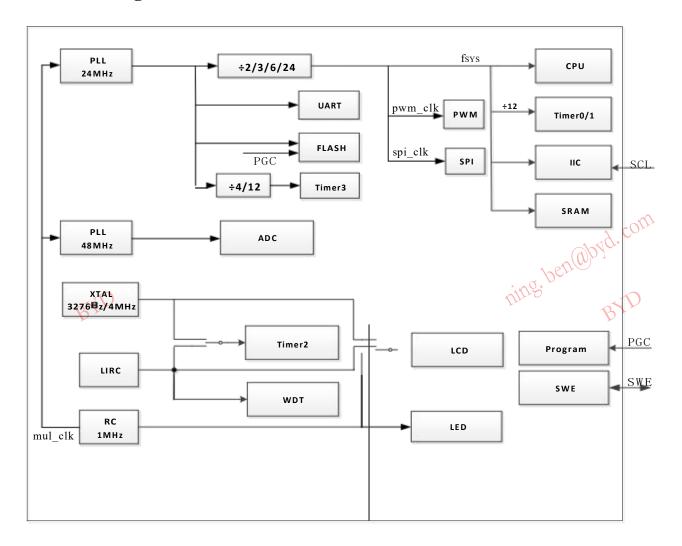


System bus frame diagram

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## 1.4. Clock Diagram



Clock block diagram

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## 1.5. Selection List

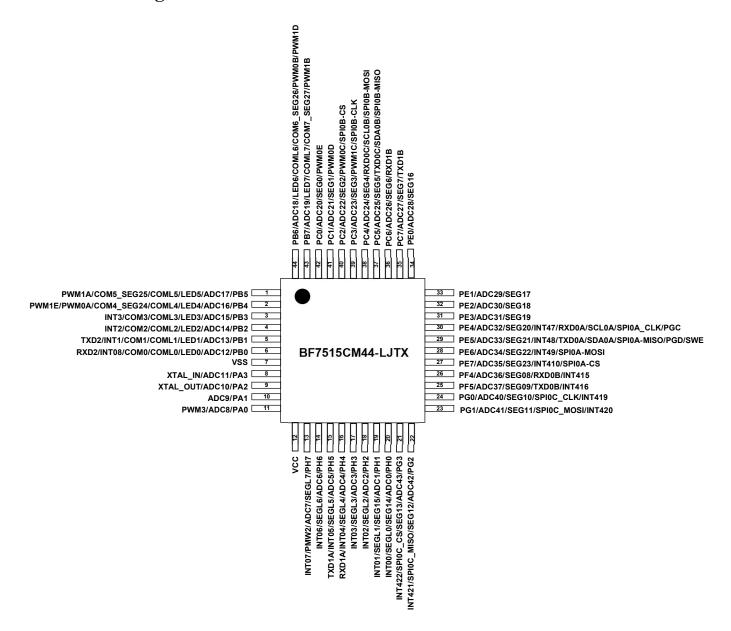
Ty	ype	BF7515CM44-LJTX
Opera	tion voltage (V)	2.7~5.5
Operating from	equency (Hz)	12M
C	ore	1T 8051
	CODE	63/61/59/55K
Manager (Dartes)	BOOT	0/2/4/8K
Memory (Bytes)	DATA	1K +2*512
	SRAM	256 +4K
	WDT	1
	Timer0*16bit	1
Timer	Timer1*16bit	1
	Timer2*32bit	1
	Timer3*16bit	1
	IIC	1
Communication module	UART	3
	SPI	1
Analog module	ADC*12 bit	42
GI	PIO	42
CC	OM	8
I	NT	22
	LED serial	7*8
Display module	LED ranks	8COM*8SEG
	LCD	8COM*24SEG
	PWM0*16bit	5
DWD ( 1.1	PWM1*16bit	5
PWM module	PWM2*16bit	1
	PWM3*16bit	1
Pac	kage	LQFP44(10mm*10mm, e=0.8mm)

Selection List

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### 1.6. Pin Assignment



BF7515CM44-LJTX LQFP44 Package pin diagram

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# 1.7. Pin Description

BF7515CM44-LJTX	Function description
1	Default function: GPIO <pb5> Other function: ADC17: ADC channel</pb5>
2	Default function: GPIO <pb4> Other function: ADC16: ADC channel</pb4>
3	Default function: GPIO <pb3> Other function: ADC15: ADC channel</pb3>
4	Default function: GPIO <pb2> Other function: ADC14: ADC channel</pb2>
5	Default function: GPIO <pb1> Other function: ADC13: ADC channel</pb1>
6	Default function: GPIO <pb0> Other function: ADC12: ADC channel</pb0>

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16:20.3	DVD2. Social post receiving
	RXD2: Serial port receiving
7	Default function: GND <vss></vss>
	Default function: GPIO <pa3></pa3>
8	Other function: ADC11: ADC channel
	XTAL_IN: External crystal oscillator input
	Default function: GPIO <pa2></pa2>
9	Other function: ADC10: ADC channel XTAL OUT: External crystal oscillator output
	Default function: GPIO <pa1></pa1>
10	Other function: ADC9: ADC channel
	Default function: GPIO <pa0></pa0>
11	Other function: ADC8: ADC channel
	PWM3: PWM3 output port
12	Default function: power supply <vcc></vcc>
	Default function: GPIO <ph7></ph7>
	Other function: SEGL7: SEG of LED column matrix
13	ADC7: ADC channel
	PWM2: PWM2 output port
	INT07: External Interrupt
	Default function: GPIO <ph6></ph6>
14	Other function: SEGL6: SEG of LED column matrix
14	ADC6: ADC channel
	INT06: External Interrupt
	Default function: GPIO <ph5></ph5>
	Other function: SEGL5: SEG of LED column matrix
15	ADC5: ADC channel
	INT05: External Interrupt
	TXD1A: Serial port transmission
	Default function: GPIO <ph4></ph4>
	Other function: SEGL4: SEG of LED column matrix
16	ADC4: ADC channel
	INT04: External Interrupt
	RXD1A: Serial port receiving
	Default function: GPIO <ph3></ph3>
17	Other function: SEGL3: SEG of LED column matrix
	ADC3: ADC channel
	INT03: External Interrupt
	Default function: GPIO <ph2></ph2>
18	Other function: SEGL2: SEG of LED column matrix
	ADC2: ADC channel INT02: External Interrupt
	INTOZ. External interrupt

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(36.5)	)
19 19	Default function: GPIO <ph1></ph1>
05-01-0	Other function: SEGL1: SEG of LED column matrix
19	ADC1: ADC channel
	SEG15: SEG ofLCD
	INT01: External Interrupt
	Default function: GPIO <ph0></ph0>
	Other function: SEGL0: SEG of LED column matrix
20	ADC0: ADC channel
	SEG14: SEG ofLCD
	INT00: External Interrupt
	Default function: GPIO <pg3></pg3>
	Other function: ADC43: ADC channel
21	SEG13: SEG ofLCD
	SPI0C_CS: SPI chip select signal
	INT422: External Interrupt
	Default function: GPIO <pg2></pg2>
	Other function: ADC42: ADC channel
22	SEG12: SEG ofLCD
	SPI0C_MISO: SPI master data input
	INT421: External Interrupt
	Default function: GPIO <pg1></pg1>
	Other function: ADC41: ADC channel
23	SEG11: SEG ofLCD
	SPIOC_MOSI: SPI master data output
	INT420: External Interrupt
	Default function: GPIO <pg0></pg0>
	Other function: ADC41: ADC channel
24	SEG10: SEG ofLCD
	SPIOC_CLK: SPI clock
	INT419: External Interrupt
	Default function: GPIO <pf5></pf5>
	Other function: ADC37: ADC channel
25	SEG09: SEG ofLCD
	TXD0B: Serial port transmission
	INT416: External Interrupt
	Default function: GPIO <pf4></pf4>
	Other function: ADC36: ADC channel
26	SEG08: SEG ofLCD
	RXD0B: Serial port receiving
	INT415: External Interrupt

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6.58	.53
2 11 10.3	Default function: GPIO <pe7></pe7>
25-01-0	Other function: ADC35: ADC channel
27	SEG23: SEG ofLCD
	INT410: External Interrupt
	SPI0A_CS: SPI chip select signal
	Default function: GPIO <pe6></pe6>
	Other function: ADC34: ADC channel
28	SEG22: SEG ofLCD
	INT49: External Interrupt
	SPI0A_MOSI: SPI master data output
	Default function: GPIO <pe5></pe5>
	Other function: ADC33: ADC channel
	SEG21: SEG ofLCD
	INT48: External Interrupt
29	TXD0A: Serial port transmission
	PGD: Programming port PGD
	SDA0A: Serial data line ofIIC
	SWE: Single-line simulation
	SPI0A MISO: SPI master data input
	Default function: GPIO <pe4></pe4>
	Other function: ADC32: ADC channel
	SEG20: SEG ofLCD
	INT47: External Interrupt
30	RXD0A: Serial port receiving
	PGC: Programming port PGC
	SCL0A: Serial clock line of IIC
	SPI0A CLK: SPI clock
	Default function: GPIO <pe3></pe3>
31	Other function: ADC31: ADC channel
31	SEG19: SEG ofLCD
22	Default function: GPIO <pe2></pe2>
32	Other function: ADC30: ADC channel
	SEG18: SEG ofLCD
	Default function: GPIO <pe1></pe1>
33	Other function: ADC29: ADC channel
	SEG17: SEG ofLCD
	Default function: GPIO <pe0></pe0>
34	Other function: ADC28: ADC channel
	SEG16: SEG ofLCD
35	Default function: GPIO <pc7></pc7>
33	Other function: ADC27: ADC channel

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16.58	$\frac{1}{2}$
025-07-01-76:58	SEG7: SEG ofLCD
m5-01	TXD1B: Serial port transmission
N L	Default function. Of 10 4 Co
36	Other function: ADC26: ADC channel
	SEG6: SEG of LCD
	RXD1B: Serial port receiving
	Default function: GPIO <pc5></pc5>
	Other function: ADC25: ADC channel
37	SEG5: SEG of LCD TXD0C: Serial port transmission
	SDA0B: Serial data line of IIC
	SPI0B MISO: SPI master data input
	Default function: GPIO <pc4></pc4>
	Other function: ADC24: ADC channel
	SEG4: SEG ofLCD
38	RXD0C: Serial port receiving
	SCL0B: Serial clock line ofIIC
	SPI0B_MOSI: SPI master data output
	Default function: GPIO <pc3></pc3>
	Other function: ADC23: ADC channel
39	SEG3: SEG ofLCD
	PWMXX: PWM output port
	SPI0B_CLK: SPI clock
	Default function: GPIO <pc2></pc2>
40	Other function: ADC22: ADC channel
40	SEG2: SEG of LCD PWM0C: PWM output port
	SPI0B CS: SPI chip select signal
	Default function: GPIO <pc1></pc1>
	Other function: ADC21: ADC channel
41	SEG1: SEG ofLCD
	PWM0D: PWM output port
	Default function: GPIO <pc0></pc0>
	Other function: ADC20: ADC channel
42	SEG0: SEG ofLCD
	PWM0E: PWM output port
	Default function: GPIO <pb7></pb7>
	Other function: ADC19: ADC channel
43	LED7: LED serial dot matrix
	COML7: COM of LCD can be shared as SEG
	COM7_SEG27: COM of LCD can be shared as SEG

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(.50.33	
1/0.30	PWM1B: PWM output port
02-01-0	Default function: GPIO <pb6></pb6>
	Other function: ADC18: ADC channel
	LED6: LED serial dot matrix
44	COML6: COM of LCD can be shared as SEG
	COM6_SEG26: COM of LCD can be shared as SEG
	PWM0B: PWM output port
	PWM1D: PWM output port

Package pin correspondence diagram

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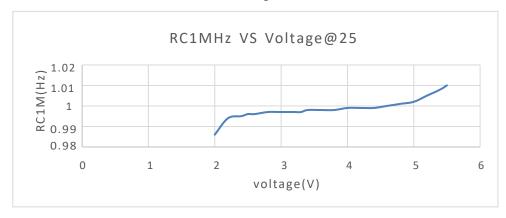


## 2. Electrical Characteristics

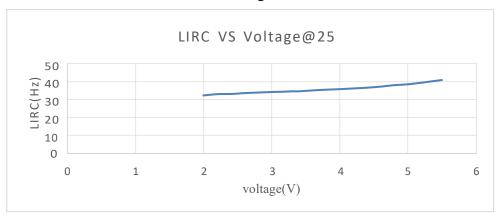
### 2.1. AC Characteristics

D .	Symbol	Cor	nditions	Min	Т	M	<b>T</b> T •	
Parameter		VCC	Temperature	Min	Тур	Max	Unit	
		537	-20 °C~65	-1%	1	+1%		
	Internal high-speed	5V	-40°C ~105°C	-3%	1	+3%	) MII	
frcim	RC oscillator		25°C	-1%	1	+1%	MHz	
		2.7V~5.5V	-40°C ~105°C	-3%	1	+3%		
	System clock	537	-20 °C~65	-1%	12/8/4/1	+1%	MHz	
		5V	-40°C ~105°C	-3%	12/8/4/1	+3%		
fsys		2.7V~5.5V	25°C	-1%	12/8/4/1	+1%		
			-40°C ~105°C	-3%	12/8/4/1	+3%		
$ m f_{LIRC}$		<b>53</b> /	25°C	-25%	32	+25%		
	Internal low-speed	5V	-40°C ~105°C	-35%	32	+35%	kHz	
	RC oscillator	2.7V~5.5V	25°C	-35%	32	+35%		

AC characteristic parameter table

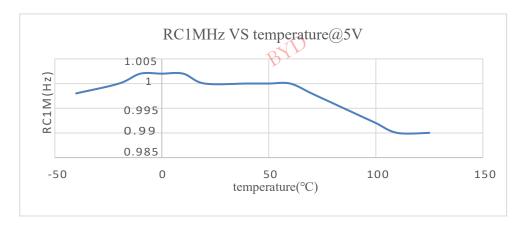


 $f_{RC1M}$  voltage curve

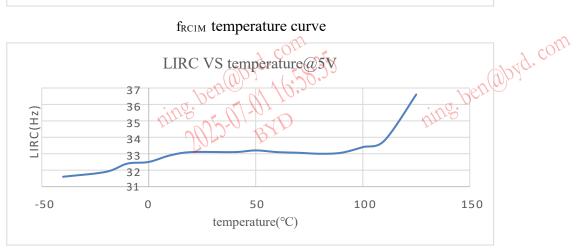


 $f_{LIRC}$  voltage curve

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#### $f_{RC1M}$ temperature curve



 $f_{\text{LIRC}}$  temperature curve

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# 2.2. DC Characteristics

Ta=25°C

_		Test Conditions			_	Ta		
Parameter	Symbol	VCC	Conditions	Min	Тур	Max	Unit	
VCC	Operating Voltage	-	-	2.7	-	5.5	V	
		3.3V	frcim/ PLL on, fsys =12MHz, f <sub>LIRC</sub> on, no	-	2.6	3.4		
		5V	load, all peripherals off	-	2.7	3.5		
		3.3V	f <sub>RC1M</sub> / PLL on, f <sub>SYS</sub> =8	-	2.3	3.0		
	Active mode	5V	MHz, f <sub>LIRC</sub> on, no load, all peripherals off	-	2.4	3.1		
Іор	current	3.3V	f <sub>RC1M</sub> / PLL on, f <sub>SYS</sub> =4 MHz, f <sub>LIRC</sub> on, no load,	-	2.0	2.5	mA	
		5V	all peripherals off	-	2.0	2.6		
		3.3V	f <sub>RC1M</sub> / PLL on, f <sub>SYS</sub> =1	-	1.6	2.1		
		5V	MHz, f <sub>LIRC</sub> on, no load, all peripherals off	-	1.7	2.2		
I <sub>STB0</sub>	idle mode 0 current	3.3V	f <sub>RC1M</sub> / PLL on, f <sub>SYS</sub> off,	-	1.5	2.1	mA	
		5V	flire on, all peripherals off	-	1.6	2.0		
	idle mode 1 current	3.3V	frcim/ PLL/ fsys off, flire	-	14	18.2	μΑ	
I <sub>STB1</sub>		5V	on, all peripherals off	-	12	15.6		
	Average current for intermittent wake-up from idle mode 1	3.3V nin	WDT_CTRL=7, WDT interrupt 2s wake up, 2ms-working time, IO	-	16.4	21.3	μΑ	
		5V	output is low, close other functions	-	15	19	•	
I <sub>STB2</sub>		3.3V	Timer2 external crystal oscillator wakes up in 2s, 2ms working time,	-	16.4	21.3		
		5V	IO output is low, and other functions are closed	-	15	19	μΑ	
V <sub>IL</sub>	Input low level	2.7~5.5V	-	-	-	0.3*VCC	V	
V <sub>IH</sub>	Input high level	2.7~5.5V	-	0.7*VCC	-	-	V	
Vintl	INT input low level	2.7~5.5V	-	-	-	0.3*VCC	V	

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VINTH	INT input high level	2.7~5.5V	-	0.7*VCC	ı	-	V
Vol	output low voltage	5V	I <sub>OL</sub> =68mA	-	1	0.1*VCC	V
Vон	output high voltage	5V	I <sub>OH</sub> =16mA	0.9*VCC	-	-	V
I <sub>OL</sub>	IO sink current	5V	V <sub>OL</sub> =0.1VCC	48	68	88	mA
Іон	IO Source current	5V	V <sub>OH</sub> =0.9VCC	11	16	20	mA
Ісом	PB large sink current	5V	V <sub>OL</sub> =0.1VCC	-	130	-	mA
I <sub>Leak</sub>	Input leakage current	5V	-	-	1	5	μΑ
R <sub>PH</sub>	IO internal pull-up	5V	-	25	35	46	kΩ

The working current of the module is shown in the table below:

D.	G 1 1	Test Conditions			Тур	Max	Unit
Parameter	Symbol	VCC	VCC Conditions				
I <sub>BOR</sub>	BOR operating current	5V	In idle mode 1, no load, BOR enabled		4. 9	-	μΑ
I <sub>LVDT</sub>	LVDT operating current	5V	In idle mode 1, no load, LVDT enabled, voltage selection 3.8V	-	4.8	-	μΑ
IADC	ADC operating current	5V	fsys=12MHz, no load, ADC enable, open a channel, GET_ADC scan, other peripherals off	-	2.1	-	mA
$I_{PWM}$	PWM operating current	5V	fsys=12MHz, no load, PWM0 is enabled, other peripherals off	-	0.5	-	mA
I <sub>ERASE</sub>	Page erase Current	5V	No load, enable NVR3, only NVR3 is erased in while, other peripherals off		2.1	-	mA
Iprog	Programming current	5V	No load, enable NVR3, write only one byte in while, other peripherals off		2.9	-	mA

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# 2.3. ADC Characteristics

Ta=25°C

			<b>Test Conditions</b>			Max	14 23 0
Parameter	Symbol	VCC	Conditions	Min	Тур		Unit
$V_{ADC}$	Supply Voltage	_	-	2.7	_	5.5	V
$N_R$	Accuracy	_	-	_	9	10	Bit
V <sub>ADCI</sub>	ADC Input voltage	_	_	VSS	_	V <sub>REF</sub>	V
_	. D.C.I		No RC filtering	1.2	3.2	17.5	1.0
Radci	ADC Input resistance	5V	RC filtering	10	14.2	31.5	$k\Omega$
IADC	ADC operating current	5V	f <sub>SYS</sub> =12MHz, enable ADC, open a channel	-	2.1	-	mA
Iadci	input current	_	-	_	-	1	μΑ
DNL	Differential nonlinear error	5V	-	-	±4	±6	LSB
INL	Integral nonlinear error	5V	-	_	±4	±6	LSB
t1	ADC sampling time	_	-	0.5	-	_	μs
tadc	ADC conversion time	_	-	2.875	-	_	μs
RESO	Resolution	_	-		12		Bit
N <sub>ADC</sub>	Input channel			_	-	42	Channel

ADC characteristic parameter table

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#### 2.4. Limit Parameters

D .	G 1.1	Test	Conditions	Min	Т	M	<b>T</b> T •		
Parameter	Symbol	VCC	Conditions	Min	Тур	Max	Unit		
VCC	Supply voltage when working	-	_	VSS+2.7	-	VSS+5.5	V		
Tstg	Non-working storage temperature	-	-	-40	-	125	°C		
Ta	Operating temperature	-	_	-40	-	105	°C		
Vin	I/O input voltage	-	_	VSS-0.5	-	VCC+0.5	V		
Ivcc	Power supply VCC current	-	-		130		mA		
Ivss	Ground VSS current	-	-		130		mA		
Iola	IOL total current	-	-		130				
I <sub>OHA</sub>	IOH total current	-	-130						
ESD(HBM)	Port electrostatic discharge voltage	-	-	-8	-	8	kV		

Limit parameters characteristics parameters table

Notes: Exceed the limit parameters may cause damage to the chip, unable to expect the chip work outside the above indicated range. If you work under conditions outside the marked range for a long time, it may affect the reliability of the chip.

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## 3. Memory and SFR

### 3.1. Memory

FLASH main features:

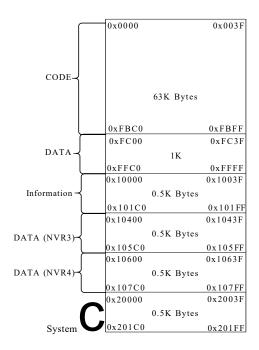
- CODE area: ICP programming supports block erasing, page erasing and byte writing
- DATA area: page erasing and byte writing
- Program/erase time: CODE area: at least 20000 times@25

DATA area: at least 20000 times@25

Data retention period: 100 years@25°C

10 years@85°C

IAP BOOT upgrade function, storage protection, 2K/4K/8K BOOT function area



Flash Storage Architecture

Module	Size (Bytes)	Address	Page
CODE	63K	0x0000~0xFFFF	126
DATA	1K	0xFC00~0xFFFF	1
Information	512	0x10000~0x101FF	1
NVR3	512	0x10400~0x105FF	1
NVR4	512	0x10600~0x107FF	1
System	512	0x20000~0x201FF	1

Address allocation table

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#### 3.1.1. Information and System

The main function of the information block is to store configuration words. The configuration word CFG\_11 is stored in the system block. There are two ways to read the configuration word of BF7515CMXX-LJTX.

#### Method 1: Read steps

- 1. Turn off the interrupt;
- 2. Configure SPROG CMD = 0x88;
- 3. Configure SPROG\_ADDR\_L, SPROG\_ADDR\_H, Select the address to be read;
- 4. Read SPROG RDATA data;
- 5. Need to continue to read data, jump to step 2 and 3;
- 6. After reading SPROG RDATA data, Configure SPROG CMD = 0x00;
- 7. Configure SPROG\_ADDR\_L=0x00, SPROG\_ADDR\_H=0x00; Restore interrupt settings.

#### Method 2: Read steps

- 1. Turn off the interrupt;
- 2. Configure the secondary bus address;
- 3. Read data;
- 4. Need to continue to read data, skip to step 2 and 3;
- 5. Restore interrupt settings.

 $\{SPROG\_ADDR\_H\ SPROG\_ADDR\_L\}\$ The logical address  $(0x4000+(0\sim511))\$ corresponds to the physical address  $(0x10000\sim0x101FF)$ 

 $\{SPROG\_ADDR\_H SPROG\_ADDR\_L\}$  The logical address  $(0x8000+(0\sim511))$  corresponds to the physical address  $(0x20000\sim0x201FF)$ 

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#### 3.1.2. Unique Identification Code

Steps to read the unique identification code (UID) of the chip:

- 1. Off the interrupt;
- 2. Configure SPROG CMD = 0x88;
- 3. Configure SPROG\_ADDR\_L, SPROG\_ADDR\_H, select the address to be read, 0x41A8~0x41B7 corresponds to product ID1~ID16;
- 4. Read SPROG\_RDATA data;
- 5. Need to continue to read data, jump to step 2 and 3;
- 6. After reading SPROG RDATA data, configure SPROG CMD = 0x00;
- 7. corresponds SPROG\_ADDR\_L=0x00, SPROG\_ADDR\_H=0x00; restore interrupt settings.

#### 3.1.3. Registers

Address	Name	RW	Reset	Description
0xCE	SPROG_ADDR_H	RW	0000_0000Ь	Address control register
0xCF	SPROG ADDR L	RW	0000_0000b	Address control register low 8 bits
0xD2	SPROG_CMD	RW	0000_0000b	Command register
0xD4	SPROG_RDATA	R	0000_0000Ь	Information block/system block data read register

SPROG ADDR H (CEH) Address control register

Bit number	7	6	5	4	3	2	1	0		
Symbol	_									
R/W		R/W								
Reset value		0								

Bit number	Bit symbol	Description
		The system and information modules use bits[7:6] and bit0 of this register Bit[7:6]: block selection when reading data indirectly 10: Select system block, multiplexed to read data indirectly
7~0		01: Select information block, multiplexed to read data indirectly
		11/00: reserved;
		{SPROG_ADDR_H[0], SPROG_ADDR_L[7:0]} address system and information address configuration

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SPROG ADDR L(CFH) Address control register low 8 bits

Bit number	- 7	6	01005	3	2	ning 1 0
Symbol			SPROG_AI	DDR_L[7:	[0]	Mrs Br
R/W			R/	W		
Reset value				)		

Bit number	Bit symbol	Description
7~0	SPROG_ADDR_L[7:0]	The lower 8 bits of the address

SPROG CMD(D2H) Command register

Bit number	7	6	5	4	3	2	1	0		
Symbol	20			com	<u> </u>			com		
R/W	6.32		and RAW							
Reset value	20.2		Den (1) 10.00.							
6. 1.0			sing of Mall							

Bit number	Bit symbol	72	10	12.	B	1,	<i>)</i>	Description	>	,	00	13.	9,	BY	V	
7~0		Write 0x88: Read data indirectly;														

SPROG\_RDATA (D4H) Information block/system block data read register

Bit number	7	6	5	4	3	2	1	0		
Symbol	<u>_</u>									
R/W		R								
Reset value				(	0					

Bit number	Bit symbol	27	Description	0
7~01.		Indirectly read the data	in the information block	
Pen (0)		12671 (0)	7 EU (0) 3 ,	_
Ova od.		hing. De	hing. De	
PIR		<i>y</i>	<i>Y</i>	

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## 3.2. RAM

ning benobyd com
re address of 11 16:58 There are 256 Bytes internal, the address is 00H~FFH, including working registers group, bit addressing areas, buffers and SFR, the buffer contain the stack area.

Internal low 128 Bytes: 00H~7FH has 128 Bytes. Read and write data by immediate addressing or indirect addressing.

Internal high 128 Bytes: 80H~FFH has 128 Bytes. Read and write data only by immediate addressing or indirect addressing.

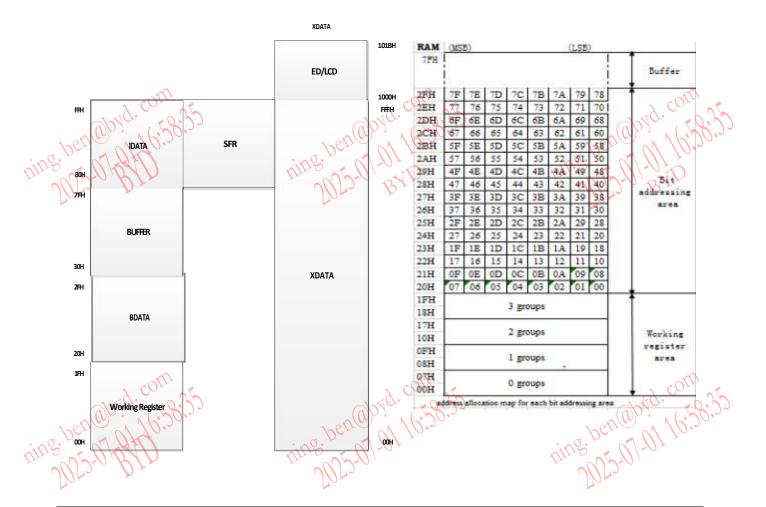
Special function register SFR: the address is 80H~FFH, Read and write data only by direct addressing.

Xdata have 4K Bytes, the address is 0000H~0FFFH, users can use this area completely. To read and write data through the data pointer or working registers group addressing mode.

LED/LCD storage RAM occupies XRAM, the address is 1000~101BH. This area is the LED display buffer, and the display content is modified by changing the area data

Note reserved stack space when writing a program, in order to avoid stack overflow and program goes wrong. Stack first address automatically assigned by program, when programming with C language, but it must be stored in data or idata. KEIL stack can be set in the first address in STARTUP.A51

RAM address space allocation map



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The faller	Vine Who lists the methods t	to got volue	in the three ports of DAM.		
ning the follow	wing table lists the methods t	MOV	A,direct		
1777		MOV	direct,A		
DATA		MOV	direct,#data		
DATA		MOV	direct1,direct2		
		MOV	Rn,direct		
		MOV	direct,Rn		
		MOV	A,@Ri		
		MOV	@Ri,A		
IDATA		MOV	direct,@Ri		
		MOV	@Ri,direct		
		MOV	@Ri,#data		
XDATA		MOVX @DPTR,A MOVX A,@DPTR			

RAM value instruction table

In the above table, n ranges from 0 to 7, and i ranges from 0 to 1.

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## 3.3. SFR Table

اللمم		The		The control of
Address	Name	RW	Reset	Description
0x80	DATAB	RW	1111_111b	PB data register
0x81	SP	RW	0000_0111b	Stack pointer register
0x82	DPL	RW	0000_0000b	Data pointer register0 low 8-bit
0x83	DPH	RW	0000_0000b	Data pointer register0 high 8-bit
0x84	TIMER3_CFG	RW	xxxx_x000b	TIMER3 configuration register
0x85	TIMER3_SET_H	RW	0000_0000Ь	TIMER3 count value configuration register, high 8 bits
0x86	TIMER3_SET_L	RW	0000_0000Ь	TIMER3 count value configuration register, low 8 bits
0x87	PCON	RW	xxxx_xxx0b	Idle mode 1 select register
0x88	TCON	RW	0000_0x0xb	Timer control register
0x89	TMOD	RW	xx00_xx00b	Timer mode register
0x8A	TL0	RW	0000_0000ь	Timer 0 counter low 8-bit
0x8B	TL1	RW	0000_0000Ь	Timer 1 counter low 8-bit
0x8C	TH0	RW	0000_0000b	Timer 0 counter high 8-bit
0x8D	TH1	RW	0000_0000b	Timer 1 counter high 8-bit
0x8E	SOFT_RST	RW	0000_0000ь	Soft reset register
0x90	DATAC	RW	1111_1111b	PC port data register
0x91	WDT_CTRL	RW	xxxx_x000b	WDT timing overflow control register
0x92	WDT_EN	RW	0000_0000ь	WDT timing enable register
0x93	TIMER2_CFG	RW	xxxx_x000b	TIMER2 configuration register
0x94	TIMER2_SET_H	RW	0000_0000Ь	TIMER2 count value configuration register, high 8 bits
0x95	TIMER2_SET_L	RW	0000_0000Ь	TIMER2 count value configuration register, low 8 bits
0x96	REG_ADDR	RW	0000_0000b	Second address bus register
0x97	REG_DATA	RW	0000_0000b	Second data read and write bus register
0x98	UART2_STATE	R/RW	x000_0000b	UART2 status flag register
0x99	PWM0_L_L	RW	0000_0000Ь	PWM0 low level control register (low 8-bit)
0x9A	PWM0_L_H	RW	0000_0000Ь	PWM0 low level control register (high 8-bit)
0x9B	PWM0_H_L	RW	0000_0000Ь	PWM0 high level control register (low 8-bit)
0x9C	PWM0_H_H	RW	0000_0000Ь	PWM0 high level control register (high 8-bit)
0x9D	PWM1_L_L	RW	0000_0000b	PWM1 low level control register

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(0)27	16.58.33			
period W	10.5			(low 8-bit)
0x9E	PWM1_L_H	RW	0000_0000ь	PWM1 low level control register (high 8-bit)
0x9F	PWM1_H_L	RW	0000_0000Ь	PWM1 high level control register (low 8-bit)
0xA0	P2_XH	RW	1111_1111b	MOVX @Ri, A operation pdata address high 8 bits
0xA1	PWM1_H_H	RW	0000_0000Ь	PWM1 high level control register (high 8-bit)
0xA2	PWM2_L_L	RW	0000_0000Ь	PWM2 low level control register (low 8-bit)
0xA3	PWM2_L_H	RW	0000_0000ь	PWM2 low level control register (high 8-bit)
0xA4	PWM2_H_L	RW	0000_0000ь	PWM2 high level control register (low 8-bit)
0xA5	PWM2_H_H	RW	0000_0000ь	PWM2 high level control register (high 8-bit)
0xA6	PWM3_L_L	RW	0000_0000ь	PWM3 low level control register (low 8-bit)
0xA7	PWM3_L_H	RW	0000_0000Ь	PWM3 low level control register (high 8-bit)
0xA8	IEN0	RW	0xxx_0000b	Interrupt enable register
0xA9	PWM3_H_L	RW	0000_0000Ь	PWM3 high level control register (low 8-bit)
0xAA	PWM3_H_H	RW	0000_0000Ь	PWM3 high level control register (high 8-bit))
0xAD	SYS_CLK_CFG	RW	xxx0_1000b	System clock configuration register
0xAE	INT_PE_STAT	RW	0000_0000b	Interrupt status register
0xAF	SCAN_START	RW	xxxx_xxx0b	LCD, LED scan open register
0xB0	DATAE	RW	1111_1111b	PE data register
0xB1	DP_CON	RW	x000_0000b	LCD, LED control register
0xB2	DP_MODE	RW	0000_0000b	LCD, LED mode register
0xB3	SCAN_WIDTH	RW	0000_0000b	LED period configuration register
0xB4	LED2_WIDTH	RW	0000_0000ь	LED dot matrix drive mode cycle configuration register
0xB5	SPI_CFG1	RW	0001_0101b	SPI control register 1
0xB6	SPI_CFG2	RW	x001_1000b	SPI control register 2
0xB8	IPL0	RW	xxxx_0000b	Interrupt priority register 0
0xB9	DP_CON1	RW	x000_0000b	LCD contrast configuration register
0xBA	UART2_BDL	RW	0000_0000b	UART2 baud rate control register

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OXBB         ÜART2 CON1         RW         x000_0000b         UART2 mode control register 1           OXBC         UART IO CTRL1         RW         xx00_0000b         UART pin enable register           OXBD         UART2 BUF         RW         xxxxx x001b         SPI status flag register           OXBF         SPI SIPD         RW         0000_0000b         SPI data register           OXC0         DATAF         RW         1111_1111b         PF data register           OxC1         ADC SPT         RW         0000_0000b         SPI data register           0xC1         ADC SPT         RW         0000_0000b         ADC sample time configuration register           0xC2         UART JXD/RXD pin exchange register           0xC3         ADC SCAN CFG         RW         x000_0000b         ADC scan configuration register           0xC4         ADCCKC         RW         x000_0000b         ADC scan result register register           0xC5         ADC_RDATAH         R         xxxx         xxxx         ADC scan result register ligh 4 bits           0xC6         ADC_RDATAL         R         0000_0000b         External Interrupt status register           0xC8         DATAG         RW         xxxx         xxxx         xxxx         xxxx	(0)	(.,70.5			
OxBD         UART2 BUF         RW         1111 1111b         UART2 data registerv           0xBE         SPI STATE         RW         xxxx x001b         SPI status flag register           0xBF         SPI SIPD         RW         0000 0000b         SPI data register           0xC0         DATAF         RW         1111 1111b         PF data register           0xC1         ADC SPT         RW         0000 0000b         ADC sample time configuration register           0xC2         UART IO_CTRL         RW         xxxxx x000b         ADC scan configuration register           0xC3         ADC SCAN CFG         RW         xxxx x000b         ADC scan configuration register           0xC4         ADCCKC         RW         0000 0000b         ADC scan result register low 8 bits           0xC5         ADC RDATAL         R         0000 0000b         ADC scan result register low 8 bits           0xC6         ADC_RDATAL         R         0000 0000b         ADC scan result register low 8 bits           0xC7         EXINT STAT         RW         0000 0000b         External Interrupt status register           0xC8         DATAG         RW         xxxxx 1111b         PG data register           0xCA         PULL_I SELA_L         RW         0000 0000b	0xBB	UART2_CON1	RW	x000_0000b	UART2 mode control register 1
0xBE         SPI_STATE         RW         xxxx x001b         SPI status flag register           0xBF         SPI_SIPD         RW         0000_0000b         SPI data register           0xC0         DATAF         RW         1111_1111b         PF data register           0xC1         ADC_SPT         RW         0000_0000b         ADC sample time configuration register           0xC2         UART_IO_CTRL         RW         xxxxx_x000b         ADC scan configuration register           0xC3         ADC_SCAN_CFG         RW         xxxx_x000b         ADC scan configuration register           0xC4         ADCCKC         RW         0000_0000b         ADC scan result register high 4 bits           0xC5         ADC_RDATAH         R         xxxx_x0000b         ADC scan result register low 8 bits           0xC6         ADC_RDATAL         R         0000_0000b         ADC scan result register low 8 bits           0xC7         EXINT_STAT         RW         0000_0000b         External Interrupt status register           0xC8         DATAG         RW         xxxx_1111b         PG data register           0xCB         SPROG_ADDR_H         RW         0000_0000b         Address control register           0xCF         SPROG_ADDR_L         RW         0000_000	0xBC	UART_IO_CTRL1	RW	xx00_0000b	UART pin enable register
0xBF         SPI SIPD         RW         0000_0000b         SPI data register           0xC0         DATAF         RW         1111_1111b         PF data register           0xC1         ADC_SPT         RW         0000_0000b         ADC sample time configuration register           0xC2         UART_IO_CTRL         RW         xxxx_x000b         UART_TXD/RXD pin exchange register           0xC3         ADC_SCAN_CFG         RW         x000_0000b         ADC scan configuration register           0xC4         ADC_RDATAH         R         xxxx_x 0000b         ADC scan result register high 4 bits           0xC6         ADC_RDATAL         R         0000_0000b         ADC scan result register low 8 bits           0xC7         EXINT_STAT         RW         0000_0000b         ADC scan result register low 8 bits           0xC8         DATAG         RW         xxxx_1111b         PG data register           0xC8         DATAG         RW         xxxx_111b         PG data register           0xCA         PULL_L_SELA_L         RW         0000_000b         Pull-up current source size selection register           0xCE         SPROG_ADDR_H         RW         0000_000b         Address control register           0xCF         SPROG_ADDR_A         RW         0	0xBD	UART2_BUF	RW	1111_1111b	UART2 data registerv
0xC0         DATAF         RW         1111         1111b         PF data register           0xC1         ADC SPT         RW         0000_0000b         ADC sample time configuration register           0xC2         UART_IO_CTRL         RW         xxxxx_x000b         VART TXD/RXD pin exchange register           0xC3         ADC_SCAN_CFG         RW         x000_0000b         ADC clock and filter configuration register           0xC4         ADC_RDATAH         R         xxxxx_0000b         ADC scan result register high 4 bits           0xC5         ADC_RDATAL         R         0000_0000b         ADC scan result register low 8 bits           0xC6         ADC_RDATAL         R         0000_0000b         External Interrupt status register           0xC6         ADC_RDATAL         RW         0000_0000b         External Interrupt status register           0xC8         DATAG         RW         xxxxx_1111b         PG data register           0xCA         PULL_L_SELA_L         RW         0000_0000b         Address control register           0xCE         SPROG_ADDR_H         RW         0000_0000b         Address control register           0xD1         SPROG_ADATA         RW         0000_0000b         Write data register           0xD2         SPROG_CMD	0xBE	SPI_STATE	RW	xxxx_x001b	SPI status flag register
0xC1         ADC SPT         RW         0000 0000b         ADC sample time configuration register           0xC2         UART_IO_CTRL         RW         xxxxx_x000b         UART TXD/RXD pin exchange register           0xC3         ADC_SCAN_CFG         RW         x000_000b         ADC scan configuration register           0xC4         ADCCKC         RW         0000_000b         ADC clock and filter configuration register           0xC5         ADC RDATAH         R         xxxxx_000b         ADC scan result register high 4 bits           0xC6         ADC RDATAL         R         0000_000b         ADC scan result register low 8 bits           0xC7         EXINT_STAT         RW         0000_000b         External Interrupt status register           0xC8         DATAG         RW         xxxx_1111b         PG data register           0xCA         PULL_L SELA_L         RW         0000_000b         Address control register           0xCE         SPROG_ADDR_H         RW         0000_000b         Address control register           0xCF         SPROG_ADDR_L         RW         0000_000b         Address control register           0xD1         SPROG_DATA         RW         0000_000b         Write data register           0xD2         SPROG_CMD         RW <td>0xBF</td> <td>SPI_SIPD</td> <td>RW</td> <td>0000_0000b</td> <td>SPI data register</td>	0xBF	SPI_SIPD	RW	0000_0000b	SPI data register
0xC2         UART_IO_CTRL         RW         xxxx_x000b         UART TXD/RXD pin exchange register           0xC3         ADC_SCAN_CFG         RW         x000_0000b         ADC scan configuration register           0xC4         ADCCKC         RW         0000_0000b         ADC clock and filter configuration register           0xC5         ADC_RDATAH         R         xxxx 0000b         ADC scan result register high 4 bits           0xC6         ADC_RDATAL         R         0000_0000b         External Interrupt status register           0xC6         ADC RDATAL         R         0000_0000b         External Interrupt status register           0xC8         DATAG         RW         xxxxx_1111b         PG data register           0xC8         DATAG         RW         xxxx_1111b         PG data register           0xCA         PULL_I_SELA_L         RW         0000_0000b         Address control register           0xCE         SPROG_ADDR H         RW         0000_0000b         Address control register           0xCF         SPROG_ADDR L         RW         0000_0000b         Address control register           0xD1         SPROG_ADDR R         RW         0000_0000b         Write data register           0xD1         SPROG_CMD         RW         00	0xC0	DATAF	RW	1111_1111b	PF data register
0xC2         OART_IO_CTRL         RW         xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	0xC1	ADC_SPT	RW	0000_0000b	ADC sample time configuration register
0xC4         ADCCKC         RW         0000_0000b         ADC clock and filter configuration register           0xC5         ADC_RDATAH         R         xxxxx_0000b         ADC scan result register high 4 bits           0xC6         ADC_RDATAL         R         0000_0000b         ADC scan result register low 8 bits           0xC7         EXINT_STAT         RW         0000_0000b         External Interrupt status register           0xC8         DATAG         RW         xxxxx_1111b         PG data register           0xCA         PULL_I_SELA_L         RW         0000_0000b         Address control register           0xCE         SPROG_ADDR_H         RW         0000_0000b         Address control register           0xCF         SPROG_ADDR_L         RW         0000_0000b         Program status word register           0xD0         PSW         R/RW         0000_0000b         Write data register           0xD1         SPROG_DATA         RW         0000_0000b         Command register           0xD2         SPROG_CMD         RW         0000_0000b         Command register           0xD3         SPROG_RDATA         R         0000_0000b         Information block/system block data read register           0xD4         SPROG_RDATA         R         0	0xC2	UART_IO_CTRL	RW	xxxx_x000b	
0xC5         ADC_RDATAH         R         xxxx         0000_0000b         register           0xC6         ADC_RDATAL         R         0000_0000b         ADC scan result register low 8 bits           0xC7         EXINT_STAT         RW         0000_0000b         External Interrupt status register           0xC8         DATAG         RW         xxxxx_1111b         PG data register           0xCA         PULL_I_SELA_L         RW         0000_0000b         Pull-up current source size selection register           0xCE         SPROG_ADDR_H         RW         0000_0000b         Address control register           0xCF         SPROG_ADDR_L         RW         0000_0000b         Address control register low 8 bits           0xD0         PSW         R/RW         0000_0000b         Program status word register           0xD1         SPROG_DATA         RW         0000_0000b         Write data register           0xD2         SPROG_CMD         RW         0000_0000b         Command register           0xD3         SPROG_TIM         RW         1101_1101b         Erase time control register           0xD4         SPROG_RDATA         R         0000_0000b         Information block/system block data read register           0xD5         INT_POBO_STAT         <	0xC3	ADC_SCAN_CFG	RW	x000_0000b	ADC scan configuration register
0xC6         ADC_RDATAL         R         0000_0000b         ADC scan result register low 8 bits           0xC7         EXINT_STAT         RW         0000_0000b         External Interrupt status register           0xC8         DATAG         RW         xxxx_1111b         PG data register           0xCA         PULL_I_SELA_L         RW         0000_0000b         Pull-up current source size selection register           0xCE         SPROG_ADDR_H         RW         0000_0000b         Address control register           0xCF         SPROG_ADDR_L         RW         0000_0000b         Address control register low 8 bits           0xD0         PSW         R/RW         0000_0000b         Address control register low 8 bits           0xD0         PSW         R/RW         0000_0000b         Program status word register           0xD1         SPROG_DATA         RW         0000_0000b         Write data register           0xD2         SPROG_CMD         RW         0000_0000b         Command register           0xD3         SPROG_RDATA         R         0000_0000b         Command register           0xD4         SPROG_RDATA         R         0000_0000b         LVDT boost/buck interrupt status register           0xD5         INT_POBO_STAT         RW	0xC4	ADCCKC	RW	0000_0000Ь	
0xC7EXINT_STATRW0000_0000bExternal Interrupt status register0xC8DATAGRWxxxx_1111bPG data register0xCAPULL_I_SELA_LRW0000_0000bPull-up current source size selection register0xCESPROG_ADDR_HRW0000_0000bAddress control register0xCFSPROG_ADDR_LRW0000_0000bAddress control register low 8 bits0xD0PSWR/RW0000_0000bProgram status word register0xD1SPROG_DATARW0000_0000bWrite data register0xD2SPROG_CMDRW0000_0000bCommand register0xD3SPROG_TIMRW1101_1101bErase time control register0xD4SPROG_RDATAR0000_0000bInformation block/system block data read register0xD5INT_POBO_STATRWxxxx_xxx00bLVDT boost/buck interrupt status register0xD6UART1_BDLRW0000_0000bUART1 baudrate control register0xD7UART1_CON1RWx000_0000bUART1 mode control register0xD8DATAHRW1111_1111bPH data register0xD9UART1_CON2RWxx00_1100bUART1 status flag register0xDBUART1_BUFRW1111_1111bUART1 data register0xDCUART0_BDLRWx000_0000bUART0 mode control register 10xDEUART0_CON1RWx000_0000bUART0 mode control register 20xDFUART0_CON2RWxx00_1100bUART0 status flag registe	0xC5	ADC_RDATAH	R	xxxx_0000b	ADC scan result register high 4 bits
0xC8DATAGRWxxxx 1111bPG data register0xCAPULL_I_SELA_LRW0000_0000bPull-up current source size selection register0xCESPROG ADDR_HRW0000_0000bAddress control register0xCFSPROG ADDR_LRW0000_0000bAddress control register low 8 bits0xD0PSWR/RW0000_0000bProgram status word register0xD1SPROG DATARW0000_0000bWrite data register0xD2SPROG CMDRW0000_0000bCommand register0xD3SPROG TIMRW1101_1101bErase time control register0xD4SPROG_RDATAR0000_0000bInformation block/system block data read register0xD5INT_POBO_STATRWxxxx_xx00bLVDT boost/buck interrupt status register0xD6UART1_BDLRW0000_0000bUART1 baudrate control register0xD7UART1_CON1RWx000_0000bUART1 mode control register 10xD8DATAHRW1111_1111bPH data register0xD9UART1_CON2RWxx00_1100bUART1 mode control register 20xDAUART1 BUFRW1111_1111bUART1 data register0xDBUART1 BUFRW1111_1111bUART1 data register0xDCUART0_BDLRW0000_0000bUART0_baudrate control register 10xDEUART0_CON1RWxx00_1100bUART0_mode control register 20xDFUART0_CON2RWxx00_1100bUART0_mode control register 2 <td>0xC6</td> <td>ADC_RDATAL</td> <td>R</td> <td>0000_0000b</td> <td>ADC scan result register low 8 bits</td>	0xC6	ADC_RDATAL	R	0000_0000b	ADC scan result register low 8 bits
0xCA         PULL_I_SELA_L         RW         0000_0000b         Pull-up current source size selection register           0xCE         SPROG_ADDR_H         RW         0000_0000b         Address control register           0xCF         SPROG_ADDR_L         RW         0000_0000b         Address control register low 8 bits           0xD0         PSW         R/RW         0000_0000b         Program status word register           0xD1         SPROG_DATA         RW         0000_0000b         Write data register           0xD2         SPROG_CMD         RW         0000_0000b         Command register           0xD3         SPROG_RDATA         R         0000_0000b         Information block/system block data read register           0xD4         SPROG_RDATA         R         0000_0000b         LVDT boost/buck interrupt status register           0xD5         INT_POBO_STAT         RW         xxxxx_xx00b         LVDT boost/buck interrupt status register           0xD6         UART1 BDL         RW         0000_0000b         UART1 bould rate control register           0xD7         UART1 CON1         RW         x000_0000b         UART1 mode control register           0xD9         UART1 CON2         RW         xx00_1100b         UART1 mode control register           0xDB	0xC7	EXINT_STAT	RW	0000_0000Ь	External Interrupt status register
0xCA         FOLE_I_SELA_L         RW         0000_0000b         register           0xCE         SPROG_ADDR_L         RW         0000_0000b         Address control register           0xCF         SPROG_ADDR_L         RW         0000_0000b         Address control register low 8 bits           0xD0         PSW         R/RW         0000_0000b         Program status word register           0xD1         SPROG_DATA         RW         0000_0000b         Command register           0xD2         SPROG_CMD         RW         0000_0000b         Command register           0xD3         SPROG_TIM         RW         1101_1101b         Erase time control register           0xD4         SPROG_RDATA         R         0000_0000b         Information block/system block data read register           0xD5         INT_POBO_STAT         RW         xxxxx_xx00b         LVDT boost/buck interrupt status register           0xD6         UART1_BDL         RW         x000_0000b         UART1 baudrate control register           0xD7         UART1_CON1         RW         x000_0000b         UART1 mode control register           0xD8         DATAH         RW         1111_1111b         PH data register           0xDA         UART1_STATE         RW         x000_0000b	0xC8	DATAG	RW	xxxx_1111b	PG data register
0xCFSPROG ADDR LRW0000 0000bAddress control register low 8 bits0xD0PSWR/RW0000 0000bProgram status word register0xD1SPROG DATARW0000 0000bWrite data register0xD2SPROG CMDRW0000 0000bCommand register0xD3SPROG TIMRW1101 1101bErase time control register0xD4SPROG RDATAR0000 0000bInformation block/system block data read register0xD5INT_POBO_STATRWxxxxx_xx00bLVDT boost/buck interrupt status register0xD6UART1 BDLRW0000 0000bUART1 baudrate control register0xD7UART1 CON1RWx000 0000bUART1 mode control register 10xD8DATAHRW1111 1111bPH data register0xD9UART1 CON2RWxx00 1100bUART1 mode control register 20xDAUART1 STATERWx000 0000bUART1 status flag register0xDBUART1 BUFRW1111 1111bUART1 data register0xDCUART0 BDLRWx000 0000bUART0 baudrate control register 10xDDUART0 CON1RWx000 0000bUART0 mode control register 20xDFUART0 CON2RWxxx0 1100bUART0 mode control register 20xDFUART0 STATERWx000 0000bUART0 status flag register	0xCA	PULL_I_SELA_L	RW	0000_0000Ь	_
0xD0         PSW         R/RW         0000 0000b         Program status word register           0xD1         SPROG DATA         RW         0000 0000b         Write data register           0xD2         SPROG CMD         RW         0000 0000b         Command register           0xD3         SPROG TIM         RW         1101 1101b         Erase time control register           0xD4         SPROG RDATA         R         0000 0000b         Information block/system block data read register           0xD5         INT_POBO_STAT         RW         xxxxx_xx00b         LVDT boost/buck interrupt status register           0xD6         UART1 BDL         RW         0000 0000b         UART1 baudrate control register           0xD7         UART1 CON1         RW         x000 0000b         UART1 mode control register 1           0xD8         DATAH         RW         1111 1111b         PH data register           0xD9         UART1 CON2         RW         xx00_1100b         UART1 mode control register 2           0xDA         UART1 STATE         RW         x000_0000b         UART1 status flag register           0xDC         UART0 BDL         RW         1111 1111b         UART1 data register           0xDD         UART0 CON1         RW         x000_0000b </td <td>0xCE</td> <td>SPROG_ADDR_H</td> <td>RW</td> <td>0000_0000Ь</td> <td>Address control register</td>	0xCE	SPROG_ADDR_H	RW	0000_0000Ь	Address control register
0xD1SPROG DATARW0000_0000bWrite data register0xD2SPROG CMDRW0000_0000bCommand register0xD3SPROG TIMRW1101_1101bErase time control register0xD4SPROG_RDATAR0000_0000bInformation block/system block data read register0xD5INT_POBO_STATRWxxxxx_xx00bLVDT boost/buck interrupt status register0xD6UART1_BDLRW0000_0000bUART1 baudrate control register0xD7UART1_CON1RWx000_0000bUART1 mode control register 10xD8DATAHRW1111_1111bPH data register0xD9UART1_CON2RWxx00_1100bUART1 mode control register 20xDAUART1_STATERWx000_0000bUART1 status flag register0xDBUART1_BUFRW1111_1111bUART1 data register0xDCUART0_BDLRW0000_0000bUART0 baudrate control register 10xDDUART0_CON1RWx000_0000bUART0 mode control register 10xDEUART0_CON2RWxx00_1100bUART0 mode control register 20xDFUART0_STATERWx000_0000bUART0 status flag register	0xCF	SPROG_ADDR_L	RW	0000_0000Ь	Address control register low 8 bits
0xD2SPROG CMDRW0000_0000bCommand register0xD3SPROG TIMRW1101_1101bErase time control register0xD4SPROG_RDATAR0000_0000bInformation block/system block data read register0xD5INT_POBO_STATRWxxxxx_xx00bLVDT boost/buck interrupt status register0xD6UART1_BDLRW0000_0000bUART1 baudrate control register0xD7UART1_CON1RWx000_0000bUART1 mode control register 10xD8DATAHRW1111_1111bPH data register0xD9UART1_CON2RWxx00_1100bUART1 mode control register 20xDAUART1_STATERWx000_0000bUART1 status flag register0xDBUART1_BUFRW1111_1111bUART1 data register0xDCUART0_BDLRW0000_0000bUART0 baudrate control register0xDDUART0_CON1RWx000_0000bUART0 mode control register 10xDEUART0_CON2RWxx00_1100bUART0 mode control register 20xDFUART0_STATERWx000_0000bUART0 status flag register	0xD0	PSW	R/RW	0000_0000Ь	Program status word register
0xD3SPROG TIMRW1101_1101bErase time control register0xD4SPROG_RDATAR0000_0000bInformation block/system block data read register0xD5INT_POBO_STATRWxxxxx_xx00bLVDT boost/buck interrupt status register0xD6UART1_BDLRW0000_0000bUART1 baudrate control register0xD7UART1_CON1RWx000_0000bUART1 mode control register 10xD8DATAHRW1111_1111bPH data register0xD9UART1_CON2RWxx00_1100bUART1 mode control register 20xDAUART1_STATERWx000_0000bUART1 status flag register0xDBUART1_BUFRW1111_1111bUART1 data register0xDCUART0_BDLRW0000_0000bUART0 baudrate control register 10xDDUART0_CON1RWx000_0000bUART0 mode control register 10xDEUART0_CON2RWxx00_1100bUART0 mode control register 20xDFUART0_STATERWx000_0000bUART0 status flag register	0xD1	SPROG_DATA	RW	0000_0000b	Write data register
0xD4SPROG_RDATAR0000_0000bInformation block/system block data read register0xD5INT_POBO_STATRWxxxx_xx00bLVDT boost/buck interrupt status register0xD6UART1_BDLRW0000_0000bUART1 baudrate control register0xD7UART1_CON1RWx000_0000bUART1 mode control register 10xD8DATAHRW1111_1111bPH data register0xD9UART1_CON2RWxx00_1100bUART1 mode control register 20xDAUART1_STATERWx000_0000bUART1 status flag register0xDBUART1_BUFRW1111_1111bUART1 data register0xDCUART0_BDLRW0000_0000bUART0 baudrate control register0xDDUART0_CON1RWx000_0000bUART0 mode control register 10xDEUART0_CON2RWxx00_1100bUART0 mode control register 20xDFUART0_STATERWx000_0000bUART0 status flag register	0xD2	SPROG_CMD	RW	0000_0000b	Command register
0xD4SPROG_RDATAR0000_0000bread register0xD5INT_POBO_STATRWxxxx_xx00bLVDT boost/buck interrupt status register0xD6UART1_BDLRW0000_0000bUART1 baudrate control register0xD7UART1_CON1RWx000_0000bUART1 mode control register 10xD8DATAHRW1111_1111bPH data register0xD9UART1_CON2RWxx00_1100bUART1 mode control register 20xDAUART1_STATERWx000_0000bUART1 status flag register0xDBUART1_BUFRW1111_1111bUART1 data register0xDCUART0_BDLRW0000_0000bUART0 baudrate control register0xDDUART0_CON1RWx000_0000bUART0 mode control register 10xDEUART0_CON2RWxx00_1100bUART0 mode control register 20xDFUART0_STATERWx000_0000bUART0 status flag register	0xD3	SPROG_TIM	RW	1101_1101b	Erase time control register
0xD6UART1 BDLRW0000 0000bUART1 baudrate control register0xD7UART1 CON1RWx000 0000bUART1 mode control register 10xD8DATAHRW1111 1111bPH data register0xD9UART1 CON2RWxx00 1100bUART1 mode control register 20xDAUART1 STATERWx000 0000bUART1 status flag register0xDBUART1 BUFRW1111 1111bUART1 data register0xDCUART0 BDLRW0000 0000bUART0 baudrate control register0xDDUART0 CON1RWx000 0000bUART0 mode control register 10xDEUART0 CON2RWxx00 1100bUART0 mode control register 20xDFUART0 STATERWx000 0000bUART0 status flag register	0xD4	SPROG_RDATA	R	0000_0000Ь	
0xD7UART1 CON1RWx000 0000bUART1 mode control register 10xD8DATAHRW1111 1111bPH data register0xD9UART1 CON2RWxx00 1100bUART1 mode control register 20xDAUART1 STATERWx000 0000bUART1 status flag register0xDBUART1 BUFRW1111 1111bUART1 data register0xDCUART0 BDLRW0000 0000bUART0 baudrate control register0xDDUART0 CON1RWx000 0000bUART0 mode control register 10xDEUART0 CON2RWxx00 1100bUART0 mode control register 20xDFUART0 STATERWx000 0000bUART0 status flag register	0xD5	INT_POBO_STAT	RW	xxxx_xx00b	_
0xD8DATAHRW1111 1111bPH data register0xD9UART1 CON2RWxx00 1100bUART1 mode control register 20xDAUART1 STATERWx000 0000bUART1 status flag register0xDBUART1 BUFRW1111 1111bUART1 data register0xDCUART0 BDLRW0000 0000bUART0 baudrate control register0xDDUART0 CON1RWx000 0000bUART0 mode control register 10xDEUART0 CON2RWxx00 1100bUART0 mode control register 20xDFUART0 STATERWx000 0000bUART0 status flag register	0xD6	UART1_BDL	RW	0000_0000b	UART1 baudrate control register
0xD9UART1_CON2RWxx00_1100bUART1 mode control register 20xDAUART1_STATERWx000_0000bUART1 status flag register0xDBUART1_BUFRW1111_1111bUART1 data register0xDCUART0_BDLRW0000_0000bUART0 baudrate control register0xDDUART0_CON1RWx000_0000bUART0 mode control register 10xDEUART0_CON2RWxx00_1100bUART0 mode control register 20xDFUART0_STATERWx000_0000bUART0 status flag register	0xD7	UART1_CON1	RW	x000_0000b	UART1 mode control register 1
0xDAUART1 STATERWx000 0000bUART1 status flag register0xDBUART1 BUFRW1111 1111bUART1 data register0xDCUART0 BDLRW0000 0000bUART0 baudrate control register0xDDUART0 CON1RWx000 0000bUART0 mode control register 10xDEUART0 CON2RWxx00 1100bUART0 mode control register 20xDFUART0 STATERWx000 0000bUART0 status flag register	0xD8	DATAH	RW	1111_1111b	PH data register
0xDBUART1 BUFRW1111 1111bUART1 data register0xDCUART0 BDLRW0000 0000bUART0 baudrate control register0xDDUART0 CON1RWx000 0000bUART0 mode control register 10xDEUART0 CON2RWxx00 1100bUART0 mode control register 20xDFUART0 STATERWx000 0000bUART0 status flag register	0xD9	UART1_CON2	RW	xx00_1100b	UART1 mode control register 2
0xDCUART0_BDLRW0000_0000bUART0 baudrate control register0xDDUART0_CON1RWx000_0000bUART0 mode control register 10xDEUART0_CON2RWxx00_1100bUART0 mode control register 20xDFUART0_STATERWx000_0000bUART0 status flag register	0xDA	UART1_STATE	RW	x000_0000b	UART1 status flag register
0xDDUART0_CON1RWx000_0000bUART0 mode control register 10xDEUART0_CON2RWxx00_1100bUART0 mode control register 20xDFUART0_STATERWx000_000bUART0 status flag register	0xDB	UART1_BUF	RW	1111_1111b	UART1 data register
0xDE     UART0_CON2     RW     xx00_1100b     UART0 mode control register 2       0xDF     UART0_STATE     RW     x000_000b     UART0 status flag register	0xDC	UART0_BDL	RW	0000_0000b	UART0 baudrate control register
0xDF UART0_STATE RW x000_0000b UART0 status flag register	0xDD	UART0_CON1	RW	x000_0000b	UART0 mode control register 1
	0xDE	UART0_CON2	RW	xx00_1100b	UART0 mode control register 2
0xE0 ACC RW 0000_0000b Accumulator	0xDF	UARTO_STATE	RW	x000_0000b	UART0 status flag register
	0xE0	ACC	RW	0000_0000b	Accumulator

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0xE1	IRCON2	RW	0000_0000b	Interrupt flag register 2
0xE2	UART0_BUF	RW	1111_1111b	UART0 data register
0xE3	IICADD	RW	0000_000xb	IIC address register
0xE4	IICBUF	RW	0000_0000Ь	IIC send and receive data register
0xE5	IICCON	RW	xx01_0000b	IIC configuration register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xE7	IEN2	RW	0000_0000b	Interrupt enable register 2
0xE8	IICSTAT	R/RW	0100_0100b	IIC status register
0xE9	IICBUFFER	RW	0000_0000ь	IIC transmit and receive data buffer register
0xEA	TRISA	RW	xxxx_1111b	PA direction register
0xEB	TRISB	RW	1111_1111b	PB direction register
0xEC	TRISC	RW	1111_111b	PC direction register
0xED	UART2_CON2	RW	xx00_1100b	UART2 mode control register 2
0xEE	TRISE	RW	1111_111b	PE direction register
0xEF	TRISF	RW	1111_1111b	PF direction register
0xF0	В	RW	0000_0000Ь	B register
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF2	TRISG	RW	xxxx_1111b	PG direction register
0xF4	IPL2	RW	0000_0000b	Interrupt priority register 2
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xF7	TRISH	RW	1111_1111b	PH direction register
0xF8	DATAA	RW	xxxx_1111b	PA data register
0xFA	PWM_INT_CTRL	RW	xxxx_xx00b	PWM interrupt enable control register

#### Note:

- 1. Registers whose addresses end in 8 or 0 can be bit-operated, for example, registers 0x80 and 0x88.
- 2. Reset value: reset value of different modes (8 reset modes: power-on reset, power-off reset, programming reset, software reset, modify configuration reset, watchdog timer overflow reset, PC pointer overflow reset, ROM address jump reset).
- 3. 'x': indefinite, reserved bit.
- 4. R: read only; RW: Read and write.
- 5. the reserved register and register reserved bits, forbid write operations, otherwise may cause chip abnormalities.

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### 3.4. Secondary Bus Register Table

The BF7515CM44-LJTX series supports expanded secondary bus registers for expanding more register functions. Just write the address of the secondary bus register to be accessed into REG\_ADDR, and then access the corresponding secondary bus register through the REG\_DATA register. It is recommended that when reading and writing secondary bus registers, first EA = 0, and then EA = 1 after the operation is completed. Prevent other interrupts or operations from modifying the address or data of the secondary bus register.

	Secondary bus										
Address	Name	Description	Reset								
0x96	REG_ADDR	<7:0>	RW	Second address bus register	0x00						
0x97	REG DATA	<7:0>	RW	Second data read and write bus register	0x00						

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Addr	Name	RW	Reset	Description
0x00	CFG0_REG	R	1111_1111111111111111111111111111111111	Configuration word register 0
0x01	CFG1_REG	R	0110_0100b 1	Configuration word register 1
0x02	CFG2_REG	R	0001_1111b 1	Configuration word register 2
0x03	CFG3_REG	R	1111_1111b 1	Configuration word register 3
0x04	CFG4_REG	R	0010_1101b 1	Configuration word register 4
0x05	CFG5_REG	R	1100_1001b 1	Configuration word register 5
0x06	CFG6_REG	R	0011_1111b 1	Configuration word register 6
0x07	CFG7_REG	R	0001_1111b 1	Configuration word register 7
0x08	CFG8_REG	R	1111 <u>1</u> 1111b 1	Configuration word register 8
0x09	CFG9_REG	R	1111 <u>1</u> 1111b 1	Configuration word register 9
0x0A	CFG10_REG	R	1111_1111b 1	Configuration word register 10
0x0B	CFG11_REG	R	1111_1111b 1	Configuration word register 11
0x0C	CFG12_REG	R	0111_1111b 1	Configuration word register 12
0x0D	CFG13_REG	R	0000_0111b 1	Configuration word register 13
0x0F	RST_STAT	RW	0000_0010b 2	Reset flag register
0x17	PU_PA	RW	xxxx_0000b	PA port pull-up resistor control register
0x18	PU_PB	RW	0000_0000ь	PB port pull-up resistor control register
0x19	PU_PC	RW	0000_0000ь	PC port pull-up resistor control register
0x1B	PU_PE	RW	0000_0000ь	PE port pull-up resistor control register
0x1C	PU_PF	RW	0000_0000ь	PF port pull-up resistor control register
0x1D	PU_PG	RW	xxxx_0000b	PG port pull-up resistor control register
0x1E	PU_PH	RW	0000_0000ь	PH port pull-up resistor control register
0x1F	LCD_IO_SEL_1	RW	0000_0000Ь	LCD_SEG0-7 port select configuration register
0x20	LCD_IO_SEL_2	RW	0000_0000ь	LCD_SEG8-15 port select configuration register

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$-\infty(0)$	0) (.50.33			
0x21	LCD_IO_SEL_3	RW	0000_0000ь	LCD_SEG16-23 port select configuration register
0x22	LCD_IO_SEL_4	RW	xxxx_0000b	LCD_SEG24-27 port select configuration register
0x23	COM_IO_SEL	RW	0000_0000Ь	COM select configuration register
0x24	SEG_IO_SEL	RW	0000_0000ь	LED_SEG0-7 port select configuration register
0x25	ODRAIN_EN	RW	xxxx_0000b	PC4/5/PE4/5 open drain output enable register
0x2A	ADC_IO_SEL0	RW	x000_0000b	ADC function selection register
0x2C	SEL_LVDT_VTH	RW	xxxx_x000b	LVDT threshold selection register
0x2D	PD_ANA	RW	x111_xx11b	Analog module switch register
0x30	IDLE_WAKE_CFG	RW	xxxx_x111b	System wake up configuration register
0x31	LED_DRIVE	RW	xxxx_0000b	LED port drive capability configuration register
0x32	ADC CFG SEL	RW	x000_0000b	ADC configuration register
0x33	PWM IO SEL	RW	0000 0000b	PWM port selection register
0x34	PERIPH IO SEL1	RW	0001 0000b	External port function selection register 1
0x35	PERIPH IO SEL2	RW	0000 0000Ь	External port function selection register 2
0x36	PERIPH IO SEL3	RW	1xxx xxxxb	External port function selection register 3
0x37	PERIPH IO SEL4	RW	0xxx x000b	External port function selection register 4
0x38	PERIPH IO SEL5	RW	0000 0000ь	External port function selection register 5
0x39	EXT INT CON1	RW	0101 0101b	External interrupt configuration register 1
0x3A	EXT INT CON2	RW	xxxx x001b	External interrupt configuration register 2
0x3E	SPI_TX_START_ADDR	RW	0000_0000Ь	SPI High-speed mode send buffer first address
0x3F	SPI_RX_START_ADDR	RW	0000_0000ь	SPI high-speed mode receive buffer first address
0x40	SPI_NUM_L	RW	0000_0000Ь	SPI high-speed mode data cache address number low 8 bits
0x41	SPI_NUM_H	RW	xxxx_0000b	SPI high-speed mode data cache address number high 4 bits
0x42	ADC_CFG_SEL1	RW	xx00_0010b	ADC comparator offset cancellation selection register
0x50	IIC_FIL_MODE	RW	xxxx_xx10b	IIC filter selection register
0x53	ADC_IO_SEL1	RW	0000_0000Ь	ADC select enable register 1
0x54	ADC_IO_SEL2	RW	0000_0000Ь	ADC select enable register 2
0x55	ADC_IO_SEL3	RW	0000_0000Ь	ADC select enable register 3
0x56	ADC_IO_SEL4	RW	0000_0000Ь	ADC select enable register 4
0x57	ADC_IO_SEL5	RW	xxx0_0000b	ADC select enable register 5

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	- 110				
1	0x58	LED_IO_START	RW	xxxx_x000b	LED scan start selection register
Ó	0x59	PWM_IO_SEL1	RW	xxxx_0000b	PWM port selection register 1
	0x5A	FLASH_BOOT_EN	RO	xxxx_xxx0b	BOOT mode status register
(	0x5B	EEP_SELECT	RW	xxxx_xxx0b	DATA area selection register
	0x60	PWM0_POLA_SEL	RW	xxx0_0000b	PWM0 polarity selection register
	0x61	PWM1_POLA_SEL	RW	xxx0_0000b	PWM1 polarity selection register
	0x63	XTAL_CLK_SEL	RW	xxxx_xxx0b	Crystal frequency selection register
	0x65	SEL_LVDT_DELAY	RW	xxxx_xx00b	LVDT delay control register
	0x66	BOR_SEL	RW	xxxx_0000b 3	BOR control register
	0x67	UART_BD_EXT	RW	xxxx_xxx0b	UART0/1/2 baud rate configuration extension bit register
	0x68	SPI_IO_SEL	RW	xxxx_xx00b	SPI communication port selection register
	0x69	SPI_MCLK_MOD	RW	xxxx_xxx0b	SPI master mode receiver clock selection register
(	0x6A	BOOT_CMD	RW	0000_0000ь	Program space jump instruction register
(	0x6B	ROM_OFFSET_L	R	0000_0000ь	Address offset of CODE area, low 8 bit
	0x6C	ROM_OFFSET_H	R	0000_0000ь	Address offset of CODE area, high 8 bit

#### Note:

- 1. Registers whose addresses end with 8 or 0 can be bit-operated.
- 2. R: read-only; RW: Read and write.
- 3. 'x': indeterminate, reserved bit.
- 4. Do not write the reserved registers and reserved bits of registers. Otherwise, chip exceptions may occur.
- 5. 1: The reset value is the default value after power-on reset. The global reset value is the factory calibration value, which can be read by referring to 3.1.1.
- 6. 2 : Reset to 1 after power-on. Other resets: Reset to 0 after power-on and 1 after corresponding reset.
- 7. 3: The register is reset after power-on. Other resets do not change the configuration value.

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## 4. Register Summary

## 4.1. SFR register Details

DATAB (80H) PB data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

	Bit number	Bit symbol	Description
	16. 16. 16.	9:23	PB data register, configurable PB group IO port as GPIO
5	7~0		port output level, the read value is the current level state of
	05-01	Υ,	IO port (input) or configured output value (output).

SP (81H) Stack pointer register

Bit number	7	6	5	4	3	2	1	0		
Symbol		SP[7:0]								
R/W		R/W								
Reset value				,	7					

DPL (82H) Data pointer register0 low 8-bit

Bit number	7	6	5	4	3	2	1	0
Symbol				DPL	[7:0]			
R/W	0			√ coR	W			1 com
Reset value	8:33		(1	bya. C	8:33			DYO. CC

DPH (83H) Data pointer register0 high 8-bit

, C	Bit number	7 6 10 5 4 3 2 11 3	
	Symbol	DPH[7:0]	Br
	R/W	R/W	
	Reset value	0	

TIMER3 CFG (84H) TIMER3 configuration register

- (- ) 0 0									
Bit number	7~3	2	1	0					
Symbol	_	TIMER3_CLK_SEL	TIMER3_RLD	TIMER3_EN					
R/W	_	R/W	R/W	R/W					
Reset value	_	0	0	0					

Bit number Bit symbol	Description	abyd. co
pen 01 79:30.	TIMER3 timing clock selection register	W. 10:3
TIMER3_CLK_SELC	1: Select clk_24m/4;	= 1/-1/1
John Dr.	0: Select clk_24m/12.	73.0

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$\overline{(0)}$	70.2	
s pener of 10	.5	TIMER3 auto reload enable register
	TIMER3_RLD	1: Auto reload mode;
		0: Manual reload mode.
		TIMER3 count enable register Configure 1 to start timing, configure 0 to stop timing In manual reload mode, the
0	TIMER3_EN	hardware will automatically clear this register after the
		timing is completed.
		Configure the register during the scan process to re-count.

TIMER3 SET H (85H) TIMER3 count value configuration register, high 8-bits

	Bit number	7	6	5	4	3	2	1	0		
	Symbol	Ω	TIMER3_SET_H[7:0]								
	R/W	R/W. R/W.				R/W					
	Reset value	30.3	100000000000000000000000000000000000000					750 (0) 1 (2.90.2)			
Z			sing. M. J.						111 10.		

	10/1/26	
Bit number	Bit symbol	Description Description
7~0	TIMER3_SET_H[7:0]	TIMER3 count value configuration register, high 8 bits, the register will count again when configured during scanning.

TIMER3 SET L (86H) TIMER3 count value configuration register, low 8 bits

Bit number	7	6	5	4	3	2	1	0	
Symbol		TIMER3_SET_L[7:0]							
R/W		R/W							
Reset value		0							
9.co,	22 2d con 25							g. Corr	

Bit number Bit symbol	Description (0)
TIMER3_SET_L[7:0]	TIMER3 count value configuration register, low 8 bits, the register will re-count when configured during scanning.

PCON(87H) Idle mode 1 select register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	_	IM1_EN
R/W	_	_	_	_	_	_	_	R/W
Reset value	_	_	_	_	_	_	_	0

	Bit number	Bit symbol	Description
	7~1 <sub>2</sub> co		Reserve 2 COM
	20)phg.		Idle Mode I Enable
ď	beneby	IM1 ENI	1; Idle mode 1;
ning		IM1_EN	0. Active mode, automatically cleared after wake-up
			Note: The software delay must be ≥100µsafter wake-up,

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#### otherwise the wake-up function is abnormal

TCON (88H) Timer control register

Bit number	7	6	13/13	84	3	2	177	80
Symbol	TF1	TR1	TF0	TR0	IE1	_	IE0	_
R/W	R/W	R/W	R/W	R/W	R/W		R/W	_
Reset value	0	0	0	0	0	_	0	_

Bit number	Bit symbol	Description
7	TF1	Timer 1 overflow flag bit, set by hardware when Timer1 overflows, or TH0 of Timer0 overflows in mode 3.
6	TR1	Timer1 start enable, when set to1, start Timer1, or start Time0 mode three, TH0 count.
5	TF0	Timer 0 overflow flag, set by hardware when Timer 0 overflows.
4	TR0	Timer0 start enable, set to 1 to start Timer0 counting.
3	IE1	External interrupt 1 flag bit, set by hardware, cleared by software.
1	IE0	Timer 1 overflow flag bit, set by hardware when Timer1 overflows, or TH0 of Timer0 overflows in mode 3.
0, 2		Reserved

TMOD (89H) Timer mode register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	-	M1[	[1:0]	_	-	M0[	[1:0]
R/W	_	_	R/	W	_	_	R/	'W
Reset value	O -	-	0	0	_	-	0	0

	-1-110.		1-510.	-1-210.
	Bit number	Bit symbol	Description	000
Į	7~6, 3~2		Reserved	ing or of Milion
0	1520, PID	\$	Timer I mode select Bit	Jun 2002-01
			00 = Mode  0 - 13 -bit timer	Mar
	5~4	M1[1:0]	01 = Mode 1 - 16-bit timer	
	<i>3</i> ~4	WII[1.0]	10 = Mode  2 - 8 -bit timer with auton	natic reloading of initial
			value	
			11 = Mode  3 - Two  8 - bit timers	
			Timer 0 mode select Bit	
			00 = Mode  0 - 13 -bit timer	
	1 0	M0[1:0]	01 = Mode 1 - 16-bit timer	
	1~0	1~0 M0[1:0]	10 = Mode 2 - 8-bit timer with auton	natic reloading of initial
	abya.	3:33	value (1910)	apya. 128
	762m 1 10	7.70.	11 = Mode 3 - Two 8-bit timers	penies 1 16:30

TL0 (8AH) Timer 0 timer low 8 bits

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	0	9:33							
ď	Symbol	TL0[7:0]							
ning	R/W	R/W							
C	Reset value		0						
	TL1 (8BH) Time	er 1 timer	low 8 bits					_	
	Bit number	7	6	5	4	3	2	1	0
	Symbol				TL1	[7:0]			
	R/W				R/	W			
	Reset value				(	0			
	TH0 (8CH) Tim	er 0 timer	high 8 bits	5					
	Bit number	7	6	5	4	3	2	1	0
	Symbol	0			THO	[7:0]			com
	R/W	6.35			byd. R/	W			pyd. co.
	Reset value	20.		benle	1/0.	9		ben/a	1/9:30
ning	TH1 (8DH) Tim	er 1 timer	high 8 bits	ing. C	1-11,		,	ing. "	
	Bit number	7	6	12/2	B4	3	2	1/1/2-	Bo
	Symbol				TH1	[7:0]			
	R/W		R/W						
	Reset value				(	0			
	SOFT RST (8E	H) Soft re	set register						
	Bit number	7	6	5	4	3	2	1	0
	Symbol	SOFT_RST[7:0]							
	R/W	R/W							
	Reset value	0100							
	abyd. Co.	cho.			byd. Co	c.35			md. Co.
	Bit number	Bit sy	mbol	hen(C	DD 1 10:	Descr	iption	ben(0	16:30
ning	7-72-0	SOFT_RST[7:0] Soft reset register, only when the register value is 0x55, the							

Bit number	Bit symbol	Des	cription	1
75-9-0	SOFT_RST[7:0]	Soft reset register, only when software reset is generated	n the register value is 0x55, the	<u> </u>
1,0		1,0		

DATAC (90H) PC port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0		PC port data register, you can configure the output level when the IO port of the PC group is used as a GPIO port, and the read value is the current level state of the IO port (input) or the configured output value (output)

WDT\_CTRL (91H) WDT timing overflow control register

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	1/10-		\ \ \		// 10-		\ ( )	100
Bit number	7	6	15en	0/4/0.	3	2	2 PEU	110,000
Symbol	_	<u> </u>	11.8V-1		_	WD	T_TIME	SEL
R/W	_		J/772	_	_		R/W	
Reset value	_	_	_	_	_	0	0	0

Bit number	Bit symbol	Description
		WDT timing overflow control register, the timing length is as follows:
2~0	WDT_TIME_SEL	
		0x03: 144ms; 0x04: 288ms; 0x05: 576ms;
-01	Ω	0x06: 1152ms; 0x07: 2304ms;

WDT\_EN (92H) WDT timing enable register

	Bit number	70.3	6	5en (1)	4/6:30.3	3	2	Prop	0/10
5	Symbol			128. W.	WDT_EN		n'i	08. " W	The road
	R/W		7)	1000	R/W			JU 2-01	
	Reset value				0			10	

Bit n	umber	Bit symbol	Description
7	~0	WDT_EN	WDT timer enable configuration register, when the configuration value is 0x55, the watchdog is closed

TIMER2 CFG (93H) TIMER2 configuration register

Bit number	7~4	3	2	1	0
Symbol	0 -	TIMER2_CNT_MOD	TIMER2_CLK_SEL	TIMER2_RLD	TIMER2_EN
R/W	0.25	R/W	R/W	R/W	R/W
Reset value	26.22	0	(0)07 (0,50.55	0	0000

S CONTRACTOR	in	ing of the
Bit number	Bit symbol	Description Description
		TIMER2 counting step mode selection register
3	TIMER2_CNT_MOD	1: The counting step is 65536 clocks
		0: The counting step is one clock
		TIMER2 clock selection register
2	TIMER2_CLK_SEL	1: select XTAL32.768kHz/4MHz
		0: select LIRC
		TIMER2 auto reload enable register
1	TIMER2_RLD	1: Auto reload mode
		0: manual reload mode
		TIMER2 count enable register:
0 1	TIMER2 EN	Configure 1 to start timing, configure 0 to stop timing; In
BILL		manual reload mode, the hardware will automatically
y ·		clear this register after the count is completed, stop

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counting, and in automatic reload mode, the enable register will be maintained after the count is completed, and it will automatically restart; Counting from zero, no matter which mode, if this register is set to 1 during the counting process, it will start counting from zero.

TIMER2 SET H (94H) TIMER2 count value configuration register, high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol		TIMER2_SET_H[7:0]						
R/W		R/W						
Reset value				(	)			

	Bit number	Bit symbol	Description	Opyd. Co.
	Per (0) 1/9	20.2	TIMER2 count value configuration register,	high 8 bits,
Ę	7-0	TIMER2_SET_H[7:0]?	the register will count again when configured	d during
C	052-0		scanning.	7-0,

TIMER2 SET L (95H) TIMER2 count value configuration register, low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol		TIMER2_SET_L[7:0]						
R/W		R/W						
Reset value				(	)			

Bit number	Bit symbol	Description
7~07.00	TIMER2_SET_L[7:0]	TIMER2 count value configuration register, low 8 bits, the register will re-count when configured during scanning

REG ADDR (96H) Secondary bus address configuration register

Bit number	7	6	3	2
Symbol			REG_ADDR	Mrs
R/W			R/W	
Reset value			0	

Bit number	Bit symbol	Description
		Secondary bus Address configuration register: When operating the secondary bus register, it is
5-0 com	REG_ADDR	recommended that RW secondary bus register first, EA = 0, then EA = 1, after the operation is completed, to prevent other interrupts or operations from modifying the secondary bus register Address or data

REG DATA (97H) Second data read and write bus register

V-11-15-0-11-16.	,,			0			0,1,1,0	
Bit number	7	6	2	4	3	2		0

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Symbol	REG_DATA
R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
		Secondary bus data RW register:
7~0	REG_DATA	When RW secondary bus register is recommended, $EA = 0$ first, then $EA = 1$ , after the operation is completed, to
		prevent other interrupts or operations from modifying the address or data of the secondary bus register

	UART2 STAT	$\mathcal{O}$	an		
	Bit number	2.35 7	6,510.00	2.35 5	4 vd. 60
	Symbol	,20.2	UART2_R8	UART2_T8	Den TI2
5	R/W		ing R	R/W	R/W
	Reset value	_	000 B	0	11 20 B
	Bit number	3	2	1	0
	Symbol	RI2	UART2_RO	UART2_F	UART2_P
	R/W	R/W	R/W	R/W	R/W
	Reset value	0	0	0	0

Bit number	Bit symbol	Description				
6	UART2_R8	The 9th data of the receiver, read only				
5	UART2_T8	The 9th data of the transmitter, read only when parity check is enabled				
4BVD	TI2	Send interrupt mark: 1: Send buffer is empty 0: Send buffer is full, software write 0 to clear, write 1 invalid				
3	RI2	Receive interrupt flag:  1: Receive buffer is full  0: Receive buffer is empty, software write 0 to clear, write 1 invalid				
2	UART2_RO	Receive overflow flag: 1: Receive overflow (new data is lost) 0: No overflow, software write 0 to clear, write 1 is invalid				
1	UART2_F	Frame error flag: 1: Frame error detected 0: Frame error not detected, software write 0 to clear, write 1 is invalid				

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Wpyd.	3:33								
pena Wip	,,,,		Parity	error flag:					
	TIAT	DTO D	1: Rec	eiver parit	y error				
	UAI	RT2_P	0: Pari	ity is correc	ct, software	e write 0 t	o clear, wri	te 1 is	
			invalid	•			,		
PWM0_L_L (99	9H) PWM(	low level	control re	gister (low	8-bit)				
Bit number	7	6	5	4	3	2	1	0	
Symbol					_				
R/W	R/W 0								
Reset value									
PWM0_L_H (9	_L_H (9AH) PWM0 low level control register (high 8-bit)								
Bit number	7	6	5	4.00	3	2	1	0,00	
Symbol	0.35			shyd. Co	2.35			PAg. Co	
R/W	20.2		benic	W / R	W		hen(0	1/1:5	
Reset value		· ·	128. 6	1/7// (	)		mg. " V	1111 10	
PWM0_H_L (9	BH) PWM	0 high leve	el control r	egister (lov	w 8-bit)	7	0000	7,	
Bit number	7	6	5	4	3	2	1	0	
Symbol					_				
R/W				R/	W				
Reset value				(	)				
PWM0_H_H (9	·CH) PWM	0 high leve	el control 1	register (hig	gh 8-bit)				
Bit number	7	6	5	4	3	2	1	0	
Symbol					_				
R/W				R/	W			m	
Reset value	0.35			12/9. CO.	2,25			PAIG. CON	
PWM1_L_L (9)	DH) PWM	1 low level	control re	egister (low	8-bit)		100	16.7	
Bit number	7	6	25.3	1 2 4	3	2	ng. 1 N	1 1 0	
Symbol		77	2002-	JI BAD	_	Υ.	000	J/BYD	
R/W				R/	W		Mine	,	
Reset value				(	)				
PWM1_L_H (9	EH) PWM	1 low level	control re	egister (hig	h 8-bit)				
Bit number	7	6	5	4	3	2	1	0	
Symbol					_				
R/W				R/	W				
Reset value				(	)				
PWM1 H L (9	EH) PWM	FH) PWM1 high level control register (low 8-bit)							
Bit number	27	6	5	134CO11	3	2	1	14.00 OXIX	
Symbol	28:33		200	15. J. J. C. C.	2:22		200	D10 16	
R/W			Da. Perra	R/	W		va perio	101,10.	
Reset value		7)	11.00 L	11-0	)	7	ms 12/	11-0	
Mrs			MP2				- Mrs		

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Bit number
Symbol

R/W

200)Dya. 6.5	98:22		20(	Dold C.	8:23		(0)	D/G 16.5		
P2_XH (A0H) N		•	tion pdata	address his	gh 8 bits	۰	VE. PELLO	J. 10.		
Bit number	7	6 🛇	55	40	3	2 🚫	150	100		
Symbol			, Mar				- Mrs	V		
R/W				R/						
Reset value				F	F					
Bit number	Bit symbol									
7~0	P2_XH		_	X @Ri, A be cleared to		n, when op	perating pda	ta area,		
PWM1_H_H (A	1H) PWM	1H) PWM1 high level control register (high 8-bit)								
Bit number	0.32	6	5	204	3	2	1	2/d.0 -0		
Symbol	20. pen (1/20.2)									
$\mathbb{R}/\mathbb{W}$		ping r M R/W ping r M W								
Reset value	0									
PWM2_L_L(A	2H) PWM2	low level	l control re	egister (low	8-bit)					
Bit number	7	6	5	4	3	2	1	0		
Symbol				_						
R/W	R/W									
Reset value				(	)					
PWM2_L_H (A	3H) PWM	2 low leve	l control r	egister (hig	h 8-bit)					
Bit number	7	6	5	4	3	2	1	0		
Symbol	0			an	r			~n		
R/W	0.35			R/	W		_1	-1/9. CO.		
Reset value	20.2		1-07	0,0	9.3		1-00(0)	16.7		
PWM2_H_L (A	4H) PWM	2 high leve	el control	register (lov	v 8-bit)		v6. po. V	W. In.		
Bit number	7	6	(2) 2-1	84 V	3	2	100	80		
Symbol							MI			
R/W				R/	W					
Reset value				(	)					
PWM2_H_H (A	5H) PWM	2 high lev	el control	register (hig	gh 8-bit)					
Bit number	7	6	5	4	3	2	1	0		
Symbol	<u>_</u>									
R/W				R/	W					
Reset value					)					
PWM3 LL(A	6H) PWM3	low level	control re	egister (low	8-bit)			y com		

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R/W



Reset value 0

PWM3 L H (A7H) PWM3 low level control register (high 8-bit)

Bit number	7	6	1972	<b>3</b>	3	2	1/1/2	80		
Symbol										
R/W		- R/W								
Reset value		0								

IEN0(A8H) Interrupt enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	EA	_	-	_	ET1	EX1	ET0	EX0
R/W	R/W	_	-	_	R/W	R/W	R/W	R/W
Reset value	0	_	_	-com	0	0	0	000

	abyu.	(8.5)	aple, (6. ))
	Bit number	Bit symbol	Description Description
5	025-01-01	ζ.	Interrupt enable bit.  0: Mask all interrupts (EA has priority over the respective interrupt enable bits ofthe interrupt sources);
	7	EA	1: The interrupt is turned on. Whether the interrupt request of each interrupt source is allowed or forbidden is determined by the respective enable bit.
	6~4		Reserved
	3	ET1	Timer 1 overflow interrupt enable bit:  0: Disable timer 1 (TF1) to apply for interrupt;  1: Allow TF1 flag bit to request interrupt.
	2	EX1	INT_EXT1 enable bit:  0: Disable INT_EXT1 to apply for interrupt;  1: Allow INT_EXT1 to apply for interrupt.
	1 ET0		Timer 0 overflow interrupt enable bit:  0: Disable timer 0 (TF0) to apply for interrupt;  1: Allow TF0 flag bit to request interrupt.
	0	EX0	INT_EXT0 enable bit:  0: Disable INT_EXT0 to apply for interrupt;  1: Allow INT EXT0 to apply for interrupt.

PWM3\_H\_L (A9H) PWM3 high level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0				
Symbol	PWM3_H_L [7:0]											
R/W	0	R/W										
Reset value	0.35	35 0 35										
(V)	20.2											

PWM3 H H (AAH) PWM3 high level control register (high 8-bit)

( )					0	0 - )		( × ( )			
	Bit number	7	6	0(2) 72-1	PA	3	2	20	75-0	80	

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Symbol	PWM3_H_H[7:0]
R/W	R/W
Reset value	0

SYS CLK CFG (ADH) System clock configuration register

Bit number	7~5	4	3	2	1	0
Symbol	_	IM0_EN	PLL_CLK_SEL PD_SYS_C		PLL_CLK_SEL	
R/W	_	R/W	R/W	R/W	R/W	R/W
Reset value _		0	1	0	0	0

Bit number	Bit symbol	Description	
7~5		Reserved	
4	IM0_EN	Idle mode 0 enable:	, <0
		1: The chip enters the Idle mode 0	01/6:3
		0: The chip exits the Idle mode 0	1/1/1/
3~1	PLL_CLK_SEL	PLL clock divider selection register:	16,52-01
		000/100: 12MHz;	
		001/101: 8MHz;	
		010/110: 4MHz;	
		011/111: 1MHz	
0	PD_SYS_CLK	Core clock enable:	
		0: Turn on the core clock	
		1: Turn off the core clock	

INT\_PE\_STAT\_(AEH) Interrupt status register

	/ 1	8		
Bit number	7	67. com	5	4 1. COL
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	005-00	0 1111	005-08-10
Bit number	3	2	1	0
Symbol	INT_TIMER2_STAT	INT_PWM0_STAT	INT_LCD_STAT	INT_LED_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	INT_PWM1_STAT	PWM1 interrupt status flag, this bit is cleared by writing 0, and it can also be cleared by closing the PWM1 channel 1: Interrupt is valid; 0: Interrupt is invalid
68/1)	INT_TIMER3_STAT	TIMER3 interrupt status flag, this bit is cleared by writing 0, and can also be cleared by writing TIMER3_CFG,

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1: Interrupt is valid; 0: Interrupt is invalid INT08 port interrupt status, this bit is cleared by writing 0, and it can also be cleared by writing INT08 IO SEL=0 INT08\_STAT 5 1: Interrupt is valid 0: Interrupt is invalid WDT interrupt status flag, this bit is cleared by writing 0, and can also be cleared by writing WDT CTRL, INT WDT STAT 4 1: Interrupt is valid 0: Interrupt is invalid TIMER2 interrupt status flag, this bit is cleared by writing 0, and can also be cleared by writing TIMER2 CFG, INT TIMER2 STAT 3 1: Interrupt is valid 0: Interrupt is invalid PWM0 interrupt status flag, this bit is cleared by writing 0, and it can also be cleared by closing the PWM0 INT PWM0 STAT 2 channel 1: Interrupt is valid; 0: Interrupt is invalid LCD interrupt status mark, write 0 to clear this bit, write SCAN START operation can also be cleared, INT LCD STAT 1 1: Interrupt is valid 0: Interrupt is invalid LED interrupt status mark, this bit is cleared by writing 0, and it can also be cleared by writing SCAN START, INT LED STAT 0 1: Interrupt is valid 0: Interrupt is invalid

SCAN START (AFH) LCD, LED scan open register

Bit number	7	6	5	4	3	2	1	0
Symbol		_	_	_	_	_	_	_
R/W	ı	_	_	_	_	_	_	R/W
Reset value	_	_	_	_	_	_	_	0

Bit number	Bit symbol	Description
0		LCD, LED scan on register:
		1: Scan on; 0: Scan off

DATAE (B0H) PE port data register

Dilii	port da	ta register	(1				(4)	
Bit number	7	6	15en (0	14/0	3	2	7 EVICO	7/0/0:2
Symbol	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	RW	R/W

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Reset value 1	1	760 VI/0.	1	1	open a	1	1
205-01-01	D.	me of O -or D		ni,	U.S. 02-0	1-0,	1

Bit number	Bit symbol	Description
7~0		PE data register, you can configure the output level of PE group IO port as GPIO port, the read value is the current level state of IO port (input) or configure output value (output).

DP\_CON (B1H) LCD, LED control register
Bit number 7 6 5 4 3 2 1 0

Symbol DUTY\_SEL **DPSEL** SCAN\_MODE COM\_MOD IO ON R/WR/W R/W R/W R/W R/W Reset value 0 0 0 0.0 0 ~00 0

pen(0) 1/9	,30,	ben 0, 10:30.
Bit number	Bit symbol	Description in S
6 BAT	IO_ON	LCD/LED scanning corresponds to the total control bit of all IO ports: 0: Close IO; 1: Open IO
5~3	DUTY_SEL	LED dot matrix drive mode dot matrix selection configuration register  Bit[1:0]: 00: 4x5 dot matrix; 01: 5x6 dot matrix  10: 6x7 dot matrix; 11: 7x8 dot matrix  Bit [2]: 0: LED0 as the starting port  1: 4x5 dot matrix-Enable with LED3 (as the starting port)  LED row and column drive mode single SEG port conduction duty cycle configuration register: 0: 1/8 duty cycle 1: 2/8 duty cycle 2: 3/8 duty cycle 3: 4/8 duty cycle 4: 5/8 duty cycle 5: 6/8 duty cycle 6: 7/8 duty cycle 7: 8/8 duty cycle CD drive mode duty cycle configuration register 000: 1/4 duty cycle, 1/3 bias (4 COM X 16/24 SEG)  COM port: COM0-3, SEG port: SEG0-23 001: 1/8 duty cycle, 1/4 bias (8 COM X 16/24SEG)  COM port: COM0-7, SEG port: SEG0-23 010: 1/4 duty cycle, 1/3 bias (4 COM X 20/28 SEG)

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COM port: COM0-3, SEG port: SEG0-23, COM4-7 shared as SEG24-27 011: 1/5 duty cycle, 1/3 bias (5 COM X 19/27 SEG) COM port: COM0-4, SEG port: SEG0-23, COM5-7 shared as SEG25-27 100: 1/6 duty cycle, 1/3 bias (6 COM X 18/26 SEG) COM: COM0-5, SEG: SEG0 -23, COM6-7 shared as SEG26-SEG27 101: 1/6 duty cycle, 1/4 bias (6 COM X 18/26 SEG) COM port: COM0-5 SEG port: SEG0-23, COM6-7 shared as SEG26-SEG27 Others: 1/4 duty cycle, 1/3 bias (4 COM X 16/24 SEG) COM: COM0-3, SEG: SEG0-23 LCD, LED selection control bit **DPSEL** 0: Select LCD driver, LED driver is invalid 2 1: Select LED driver, LCD driver is invalid LCD, LED scan mode configuration 1: Cycle scan mode SCAN MODE 1 0: Interrupt scan mode High-current IO port driver enable 1: The COM port function is locked and works as a highcurrent IO port; 0: The COM port function is not locked and can be COM MOD 0 configured as other functions; When the COM port function is locked to the high-current IO port, configure the GPIO register output drive timing, LED/LCD scan configuration is invalid

DP MODE (B2H) LCD, LED mode register

Bit number	7	6	5	4	3	2	1	0
Symbol	LED_MOD	LCD_0	CKSEL	LCD_RSEL	LCD_I	FCSEL	LCD_1	RMOD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description			
		LED drive mode selection register			
7	LED_MOD	1: Serial dot matrix scanning			
		0: Row and column matrix scan			
6~5	LCD_CKSEL	LCD clock selection register 10/11: select RC1M			

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01: Select XTAL 00: Select LIRC32kHz Charge time control bit 00: 1/8 COM of LCD period; 01: 1/16 COM of LCD period; LCD FCSEL 3~2 10: 1/32 COM of LCD period; 11: 1/64 COM of LCD period LCD bias resistance selection control bit LCD RSEL 0: The sum of LCD bias resistance is 225k; 4 1: The sum of LCD bias resistance is 900k Drive mode selection bit 00: Traditional resistance mode (slow charging mode), the total bias resistance is 225k/900k, when LCD RSEL = 0, the total LCD bias resistance is 225K, when LCD RSEL = 1, the total LCD bias resistance is 900K LCD RMOD 1~0 01: Traditional resistance mode (fast charging mode), the total bias resistance is 60k 10/11: Fast and slow charging automatic switching mode, the total bias resistance is automatically switched between 60k and 225k/900k

SCAN WIDTH (B3H) LED period configuration register

Bit nu	mber	7	6	5	4	3	2	1	0		
Sym	ıbol										
R/	$\mathbf{w}_{\lambda}$	Ur.	1 CR/W								
Reset	value (	18:23		20070. (20:5)					20) Jan 19		
perio	MA	,,,		pen of 10.							

THU TO		
Bit number	Bit symbol	Description this Description
Mrs. D		Under LED matrix drive mode, corresponding to the scan time of
		a single COM port
		In the LED dot matrix drive mode, the corresponding single lamp
		lighting time configuration register-the first segment of the lamp
		cycle configuration: period=(scan_width+1)*16us, the support configuration range is 0.016~4.096ms;
7~0		When on-time 1<0n-time 2, the scan time of this group is on-time
		2.In LCD drive mode, the corresponding single COM port scan
		time:
		period=(scan_width+1)*64us, support configuration range
		0.064~4.096ms, high two digits Reserved
BI	)	Note: In this mode, this register is only applicable to the LCD
y -		selection clock CLK_1M mode, the slowest LCD frame rate in

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other clock modes is 64Hz (8\*24)

LED2 WIDTH (B4H) LED dot matrix drive mode cycle configuration register

	(D 111) Di	(B 111) EBB dot matin an confidence of the configuration register						
Bit number	7	6	3 48	3	2	1 30		
Symbol		_						
R/W		R/W						
Reset value				0				

Bit number	Bit symbol	Description
7~0		In the LED dot matrix drive mode, the corresponding single lamp lighting time configuration register-the second stage of lamp cycle configuration period=(led2_width+1)*16us  Note: This register is only applicable to LED dot matrix
		drive mode: when the on time 1 is greater than the on time 2, the scan time of this group is on time 1.

SPI CFG1 (B5H) SPI control register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	RX_IE	SPI_EN	TX_IE	MSTR	CPOL	СРНА	LSBFE	CS_N
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	1	0	1	0	1

Bit number	Bit symbol	Description
7	RX_IE	Receive enable- SPI receive buffer is full (SPRF) interrupt enable 1: Interrupt is valid; 0: Interrupt is disabled (using polling)
6	SPI_EN	SPI enable: 1: module enable open; 0: module enable close
5	TX_IE	Transmit enable - SPI transmit buffer empty (SPTEF) interrupt enable 1: Interrupt is valid; 0: Interrupt is disabled (using polling)
4	MSTR	Master-slave mode selection  1: Master mode;  0: Slave mode
3	CPOL	SCLK active level selection 1: Active low; 0: Active high
2	СРНА	SCLK phase selection  1: Send data at the first valid clock edge  0: Sample data at the first valid clock edge
1	LSBFE	LSB first (shifter direction)  1: SPI serial data transmission starts from the lowest bit

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0: SPI serial data transmission starts from the highest bit
Chip select signal:
0: Pull down CS
1: Pull up CS

SPI CFG2 (B6H) SPI control register 2

Bit number	7	6	5	4
Symbol	_	FEEDBACK	HSPEED_START	HALF_FUPLEX
R/W	_	R/W	R/W	R/W
Reset value	_	0	0	1
Bit number	3	2	1	0
Symbol	BIDIR_SELECT	c 01	SPR	com
R/W	R/W	R/W	R/W	R/W
Reset value	1	2620 1/0	0	Den On Min
		ing. M.VI	χ.	ing Mall

	Reset value	1	7600 V // 2 0 7600 V // 1/
ning	3 - 11-11		ing - M. J. sing - M. J.
7	Bit number	Bit symbol	Description Description
	6	FEEDBACK	Send the received data to the master\slave  1: Send the received data to the master\slave  0: Send the data written by MCU to the master\slave
	5	HSPEED_START	The high-speed SPI communication mode is turned on and the hardware is automatically pulled down after the work is completed  1: High-speed SPI communication mode is on  0: High-speed SPI communication mode is off.  In high-speed SPI mode, whether in slave or master mode, the chip select signal cannot be pulled high, which will
	4	HALF_FUPLEX	cause the data sent by SPI to be lost  Half-duplex mode selection:  1: Select half-duplex mode;  0: Select full-duplex mode
	3	BIDIR_SELECT	Half-duplex mode, transmission and reception direction selection 1: Send; 0: Receive
	2~0	SPR	SPI baud rate coefficient, up to 2MHz:  000: spi_clk/2; 001: spi_clk /4;  010: spi_clk/6; 011: spi_clk /8;  100: spi_clk/10; 101: spi_clk /12;  110: spi_clk/14; 111: spi_clk /16;

IPLO (B8H) Interrupt priority register0

	H DO (DOLL) III	on upt prio	ity registere	1)-					_
0	Bit number	7	6 ping	5	1-4	3	2	ing is	
1	Symbol	_	_ 1 ^	0.17	Bir	PT1	PX2	PT0	PX0

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	1/10-							
Den R/W		_	_	_	R/W	R/W	R/W	R/W
Reset value	_	_	_	_	0	0	0	

Bit number	Bit symbol	Description
7~4	_	Reserved
	DT1	TF1 (Timer1 interrupt) priority selection bit.
3	PT1	0: Timer1 is low priority; 1: Timer1 is 1high priority
_	DV2	INT_EXT1 interrupt priority selection bit.
2	2 PX2	0: INT_EXT1 is low priority; 1: INT_EXT1 is high priority
	PT0	TF0 (Timer0 interrupt) priority selection bit.
1	PIU	0: Timer0 is low priority; 1: Timer0 is high priority
1 2 d. co,	PX0	INT_EXT0 interrupt priority selection bit.
000	36.35 PAU	0: INT_EXT is low priority; 1: INT_EXT is high priority

	00) 1 (1) PX0		0: INT_EXT is low priority; 1: INT_EXT is high priority				
٠٠٥٥	DP_CON1 (B9I	H) LCD contrast con	figuration register		" " per of 1/1/10.2		
DILL	Bit number	7	11110056 1210	5	1110014		
	Symbol	_	TRI_COM_INV	MATRIX_MOD	PD_LCD_POWER		
	R/W		R/W	R/W	R/W		
			0	0	0		
	Bit number	3	2	1	0		
	Symbol		V	OL			
	R/W R/W		R/W	R/W	R/W		
	Reset value	0	0	0	0		

Bit number	Bit symbol	Description 2 COM
025.06B/D	TRI_COM_INV	LED matrix 4*4 mode COM port reverse selection register. In 4*4 mode,  1: Output high when COM is selected  0: Output low when COM is selected
5	MATRIX_MOD	LED matrix 4*4 mode selection register:  1: Select 4*4 mode, LED0~LED3 correspond,  COM0~COM3 port selection, LED4~LED7 correspond,  SEG0~SEG3 port selection;
4	PD_LCD_POWER	0: Do not select 4*4 mode  LCD contrast control enable bit:  0: Turn off LCD contrast control  1: Turn on LCD contrast control
3~0	VOL	LCD contrast control bit: 0000: VLCD = 0.53VDD; 0001: VLCD = 0.56VDD; 0010: VLCD = 0.59VDD; 0011: VLCD = 0.63VDD; 0100: VLCD = 0.66VDD; 0101: VLCD = 0.69VDD;

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(1) (1) (1) (1) (1) (1) (1) (1) (1) (1)	
205010110.30	0110: VLCD = 0.72VDD; 0111: VLCD = 0.75VDD; 1000: VLCD = 0.78VDD; 1001: VLCD = 0.81VDD;
March	1010: VLCD = 0.84VDD; 1011: VLCD = 0.88VDD;
	1100: VLCD = 0.91VDD; 1101: VLCD = 0.94VDD;
	1110: VLCD = 0.97VDD; 1111: VLCD = 1.00VDD

UART2\_BDL (BAH) UART2 baud rate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	UART2_BDL[7:0]							
R/W	R/W							
Reset value	0							

	· ^	77	2017
	Bit number	Bit symbol	Description
	pen(0) 1/2	20.2	Baud rate control register, the lower 8 bits of the baud rate
Z	2 W-11	, i	modulus divisor register
(	0520		UART_BD_EXT=0,
			Baud_Mod = {UART2_BDH[1:0], UART2_BDL};
	7~0	 	UART_BD_EXT=1,
	/~0	JAK12 BDL[/:0]	Baud_Mod= {UART2_BD_ADD[1:0], UART2_BDH[1:0],
			UART2_BDL};
			When Baud_Mod=0, the baud rate clock is not generated;
			When Baud_Mod>1,
			the baud rate = BUSCLK/(16xBaud_Mod)

UART2\_CON1 (BBH) UART2 mode control register 1

Bit number	7	6 <sub>2</sub> C	om 5	$4 \times com$
Symbol	8:22	UART2_ENABLE	RECEIVE_ENABLE	MULTI_MODE
R/W	_	R/W	R/W	P.W.
Reset value	_	DILLE OF O	0 11	0.00
Bit number	3	2	1	
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART2_ENABLE	Module enable 1: Module is enabled; 0: Module is turned off
5	RECEIVE_ENABLE	Receiver enable 1: Receiver is turned on; 0: Receiver is turned off
4	MULTI_MODE	Multiprocessor communication mode

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1: Mode is enabled; 0: Mode is disabled Stop bit width selection STOP\_MODE 1: 2 bits; 3 0: 1 bit Data mode selection 1: 9-bit mode; DATA\_MODE 2 0: 8-bit mode Parity check enable PARITY\_EN 1: Parity check is enabled; 1 0: Parity check is disabled Parity check selection 1: Odd check; PARITY SEL 0: Even check

UART IO CTRL1 (BCH) UART pin enable register

1641131 _192 0 111	Er (Berr) er ner pr	11 011001111111111111111111111111111111			
Bit number	7	6	5	4	
Symbol	-	-	UART2_RXD_ DIASB	UART2_TXD_ DIASB	
R/W	_	_	R/W	R/W	
Reset value	0	0	0	0	
Bit number	3	2	1	0	
Symbol	UART1_RXD_ DIASB	UART1_TXD_ DIASB	UART0_RXD_ DIASB	UART0_TXD_ DIASB	
R/W	R/W	R/W	R/W	R/W	
Reset value 0		(a)	8:55	abyer (in	
per of		Per Ul 10.		- Par 1/1/00	

· Jan						
Bit number	Bit symbol	Description Mills Description				
Mrs. P	(	UART2 RXD port disabled				
5	UART2_RXD_DIASB	0: RXD pin is enabled;				
		1: RXD pin is disabled				
		UART2 TXD port disable				
4	UART2_TXD_DIASB 0: TXD pin is enabled;					
	1: TXD pin is disabled					
		UART1 RXD port disabled				
3	UART1_RXD_DIASB	0: RXD pin is enabled;				
		1: RXD pin is disabled				
	UART1 TXD port disable					
2	UART1_TXD_DIASB	0: TXD pin is enabled;				
[Va		1: TXD pin is disabled				
1	UARTO_RXD_DIASB	UART0 RXD port disabled				

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	(0)	.50.33	
Υ.	pena Wil	7.50	0: RXD pin is enabled;
ح	05.01-0		1: RXD pin is disabled
7	777		UART0 TXD port disable
	0	UART0_TXD_DIASB	0: TXD pin is enabled;
			1: TXD pin is disabled

UART2 BUF (BDH) UART2 port data register

Bit number	7	6	5	4	3	2	1	0
Symbol		UART2_BUF[7:0]						
R/W		R/W						
Reset value	FF							

	20 <sup>4</sup>	Ω	om	
Bi	t number	Bit symbol	Description	?
her	10,10	20.2	UART2 data register:	7.
S. C.	7-0	UART2_BUF[7:0]	Reads and returns the content of read-only receive data	
00/7	)-0	<i>y</i>	buffer, writes into write-only transmit data buffer	

SPI\_STATE (BEH) SPI status flag register

Bit number	7~3	2	1	0
Symbol	_	SPRF	OVERFLOW_RX	SPTEF
R/W	_	R/W	R/W	R/W
Reset value	_	0	0	1

Bit number	Bit symbol	Description		
7~3		Reserved		
		Read buffer full mark, software write 0 to clear		
2	SPRF	0: In the receive data buffer, no data is available;		
$\Omega_{\rm re}$		1: In the receive data buffer, there is data		
RID		In the normal communication mode, when the receiving		
		overflow is caused by not reading in time,		
		OVERFLOW_RX=1, the signal does not generate an		
1	OVERFLOW_RX	interrupt, only the mark In high-speed SPI communication		
1		mode, it is invalid (when the number of received data is		
		equal to the configured {SPI_NUM_H, SPI_NUM_L}, the		
		work will end, SPRF will be set, and a full interrupt will be generated).		
		Send buffer empty mark, write into SPID hardware to clear		
		automatically. In the SPI idle state, the first data written to		
	CDTEE	SPID will be directly stored in the shift register, and the		
0	SPTEF	second data written will be loaded into the transmit buffer,		
		and SPTEF will be automatically pulled low.		
		1: The data cache is empty, data can be written;		

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0: The data cache is not empty
--------------------------------

SPI\_SPID (BFH) SPI port data register

Bit number	7	6	13/2	84	3	2	177	30
Symbol	SPI_SPID[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SPI_SPID[7:0]	SPID reading this register will return the data read from the receive data buffer rx_reg. Writing to this register will write data into the transmit data buffer tx_reg.  Data should not be written into the transmit data buffer, unless the SPI transmit buffer empty flag (SPTEF) is set, indicating that there is a certain space in the transmit buffer to queue new transmit bytes.  After setting the SPRF and before completing another transmission, you can read data from the SPID at any time. If the data is not read from the receive data buffer before the end of the new transmission, the receive overflow will result and the newly transmitted data will be lost.

DATAF (C0H) PF port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	8:21	1	1 0	by I c.	8.51	1	1,0	010.7

· VI UI						
Bit number	Bit symbol	Description Description				
		PF data register, you can configure the output level of the PF				
7~0		group IO port as a GPIO port, and the read value is the				
		current level state of the IO port (input) or the configured				
		output value (output)				

ADC\_SPT (C1H) ADC sampling time configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC SPT[7:0]							
R/W	R/W							
Reset value	7			1 con	)			1 com

Bit number	Bit symbol	ben to be Description ben to be Description
025-7-0870	ADC_SPT[7:0]	ADC sampling time configuration register  Sampling time: t1= (ADC_SPT+1)*4* TADCK

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UART IO CTRL (C2H) UART TXD/RXD pin exchange register

Bit number	7~3	2ning of	1	ning of all -01		
Symbol	ı	UART2_PAD_CHANGE	UART1_PAD_CHANGE	UARTO_PAD_CHANGE		
R/W	ı	R/W	R/W	R/W		
Reset value	ı	0	0	0		

Bit number	Bit symbol	Description
	HADTO DAD CHANCE	UART2 TXD/RXD pin exchange
2	UART2_PAD_CHANGE	1: Pin exchange; 0: Pin not exchange
	HADTI DAD CHANCE	UART1 TXD/RXD pin exchange
1	UART1_PAD_CHANGE	1: Pin exchange; 0: Pin not exchange
Javd. C	THE PAR CHANCE	UARTO TXD/RXD pin exchange
1262 (10) 1 /	UART0_PAD_CHANGE	1: Pin exchange; 0: Pin not exchange

ADC SCAN CFG (C3H) ADC scan configuration register

		(	, , , , , , ,				
0	Bit number	7	6	5 4 3	2	1	03-11 03-11
	Symbol	_		ADC_ADDR			ADC_START
	R/W	_		R/W			R/W
	Reset value			0			0

Bit number	Bit symbol	Description			
		ADC channel address selection register 000000: Corresponding to ADC0; 000001: Corresponding to ADC1;			
6~1	ADC_ADDR	101010: Corresponding to ADC42;			
Tra		101011: Corresponding to ADC43;			
P),	,	101100: ADC44_VREF. others: Reserved			
		ADC scan open register:			
		0: ADC module does not scan;			
		1: ADC module starts to scan			
		ADC_START is set from 0 to 1, ADC starts to scan, after			
0	ADC_START	scanning once, ADC_START hardware is automatically set			
		to 0, corresponding to the ADC interrupt flag bit. The ADC			
		interrupt flag bit needs to be cleared by software.			
abyd. co	28:32 pw	Note: ADC_START is not allowed to be configured during scanning			

ADCCKC (C4H) ADC clock and filter configuration register

	-)			
Bit number	7	ning. of 61-111	5 2118 25 (4)	
Symbol	FILTER_SEL	SAMBG	SAMDEL	

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	7/10-		7110-	
R/W	R/W	R/W	R/W	DE R/W
Reset value	0	mis of a large	0	me of o
Bit number	3	2 3	1	0 8
Symbol	ADC	CCKV	A	DCK
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	FILTER_SEL	ADC filter selection 0: No RC filter added; 1: RC filter added.
6	SAMBG	Sampling timing and comparison timing interval selection 0: interval of 0 Tadck; 1: interval of 1 Tadck
5~4	SAMDEL	Sampling delay time selection 00: 0*Tadck; 01: 2*Tadck; 10: 4*Tadck; 11: 8*Tadck
3~2	ADCCKV	ADC comparator offset cancellation analog input clock 00: 12MHz; 01: 8MHz; 10: 4MHz; 11: 2MHz
1~0	ADCK	ADC clock 00: 8MHz; 01: 6MHz; 10: 4MHz; 11: 3MHz

ADC\_RDATAH (C5H) ADC scan result register high 4 bits

Bit number	7	6	5	4	3	2	Mrs	0
Symbol	_	_	_	-	ADC_RDATAH [3:0]			
R/W	_	_	_	-	R			
Reset value	_	_	_	_	0			

ADC RDATAL (C6H) ADC scan result register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_RDATAL[7:0]							
R/W	R							
Reset value							1 com	

ion in the second	Bit number	Bit symbol	Description bent of 10.3
	3-0	ADC_RDATAH[3:0]	ADC scan result register, high 4bit
	7~0	ADC_RDATAL[7:0]	ADC scan result register, low 8Bit

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EXINT\_STAT (C7H) External interrupt status register

Bit number	7	ing of a long	5	me of A -01
Symbol	INT07_STAT	INT06_STAT	INT05_STAT	INT04_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT03_STAT	INT02_STAT	INT01_STAT	INT00_STAT
R/W	R/W R/W		R/W	R/W
Reset value	0	0	0	0

	Bit number	Bit symbol	Description
5	ben@byd. 0	INT0x_STAT (x=7~0)	INT0x port interrupt status, this bit is cleared by writing 0, and it can also be cleared by writing INT0x_IQ_SEL=0, 1: Interrupt is valid; 0: Interrupt is invalid

DATAG (C8H) PG port data register

Bit number	7	6	5	1	2	2		0
Bit ilullibei	/	U	3	4	3		1	U
Symbol	_	_	_	_	PG3	PG2	PG1	PG0
R/W	_	_	_	_	R/W	R/W	R/W	R/W
Reset value	_	_	_	_	1	1	1	1

	Bit number	Bit symbol	Description
3~0			PG data register, you can configure the output level when
	~~	0	the IO port of the PG group is used as a GPIO port, and the
174.00			read value is the current level state of the IO port (input) or
	(a)	26.33	the configured output value (output).

SPROG ADDR H (CEH) Address control register

Bit number	7	6	505-01-410	3	2	Mrs 1 2 1 20 D		
Symbol			No.	_				
R/W		R/W						
Reset value		0						

Bit number	Bit symbol	Description
		Bit[7:6]: block selection when reading data indirectly
		10: Select system block, multiplex to read data indirectly (SPROG_CMD=0x88)
7~0		01: Select information block, multiplexed to read data indirectly (SPROG_CMD=0x88);
Ova		11/00: invalid;
Rin		In non-Flash_Boot upgrade mode: Bit[6:2]: DATA area (0xFC00~0xFFFF) selection enable

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00000: Select DATA area (0xFC00~0xFFFF), 1024Bytes Other: invalid

1. DATA area (0xFC00~0xFFFF):
config {SPROG\_ADDR\_H[1:0], SPROG\_ADDR\_L[7:0]}

2. When SPROG\_ADDR\_H[2]=1, select NVR4:
config {SPROG\_ADDR\_H[0], SPROG\_ADDR\_L[7:0]}

3. When SPROG\_ADDR\_H[2]=0, select NVR3:
config {SPROG\_ADDR\_H[0], SPROG\_ADDR\_L[7:0]}
Note: In Flash\_Boot upgrade mode,
{SPROG\_ADDR\_H, SPROG\_ADDR\_L} multiplexing all space addresses of CODE

SPROG ADDR L(CFH) Address control register low 8 bits

Bit number	50.7	6	5 4 3 3	2	10000
Symbol		,	SPROG_ADDR_L[7:0	]	ve. pe. V. W. In.
R/W		Υ.	R/W		000
Reset value			0		Mac

Bit number	Bit symbol	Description
7~0	SPROG_ADDR_L[7:0]	The lower 8 bits of the address

PSW (D0H) Program status word register

Bit number	7	6	5	4	3	2	1	0
Symbol	CY	AC	F0	RS[	1:0]	OV	F1	P
R/W	R/W	R/W	R/W	R/	W	R/W	R/W	R/W
Reset value	0	0	0	10 COZ	<b>Q</b>	0	0	1900m
(a) (b)	78:33		(	7. 1996	8:33		(1)	pole

7/0	30,	
Bit number	Bit symbol	Description Description
0250 BIN	CY	Carry flag  0: In arithmetic or logic operation, no carry or borrow occurs  1: In arithmetic or logic operation, a carry or borrow occurs
		Auxiliary carry flag
6	AC	0: In arithmetic logic operation, no auxiliary carry or borrow occurs  1: In arithmetic logic operation, an auxiliary carry or borrow
5	F0	0 flag bit. Generic labels available to users.
3	10	Working register group selection:
4~3 BYD	RS[1:0]	Select a valid working register group:  RS[1:0] Bank IRAM Area  00 0 0x00-0x07;  01 1 0x08-0x0F;

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O(2)	28.33						
pena Wip	,50	10 2 0x10-0x17;					
205-01-01		11 3 0x18-0x1F.					
2	OV	Overflow flag 0: No overflow occurred; 1: Overflow occurred					
1	F1	1 flag.Generic labels available to users.					
0	Р	Parity bit  0: The number of digits with value 1 in accumulator A is even;  1: The number of digits with a value of 1 in the accumulator A is an odd number.					

SPROG\_DATA(D1H)Write data register

Bit number	7	6	5	4_00	3	2	1	0,00
Symbol	0.35			And. Co.	25.0			Mg. Co.
R/W	20.2		ben(	R	W		Den a	6.7
Reset value			108.	1.01	0	, i	12. N	111110
Bit number	Bit sy	mbol	1052	BAD	Desci	ription	0000	BAD
7~0	_	_	data to be	written			M	

SPROG CMD(D2H) Command register

Bit number	7	6	5	4	3	2	1	0
Symbol		_						
R/W		R/W						
Reset value		0						

Bit number	Bit symbol	Description
ben abyd. co		Write 0x96: page erase Write 0x69: byte burn Write 0x88: read data indirectly; When continuously writing data 0x12, 0x34, 0x56, 0x78, 0x9A, enter the Flash Boot upgrade mode; When continuously writing data 0xFE, 0xDC, 0xBA, 0x98, 0x76, exit the Flash Boot upgrade mode When CFG_BOOT_SEL = 3 or the program is running in a non-BOOT space, the BOOT upgrade mode cannot be entered.

SPROG TIM(D3H) Erase time control register

Bit number	7	6	5	4	3	2	1	0
Symbol O	D 25-	_	_	1-com	<u> </u>	_	_	1 com
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	Joen C	1/0	1	1	10 V	W 1/0.2

Bit number Bit symbol	Description
-----------------------	-------------

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	' \\	
ben 7~5/	SPROG_TIM[7:5]	Byte write fixed time is 23.5us
025.01.00		Erase time configuration SPROG_TIM[4:0]=0~31 When the selected address is 0xFC00~0xFFFF: When SPROG_TIM[4:0]=0~9,
4~0	SPROG_TIM[4:0]	Erase Time = 1.13 + SPROG_TIM[4:0] (ms); When SPROG_TIM[4:0]=10~31, Erase time = 9.13 (ms)
		When selecting NVR3/4 or BOOT upgrade mode: When SPROG_TIM[4:0]=0~9,
		Erase Time=0.57+0.5* SPROG_TIM[4:0] (ms);
and.cox	0.35	When SPROG_TIM[4:0]=10~31, Erase time=4.57(ms)

SPROG\_RDATA (D4H) Information block/system block data read register

Bit number	7	6	5 1 14	3	2 1 0
Symbol			MILOND S-UI BYD.		MI ON THE BYD
R/W			R		
Reset value			0		

Bit number	Bit symbol	Description
7~0		Indirectly read the data in the information block/system block

INT POBO STAT (D5H) LVDT boost/buck interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	77	-	_		<u> </u>	DIII.	INT_PO_STAT	INT_BO_STAT
R/W	8:37		_	-200	16/20.	.18:2:	R/W	RW
Reset value	<u>-</u>	_	~	perio	0//	<i></i>	0	pen of jo.

JULY 2 11 F.		
Bit number	Bit symbol	Description
		LVDT boost interrupt status.
1	INT_PO_STAT	1: Boost interrupt is valid;
		0: Boost interrupt is invalid.
		LVDT buck interrupt status.
0	INT_BO_STAT	1: The buck interrupt is valid;
		0: The buck interrupt is invalid

UART1\_BDL (D6H) UART1 baud rate control register

	Bit number	7	6	5	4 <sub>C</sub> OM	3	2	1	1 0 om
	Symbol	7)		(d	UART1_B	DL[7:0]			oyd. co
	hen R/W			henly	R/V	V		hen/a	1/0:3
5	Reset value		7	11.8. 02 V	0		ni	U.S. 25 V	17/1
	VIII O III			- (1, 1, 1, 1,	0			0,1.4.0	

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Bit number	Bit symbol	Description benta 110.3
2022-01-0	, p	Baud rate control register  Baud rate modulus divisor register, low 8 bits
		UART_BD_EXT=0, Baud Mod = {UART1 BDH[1:0], UART1 BDL};
		UART_BD_EXT=1,
7~0	UART1_BDL[7:0]	Baud_Mod= {UART1_BD_ADD[1:0], UART1_BDH[1:0], UART1_BDL};
		When Baud_Mod=0, the baud rate clock will not be
		generated. When Baud Mod≥1,
and. con	0.35	baud rate = BUSCLK/(16xBaud_Mod)

UARTI\_CON1 (D7H) UART1 mode control register

37414	(3 /11) 0111111		11.5	4 0110 1 1/1		
Bit number	7	ing. 6 1 01	5	2.00.4		
Symbol	_ UARTI_ENABLE RECEIVE_I		RECEIVE_ENABLE	MULTI_MODE		
R/W	_	R/W	R/W	R/W		
Reset value	_	0	0	0		
Bit number	3	2	1	0		
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL		
R/W	R/W	R/W	R/W	R/W		
Reset value	value 0 0		0	0		

Bit number	Bit symbol	Description
2008/d. co	UART1_ENABLE	Module enable  1: Module enable, 0: Module close
ben 5pl	RECEIVE_ENABLE	Receiver enable 1: Receiver is on, 0: Receiver is off
4	MULTI_MODE	Multi -processor communication mode  1: Mode enable, 0: Mode disable
3	STOP_MODE	Stop bit width selection 1: 2 bits, 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode, 0: 8-bit mode
1	PARITY_EN	Parity check enable 1: Parity check is enabled, 0: Parity check is disabled
0 d. co	PARITY_SEL	Parity check selection  1: Odd check, 0: Even check

DATAH (D8H) PH port data register

7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	P	1 - 8 - 5 - 1 - 1	()0					
Bit number	7	6	108.5 C	4	3	2 🐧	08. T U	0
Symbol	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0

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(10)	7(100						
Den R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W R/W
Reset value	1	1	1	1	1	1	1

Bit number	Bit symbol	Description			
7~0		PH data register, can configure the output level of PH group			
		IO port as GPIO port, the read value is the current level sta			
		of IO port (input) or configure output value (output)			

UART1\_CON2 (D9H) UART1 mode control register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	UART1_	BD_ADD	TX_EMPTY_IE	MPTY_IE RX_FULL_IE		I_BDH
R/W		R/W	R/W	R/W	R/W	R/	W	
Reset value	1 (0) - 2 -		0	20.35	1	0	19.0	

	12672 V 10	•	Per of Mis
Z	Bit number	Bit symbol	Description ing
(	1520, BAD	\\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\	The upper 2 bits of the baud rate modulus divisor register.
	5~4	UART1_BD_ADD	(it is determined by UART_BD_EXT whether to take
			effect)
			Send interrupt enable
	3	TX_EMPTY_IE	1: Interrupt enable;
			0: Interrupt disable (used in polling mode)
			Receive interrupt enable
	2	RX_FULL_IE	1: Interrupt enable;
	·		0: Interrupt disable (used in polling mode)
	1~0>	UART1 BDH	Baud rate modulus divisor register, high 2 bits

UARTI STATE (DAH) UART1 status flag register

Bit number	7	20. per 6 11 10	5	ng. berry
Symbol		UARTI_R8	UART1_T8	TII
R/W	_	R	R/W	R/W
Reset value	_	0	0	0
Bit number	3	2	1	0
Symbol	RI1	UART1_RO	UART1_F	UART1_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

	Bit number	Bit symbol	Description
	6 \ COO UART1_R8		The 9th data of the receiver, read only
\ \	ben Obyd.	UART1_T8	The 9th data of the transmitter, read only when parity check is enabled
Ö	4 TI1		Send interrupt mark:
4 9		111	1: The sending buffer is empty

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(0)	70.3	
per 01 11	, ,	0: Send buffer is full, software write 0 to clear, write 1 is invalid
		Receive interrupt mark:
3	D11	1: The receive buffer is full
3	RI1	0: The receive buffer is empty, software writes 0 to clear, writes 1 is invalid
		Receive overflow flag:
2	UART1_RO	1: Receive overflow (new data is lost)
		0: No overflow, software write 0 to clear, write 1 is invalid
	UART1_F	Frame error flag
1		1: Frame error detected
1		0: No frame error is detected, software writes 0 to clear, write 1 is invalid
	UART1_P	Parity error flag:
		1: Receiver parity error
0		0: The parity check is correct, the software writes 0 to clear, and writes 1 is invalid

UART1\_BUF (DBH) UART1 port data register

Bit number	7	6	5	4	3	2	1	0
Symbol		_						
R/W		R/W						
Reset value	FF							

	Bit number	Bit sy	mbol		λ. Ο	Desci	ription		λ. 60	(
3	pen (350)	-	-	4 07 1	~ \ \\\.•		e read-only ly transmit	4 07 1		00
7	UARTO BDL (I	OCH) UAI	RT0 baud	rate contro	register		77	11802	120	
7	Bit number	7	6	5	4	3	2	Mrs	0	
	Symbol				UART0_1	BDL[7:0]		·		
	R/W	R/W								
	Reset value				(	)				

Bit number	Bit symbol	Description
		Baud rate control register,
		Baud rate modulus divisor register, low 8 bits
		UART_BD_EXT=0,
7~0	UART0_BDL[7:0]	Baud_Mod = {UART0_BDH[1:0], UART0_BDL};
		UART_BD_EXT=1,
BAD		Baud_Mod= {UART0_BD_ADD[1:0], UART0_BDH[1:0], UART0_BDL};

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When Baud\_Mod=0, the baud rate clock is not generated; when Baud\_Mod>1, baud rate = BUSCLK/(16xBaud\_Mod)

UARTO CON1 (DDH) UARTO mode control register 1

Bit number	7	6	5	4
Symbol	_	UART0_ENABLE	RECEIVE_ENABLE	MULTI_MODE
R/W	_	R/W	R/W	R/W
Reset value	_	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	m 0	0 000
ahvd. ce	6.35	ahyd. c	ra.30	ahvd. ro

	F 7 13	
Bit number	Bit symbol	Description Description
75-6	UART0_ENABLE	Module enable 1: Module enable, 0: Module close
5	RECEIVE_ENABLE	Receiver enable 1: Receiver is on, 0: Receiver is off
4	MULTI_MODE	Multi- processor communication mode 1: Mode enable, 0: Mode disable
3	STOP_MODE	Stop bit width selection 1: 2 bits, 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode, 0: 8-bit mode
1	PARITY_EN	Parity check enable 1: Parity check is enabled, 0: Parity check is disabled
00/1	PARITY_SEL	Parity check selection 1: Odd check, 0: Even check

UART0 CON2 (DEH) UART0 mode control register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	UART0_l	BD_ADD	TX_EMPTY_IE	RX_FULL_IE	UART(	D_BDH
R/W	_	_	R/W	R/W	R/V	V	R/	W
Reset value	_	_	0	0	1	1	0	0

Bit number	Bit symbol	Description
- A	HADTO DD ADD	Baud rate modulus divisor register, high 2 bits
5~4	UART0_BD_ADD	(determined by UART_BD_EXT whether to take effect)
		Transmit interrupt enable
3	TX_EMPTY_IE	1: Interrupt enable
		0: Interrupt disable (used in polling mode)
2	RX_FULL_IE Receive interrupt enable	

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(0)	70.33	
pene Ujo	,50	1: Interrupt enable
50501-01		0: Interrupt disable (used in polling mode)
1~0	UART0_BDH	The upper 2 bits ofthe baud rate modulus divisor register

UARTO STATE (DFH) UARTO status flag register

Bit number	7	6	5	4
Symbol	_	UART0_R8	UART0_T8	TIO
R/W	_	R	R/W	R/W
Reset value	_	0	0	0
Bit number	3	2	1	0
Symbol	RI0	UART0_RO	UART0_F	UART0_P
R/W	R/W R/W		N/W	R/W
Reset value	0 (2.5)	envd.	0 250	60 vd. 0

PC2 01 11	) •	her of the				
Bit number	Bit symbol	Description in S				
013 6 B	UART0_R8	The 9th data of the receiver, read only				
5	UART0_T8	The 9th data of the transmitter, read only when parity check is enabled				
4	TIO	Send interrupt mark: 1: The sending buffer is empty				
4	TI0	0: Send buffer is full, software write 0 to clear, write 1 is invalid				
		Receive interrupt mark:				
3	DIO	1: The receive buffer is full				
3	RI0	0: The receive buffer is empty, software writes 0 to clear, writes 1 is invalid				
2 BYD	UART0_RO	Receive overflow flag:  1: Receive overflow (new data is lost)  0: No overflow, software write 0 to clear, write 1 is invalid				
		Frame error flag:				
1	UART0 F	1: Frame error detected				
1	OAKTO_I	0: No frame error is detected, software writes 0 to clear, write 1 is invalid				
		Parity error flag:				
0	UARTO P	1: Receiver parity error				
	M .	0: The parity check is correct, the software writes 0 to clear, and writes 1 is invalid				

ACC (E0H) Accumulator

Bit number	7	6	5en 4 0 3	2	Pry 0/0/0:2
Symbol		0	ACC ACC	ping	10.20
R/W			R/W		77.2

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Reset value

Bit number	Bit symbol	Description
7~0	ACC	Accumulator: The destination register is suitable for all arithmetic and logic operations.

IRCON2 (E1H) Interrupt flag register 2

\ /		$\sigma$						
Bit number	7	6	5	4	3	2	1	0
Symbol	IE15	IE14	IE13	IE12	IE11	IE10	IE9	IE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number Bit symbol  External Interrupt interrupt flag bit  1: With External Interrupt interrupt flag  0: Clear External Interrupt flag bit  1: With External Interrupt flag bit  1: There is SPI interrupt flag  0: Clear SPI interrupt flag  Timer3/PWM1 interrupt flag bit  1: With Timer3/PWM1 interrupt flag  0: Clear Timer3/PWM1 interrupt flag  UART1 interrupt flag bit  1: UART1 interrupt flag bit  1: UART1 interrupt flag is available  0: Clear UART1 interrupt flag  UART0 interrupt flag bit  1: UART0 interrupt flag bit  1: UART0 interrupt flag is available  0: Clear UART0 interrupt flag  UART1 interrupt flag bit  1: UART1 interrupt flag is eleared  UART2 interrupt flag is cleared  UART2 interrupt flag is available  0: Clear UART1 interrupt flag is available  0: LVDT interrupt flag is available  0: Clear LVDT interrupt flag is available  0: Clear LVDT interrupt flag is available	-07		201/1
1: With External Interrupt4 interrupt flag 0: Clear External Interrupt3 interrupt flag External Interrupt3 interrupt flag bit 1: With External Interrupt3 interrupt flag 0: Clear External Interrupt3 interrupt flag 0: Clear External Interrupt3 interrupt flag  SPI interrupt flag bit 1: There is SPI interrupt flag 0: Clear SPI interrupt flag  Timer3/PWM1 interrupt flag bit 1: With Timer3/PWM1 interrupt flag 0: Clear Timer3/PWM1 interrupt flag UART1 interrupt flag bit 1: UART1 interrupt flag is available 0: Clear UART1 interrupt flag  UART0 interrupt flag bit 1: UART0 interrupt flag  LVDT interrupt flag bit 1: LVDT interrupt flag is present 0: LVDT interrupt flag is cleared UART2 interrupt flag is cleared  UART2 interrupt flag is available 0: LVART2 interrupt flag is available	Bit number	Bit symbol	Description
0: Clear External Interrupt4 interrupt flag External Interrupt3 interrupt flag bit 1: With External Interrupt3 interrupt flag 0: Clear External Interrupt3 interrupt flag  SPI interrupt flag bit 1: There is SPI interrupt flag 0: Clear SPI interrupt flag  Timer3/PWM1 interrupt flag bit 1: With Timer3/PWM1 interrupt flag 0: Clear Timer3/PWM1 interrupt flag 0: Clear Timer3/PWM1 interrupt flag 0: Clear Timer3/PWM1 interrupt flag UART1 interrupt flag bit 1: UART1 interrupt flag is available 0: Clear UART1 interrupt flag  UART0 interrupt flag bit 1: UART0 interrupt flag is available 0: Clear UART0 interrupt flag  LVDT interrupt flag bit 1: LVDT interrupt flag is present 0: LVDT interrupt flag is cleared UART2 interrupt flag is cleared  UART2 interrupt flag bit 1: UART2 interrupt flag is available	Per (0) 21 10.	70.5	External Interrupt4 interrupt flag bit
External Interrupt flag bit  1: With External Interrupt3 interrupt flag  0: Clear External Interrupt3 interrupt flag  SPI interrupt flag bit  1: There is SPI interrupt flag  0: Clear SPI interrupt flag  Timer3/PWM1 interrupt flag bit  1: With Timer3/PWM1 interrupt flag  0: Clear Timer3/PWM1 interrupt flag  UART1 interrupt flag bit  1: UART1 interrupt flag is available  0: Clear UART1 interrupt flag  UART0 interrupt flag bit  1: UART0 interrupt flag bit  1: UART0 interrupt flag bit  1: UART0 interrupt flag is available  0: Clear UART0 interrupt flag bit  1: UART0 interrupt flag is cleared  UART2 interrupt flag bit  1: UART2 interrupt flag bit  1: UART2 interrupt flag is available	IE15		1: With External Interrupt4 interrupt flag
6 IE14 1: With External Interrupt 3 interrupt flag 0: Clear External Interrupt 3 interrupt flag SPI interrupt flag bit 1: There is SPI interrupt flag 0: Clear SPI interrupt flag Timer3/PWM1 interrupt flag bit 1: With Timer3/PWM1 interrupt flag 0: Clear Timer3/PWM1 interrupt flag UART1 interrupt flag bit 1: UART1 interrupt flag is available 0: Clear UART1 interrupt flag UART0 interrupt flag bit 1: UART0 interrupt flag is available 0: Clear UART0 interrupt flag is available 0: Clear UART0 interrupt flag bit 1: LVDT interrupt flag bit 1: LVDT interrupt flag bit 1: LVDT interrupt flag is present 0: LVDT interrupt flag is cleared UART2 interrupt flag bit 1: UART2 interrupt flag is available	152.		0: Clear External Interrupt4 interrupt flag
0: Clear External Interrupt 3 interrupt flag  SPI interrupt flag bit  1: There is SPI interrupt flag  0: Clear SPI interrupt flag  Timer3/PWM1 interrupt flag bit  1: With Timer3/PWM1 interrupt flag  0: Clear Timer3/PWM1 interrupt flag  UART1 interrupt flag bit  1: UART1 interrupt flag is available  0: Clear UART1 interrupt flag  UART0 interrupt flag bit  2 IE10  1: UART0 interrupt flag is available  0: Clear UART0 interrupt flag  LVDT interrupt flag bit  1 IE9  1: LVDT interrupt flag is present  0: LVDT interrupt flag is cleared  UART2 interrupt flag bit  1: UART2 interrupt flag bit			External Interrupt3 interrupt flag bit
SPI interrupt flag bit  1: There is SPI interrupt flag  0: Clear SPI interrupt flag  Timer3/PWM1 interrupt flag bit  1: With Timer3/PWM1 interrupt flag  0: Clear Timer3/PWM1 interrupt flag  UART1 interrupt flag bit  1: UART1 interrupt flag is available  0: Clear UART1 interrupt flag  UART0 interrupt flag bit  2 IE10 1: UART0 interrupt flag is available  0: Clear UART0 interrupt flag is available  1: UART0 interrupt flag bit  1: UART0 interrupt flag bit  1: UART0 interrupt flag bit  1: UVDT interrupt flag bit  1: UVDT interrupt flag bit  1: UVDT interrupt flag is present  0: LVDT interrupt flag is cleared  UART2 interrupt flag bit  1: UART2 interrupt flag is available	6	IE14	1: With External Interrupt3 interrupt flag
1: There is SPI interrupt flag 0: Clear SPI interrupt flag Timer3/PWM1 interrupt flag bit 1: With Timer3/PWM1 interrupt flag 0: Clear Timer3/PWM1 interrupt flag UART1 interrupt flag bit 1: UART1 interrupt flag is available 0: Clear UART1 interrupt flag UART0 interrupt flag bit 1: UART0 interrupt flag is available 0: Clear UART0 interrupt flag UDART0 interrupt flag is available 0: Clear UART0 interrupt flag UDART0 interrupt flag bit 1: UVDT interrupt flag bit 1: LVDT interrupt flag is present 0: LVDT interrupt flag is cleared UART2 interrupt flag bit 1: UART2 interrupt flag is available			0: Clear External Interrupt3 interrupt flag
0: Clear SPI interrupt flag  Timer3/PWM1 interrupt flag bit  1: With Timer3/PWM1 interrupt flag  0: Clear Timer3/PWM1 interrupt flag  UART1 interrupt flag bit  1: UART1 interrupt flag is available  0: Clear UART1 interrupt flag  UART0 interrupt flag bit  1: UART0 interrupt flag is available  0: Clear UART0 interrupt flag  LVDT interrupt flag bit  1 IE9  1: LVDT interrupt flag is present  0: LVDT interrupt flag is cleared  UART2 interrupt flag bit  1: UART2 interrupt flag is available			SPI interrupt flag bit
Timer3/PWM1 interrupt flag bit  1: With Timer3/PWM1 interrupt flag  0: Clear Timer3/PWM1 interrupt flag  UART1 interrupt flag bit  1: UART1 interrupt flag is available  0: Clear UART1 interrupt flag  UART0 interrupt flag bit  2 IE10 1: UART0 interrupt flag is available  0: Clear UART0 interrupt flag bit  1: UART0 interrupt flag is present  1: LVDT interrupt flag bit  1: LVDT interrupt flag is present  0: LVDT interrupt flag is cleared  UART2 interrupt flag is available	5	IE13	1: There is SPI interrupt flag
1: With Timer3/PWM1 interrupt flag 0: Clear Timer3/PWM1 interrupt flag UART1 interrupt flag bit 1: UART1 interrupt flag is available 0: Clear UART1 interrupt flag UART0 interrupt flag bit 2 IE10 1: UART0 interrupt flag is available 0: Clear UART0 interrupt flag LVDT interrupt flag bit 1 IE9 1: LVDT interrupt flag is present 0: LVDT interrupt flag is cleared UART2 interrupt flag bit 1: UART2 interrupt flag bit			0: Clear SPI interrupt flag
0: Clear Timer3/PWM1 interrupt flag  UART1 interrupt flag bit  1: UART1 interrupt flag is available  0: Clear UART1 interrupt flag  UART0 interrupt flag bit  1: UART0 interrupt flag is available  0: Clear UART0 interrupt flag is available  0: Clear UART0 interrupt flag  LVDT interrupt flag bit  1 IE9  1: LVDT interrupt flag is present  0: LVDT interrupt flag is cleared  UART2 interrupt flag bit  1: UART2 interrupt flag is available			Timer3/PWM1 interrupt flag bit
UART1 interrupt flag bit  1: UART1 interrupt flag is available  0: Clear UART1 interrupt flag  UART0 interrupt flag bit  1: UART0 interrupt flag is available  0: Clear UART0 interrupt flag is available  0: Clear UART0 interrupt flag  LVDT interrupt flag bit  1: LVDT interrupt flag is present  0: LVDT interrupt flag is cleared  UART2 interrupt flag bit  1: UART2 interrupt flag is available	4	IE12	1: With Timer3/PWM1 interrupt flag
3 IE11 1: UART1 interrupt flag is available 0: Clear UART1 interrupt flag  UART0 interrupt flag bit 1: UART0 interrupt flag is available 0: Clear UART0 interrupt flag is available 0: Clear UART0 interrupt flag  LVDT interrupt flag bit 1: LVDT interrupt flag is present 0: LVDT interrupt flag is cleared  UART2 interrupt flag bit 1: UART2 interrupt flag is available			0: Clear Timer3/PWM1 interrupt flag
0: Clear UART1 interrupt flag  UART0 interrupt flag bit  1: UART0 interrupt flag is available  0: Clear UART0 interrupt flag  LVDT interrupt flag bit  1: LVDT interrupt flag is present  0: LVDT interrupt flag is cleared  UART2 interrupt flag bit  1: UART2 interrupt flag is available			UART1 interrupt flag bit
UART0 interrupt flag bit  1: UART0 interrupt flag is available 0: Clear UART0 interrupt flag  LVDT interrupt flag bit 1: LVDT interrupt flag is present 0: LVDT interrupt flag is cleared  UART2 interrupt flag is available  1: UART2 interrupt flag is available	3	IE11	1: UART1 interrupt flag is available
2 IE10 1: UART0 interrupt flag is available 0: Clear UART0 interrupt flag  LVDT interrupt flag bit 1 IE9 1: LVDT interrupt flag is present 0: LVDT interrupt flag is cleared UART2 interrupt flag bit 1: UART2 interrupt flag is available	BID		0: Clear UART1 interrupt flag
0: Clear UART0 interrupt flag  LVDT interrupt flag bit  1: LVDT interrupt flag is present  0: LVDT interrupt flag is cleared  UART2 interrupt flag bit  1: UART2 interrupt flag is available			UART0 interrupt flag bit
LVDT interrupt flag bit  1 IE9 1: LVDT interrupt flag is present 0: LVDT interrupt flag is cleared UART2 interrupt flag bit 1: UART2 interrupt flag is available	2	IE10	1: UART0 interrupt flag is available
1 IE9 1: LVDT interrupt flag is present 0: LVDT interrupt flag is cleared UART2 interrupt flag bit 1: UART2 interrupt flag is available			0: Clear UART0 interrupt flag
0: LVDT interrupt flag is cleared  UART2 interrupt flag bit  1: UART2 interrupt flag is available			LVDT interrupt flag bit
UART2 interrupt flag bit  1: UART2 interrupt flag is available	1	IE9	1: LVDT interrupt flag is present
0 IE8 1: UART2 interrupt flag is available			0: LVDT interrupt flag is cleared
			UART2 interrupt flag bit
0: Clear LVDT interrupt flag	0	IE8	1: UART2 interrupt flag is available
	1 cor	0,5	0: Clear LVDT interrupt flag

UARTO BUF (E2H) UARTO port data register

B	it number	7	6	5en(0	14/6:30	3	2	benico	7000
	Symbol		o <sup>i</sup>	ing of U	1702		ni	38. 20	1-02
100	R/W		,	10/12	R/W		,	11/12	

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Reset value

Bit number	Bit symbol	Description
7~0		Read returns the contents ofthe read-only receive data buffer, write into the write-only transmit data buffer

IICADD (E3H) IIC address register

Bit number	7	6	5	4	3	2	1	0
Symbol		IICADD[7:1]						
R/W		R/W						
Reset value				0				_

IICBUF (E4H) IIC send and receive data register

	Bit number	2.37	6	5	3	2	1	7/d.0 +1
	Symbol	20.0		hen (a)	IICBUF		hen (a)	1/1/1
کے	R/W		· ·	ing. M	R/W	n'i	ve V	17/1/
(	Reset value		<i>y</i>	1012	0	\ \frac{1}{2}	06/3-0	,

Bit number	Bit symbol	Description
7~0	IICBUF	IIC transmit and receive data buffer

IICCON (E5H) IIC configuration register

		0		
Bit number	7	6	5	4
Symbol	_	_	IIC_RST	RD_SCL_EN
R/W	_	_	R/W	R/W
Reset value	<u> </u>	- ~	0	1
Bit number	3	2,512.00	1	0.19.00
Symbol	WR_SCL_EN	SCLEN	SR	IIC EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0000	0	000

Bit number	Bit symbol	Description			
7~6		Reserved			
		IIC module reset signal			
5	IIC_RST	1: IIC module reset operation,			
		0: IIC module works normally			
		The host reads the low clock line control bit			
4	RD_SCL_EN	1: Enable the host to read and pull down the clock line function,			
		0: Disable the host read and pull down clock line function			
1	WR_SCL_EN	The host writes the low clock line control bit,			
3810		1: Enable the function of writing and pulling down the clock line,			

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	$(0)_{i,j}$	20.3	
2	pena 01 10	, ) "	0: Disable the function of writing and pulling down the clock line
C	2	SCLEN	IIC clock enable bit: 1=clock works normally, 0=lows the clock line
	1	SR	IIC conversion rate control bit  1: The conversion rate control is turned off to adapt to the standard speed mode (100K);
			0: Conversion rate control is enabled to adapt to fast speed mode (400K)
	0	IIC_EN	IIC work enable bit: 1: IIC works normally, 0: IIC does not work

IEN1 (E6H) Interrupt enable register 1

	# \ 1 <b>0 1</b> \ . /	0			1 1 0 1			
Bit number	20.7	6	5-0	9/3/4/6	3	2	1-0	0/1/2
Symbol	EX7	EX6	10g. De	EX4	EX3	EX2	108 C	11/1/20
R/W	R/W	R/W	2002	R/W	R/W	R/W	0002	_
Reset value	0	0	_	0	0	0		_

Bit number	Bit symbol	Description
		WDT/Timer2/PWM0 interrupt enable
7	EX7	1: WDT/Timer2/PWM0 interrupt enable;
		0: WDT/Timer2/PWM0 interrupt disable
		LED/LCD interrupt enable
6	EX6	1: LED/LCD interrupt enable;
		0: LED/LCD interrupt disable
		ADC interrupt enable
4	EX4	1: ADC interrupt enable;
VVa		0: ADC interrupt disable
Dr		IIC interrupt enable
3	EX3	1: IIC interrupt enable;
		0: IIC interrupt disable
		External Interrupt2 interrupt enable
2	EX2	1: External Interrupt2 interrupt enable;
		0: External Interrupt2 interrupt disable
5, 1~0	-	Reserved

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	EX15	EX14	EX13	EX12	EX11	EX10	EX9	EX8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	20.0 Ser	0	0	0	120.9 Err	0
BAD		5	IIII			5	IIII	

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	' \ \ \ ' '					
Bit number	Bit symbol	Description Description				
0501-0		External Interrupt4 enable				
7	EX15	1: External Interrupt4 interrupt enable;				
		0: External Interrupt4 interrupt disable				
		External Interrupt3 enable				
6	EX14	1: External Interrupt3 enable;				
		0: External Interrupt3 disable				
		SPI interrupt enable				
5	EX13	1: SPI interrupt enable;				
		0: SPI interrupt disable				
		Timer3/PWM1 interrupt enable				
4	EX12	1: Timer3/PWM1 interrupt enable;				
		0: Timer3/PWM1 interrupt disable				
		UART1 interrupt enable				
3	EX11	1: UART1 interrupt enable;				
		0: UART1 interrupt disable				
		UART0 interrupt enable				
2	EX10	1: UART0 interrupt enable;				
		0: UART0 disable				
		LVDT interrupt enable				
1	EX9	1: LVDT interrupt enable;				
		0: LVDT interrupt disable				
	O EXO	UART2 interrupt enable				
0 7 00	EX8	1: UART2 interrupt enable;				
abyu.	6.37	0: UART2 interrupt disable				

IICSTAT (E8H) IIC status register

110011	, iie status register	110, 7,1		110, 111,
Bit number	7	ing 6 1	5	ing. 4 J
Symbol	IIC_START	IIC_STOP	IIC_RW	IIC_AD
R/W	R	R	R	R
Reset value	0	1	0	0
Bit number	3	2	1	0
Symbol	IIC_BF IIC_ACK		IIC_WCOL	IIC_RECOV
R/W	R R		R/W	R/W
Reset value	0	1	0	0

Bit number	Bit symbol	Description
abyd. Co.	2.35	Start signal flag
Den 07 16	IIC_START	1: Indicates that the start bit is detected;
THAN B		0. Indicates that the start bit is not detected.
1000	IIC_STOP	Stop signal flag

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BYD	Semiconductor
(3,1)	Geniconductor

Bit number

(a) (b) (c)	20:33	
perio Wijo	J	1: Means in the stop state;
25-01-01		0: Means that the stop bit is not detected.
		Read and write flag
		Record the read/write information obtained from the address
5	IIC_RW	byte after the last address match,
		1: Indicates read operation;
		0: Means write operation.
		Address data flag
4	IIC AD	1: Indicates that the most recently received or sent byte is data;
	_	0: Indicates that the most recently received or sent byte is an address.
		IICBUF full flag bit: when receiving in IIC bus mode
		1: Indicates that the reception is successful and the buffer is full;
		0: Indicates that the reception is not completed and the buffer is still empty
2	HC DE	When sending in IIC bus mode:
3	IIC_BF	1: Indicates that data transmission is in progress (not
		including the response bit and stop bit), and the buffer is still full;
		0: Indicates that the data transmission has been completed
		(not including the response bit and stop bit), and the buffer is empty.
		Reply flag
2	IIC_ACK	1: Indicates an invalid response signal; 0: Indicates an effective response signal.
		Write conflict flag
1	IIC_WCOL	1: Indicates that when the IIC is sending the current data, new data is trying to be written into the sending buffer; the new data cannot be written into the buffer;
		0: No write conflict occurred.
		Receive overflow flag
		1: Indicates that new data is received when the previous data
0	IIC_RECOV	received by IIC has not been taken away, and the new data
	Ω	cannot be received by the buffer;
Tapyd. Co	2.35	0: Indicates that no receive overflow has occurred.
IICBUFFER (E	9H) IIC transmit and	I receive data buffer register

Symbol

)4

3

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$(0)$ $\beta$ , $(3)$	$\mathcal{D}^{\circ,\circ}$	ζ
R/W	R/W	
Reset value	0	
		٠.

TRISA (EAH) PA direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	-	1	-	-	ı	-	
R/W	_	_	_	_	R/W	R/W	R/W	R/W
Reset value	_	_	_	_	1	1	1	1

Bit number	Bit symbol	Description	
		Bit[3]~ Bit[1]: direction of PA3~PA0 port pins	
3~0	<u></u>	0: PAx port is output;	com
ahvd. ce	0.35	1: PAx port is input	aprid. co

TRISB (EBH) PB direction register

Z	Bit number	7	6	ng.5 - (	1-14	3	2	1081	0
(	Symbol	_	_	JUJ3.	BALL	_	_	00/13	O'BYD
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
		Bit[7]~ Bit[1]: direction of PB7~PB0 port pins
7~0		0: PBx port is output;
		1: PBx port is input

TRISC (ECH) PC direction register

		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	$\mathcal{C}$		~ 7	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \			~7.1.7
	Bit number	27	6	5	1-1 <del>4</del> , cos	23	2	1	1-1/90cor
	Symbol	26.2	_	1-07	000 7 10-	)	-	1-00	00, 70,
ing	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Direc	Reset value	1	1		1	1	1		1

Bit number	Bit symbol	Description
		Bit[7]~ Bit[1]:direction of PC7~PC0 port pins
7~0		0: PCx port is output;
		1: PCx port is input

UART2 CON2 (EDH) UART2 mode control register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	<b>~</b> -	_	UART2_	BD_ADD	TX_EMPTY_IE	RX_FULL_IE	UAR	Г2_ВDН
R/W	- J	<b>K</b> _	R/W	R/W	R/W	R/W	F	S/M COLL
Reset value	13.	7)	0	0 0	1997 (18.33)	1	00	00.5
1-011	100			1-011	> 1 110°	4	-0110	1 11100

Bit number	Bit symbol 🛇	Me OF MILE	Description Dillipolitical Description
5~4	UART2_BD_ADD	The upper 2 bits ofthe	e baud rate modulus divisor register.

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	7().5	
ben 6 01 10		(it is determined by UART_BD_EXT whether to take effect)
77/2		Send interrupt enable
3	TX_EMPTY_IE	1: Interrupt enable;
		0: Interrupt disable (used in polling mode)
		Receive interrupt enable
2	RX_FULL_IE	1: Interrupt enable;
		0: Interrupt disable (used in polling mode)
1~0	UART2_BDH	Baud rate modulus divisor register, high 2 bits

TRISE (EEH) PE direction register

	Bit number		6	5	4	3	2	1	0.00
	Symbol	· 0.55	_	_	Md. Co.	0.35	_	- (	24g. 60.
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
5	Reset value	1	1	ng1 .		1	1	1281	1

Bit number	Bit symbol	Description
7~0		Bit[7]~ Bit[1]: direction of PE7~PE0 port pins 0: PEx port is output; 1: PEx port is input

TRISF (EFH) PF direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	_	_
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	71. co,	24	1	1	12.1COV
000	28:33		- an(	0)0/1/6	26:33		((	7.7

Bit number	Bit symbol	Description
7~0		Bit[7]~ Bit[1]; direction of PF7~PF0 port pins  0: PFx port is output;  1: PFx port is input

B (F0H) B register

Bit number	7	6	5	4	3	2	1	0	
Symbol	В								
R/W	R/W								
Reset value	0								

Bit number Bit	t symbol	Description
pen 9-0 76:28:22	В	B register: the source and destination registers of multiplication and division operations.

IRCONI (F1H) Interrupt flag register 1

410001(4411)	micon apr	1145 105151,					0,1,1,	
Bit number	7	6	3/12	4	3	2	Mrs	0

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		7/10-							
<	Symbol	IE7	IE6	_	IE4	IE3	IE2	_	_
ح	R/W	R/W	R/W	_	R/W	R/W	R/W	_	_
(	Reset value	0	0	_	0	0	0	_	_

Bit number	Bit symbol	Description
		WDT/Timer2/PWM0 interrupt flag
7	IE7	1: WDT/Timer2/PWM0 interrupt flag;
		0: Clear WDT/Timer2/PWM0 interrupt flag
		LED/LCD interrupt flag
6	IE6	1: With LED interrupt flag;
		0: Clear LED interrupt flag
		ADC interrupt flag
4	IE4	1: ADC interrupt flag is present;
		0: ADC interrupt flag is cleared
		IIC interrupt flag
3	IE3	1: IIC interrupt flag is present;
		0: IIC interrupt flag is cleared
		External Interrupt2 interrupt flag
2	IE2	1: External Interrupt2 interrupt flag;
		0: Clear External Interrupt2 interrupt flag
5, 1~0	_	Reserved

TRISG (F2H) PG direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	0 -	_	_	- 601	<u></u>	_	_	om
R/W	C.P.D.	_	_ (	774g. Co	R/W	R/W	R/W	R/W
Reset value	20	_	hen	000 10	1	1	1en	1/1/2
Marin - 3		·	128 - 1	17/11			ing.	1111

Bit number	Bit symbol	Description Description
		Bit[3]~ Bit[1]:direction of PG3~PG0 port pins
3~0		0: PGx port is output;
		1: PGx port is input

IPL2 (F4H) Interrupt priority register2

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL2.7	IPL2.6	IPL2.5	IPL2.4	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0
	<b>A</b>	-	•		<u> </u>		•	. (1)

	-1-110.	0.51	1-10.	-1-XIU. 10.
	Bit number	Bit symbol	Description	1 6000
ر ر	050707	IPL2.7	External Interrupt4 priority selection bit.  1: External Interrupt4 interrupt is high prior.	ity] 5-07-07
	N			N

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pene 11 10	,5	0: External Interrupt4 interrupt is low priority			
2501-0		External Interrupt3 priority selection bit.			
6	IPL2.6	1: External Interrupt3 interrupt is high priority;			
		0: External Interrupt3 interrupt is low priority			
		SPI priority selection bit.			
5	IPL2.5	1: SPI interrupt is high priority;			
		0: SPI interrupt is low priority			
		Timer3/PWM1 priority selection bit.			
4	IPL2.4	1: Timer3/PWM1 interrupt is high priority;			
		0: Timer3/PWM1 interrupt is low priority			
		UART1 priority selection bit.			
3	IPL2.3	1: UART1 interrupt is high priority;			
		0: UART1 interrupt is low priority			
		UART0 priority selection bit.			
2	IPL2.2	1: UART0 interrupt is high priority;			
		0: UART0 interrupt is low priority			
		LVDT priority selection bit.			
1	IPL2.1	1: LVDT interrupt is high priority;			
		0: LVDT interrupt is low priority			
		UART2 priority selection bit.			
0	IPL2.0	1: UART2 interrupt is high priority;			
		0: UART2 interrupt is low priority			

IPL1 (F6H) Interrupt priority register1

	Bit number 7	6	5	4 cos	3	2	1	70000
	Symbol IPL1.	7 IPL1.6	- (	IPL1.4	IPL1.3	IPL1.2		10 Joy
۲	R/W R/W	R/W	perio	R/W	R/W	R/W	perio	W. 10"
ح م	Reset value 0	0	JILL SOL	0	0	0 5	TILE COL	1/202
	Mrs A	·	1772				ومالال	

Bit number	Bit symbol	Description				
		WDT/Timer 2/PWM0 interrupt priority bit				
7	IPL1.7	1: WDT/Timer 2/PWM0 interrupt is high priority;				
		0: WDT/Timer 2/PWM0 interrupt is low priority				
		LED/LCD interrupt priority bit				
6	IPL1.6	1: LED/LCD interrupt is high priority;				
		0: LED/LCD interrupt is low priority				
		ADC interrupt priority bit				
4	IPL1.4	1: ADC interrupt is high priority;				
		0: ADC interrupt is low priority				
(Va		IIC interrupt priority bit				
3010	IPL1.3	1: IIC interrupt is high priority;				

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$(0)_{i,j}$	70.3	
pene UJD	,50	0: IIC interrupt is low priority
0201-01		External Interrupt2 priority selection bit
2	IPL1.2	1: External Interrupt2 is high priority;
		0: External Interrupt2 is low priority
5, 1~0		Reserved

TRISH (F7H) PH direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	_	_
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

- om	som .	c ()
Bit number Bit symbol	Description	ahyd.co
pen(0) 1 16:00.5	Bit[7] Bit[1]: direction of PH7~PH0 p	ort pins
	0. PHx port is output;	ing. 1 11.11
1052	1. PHx port is input	11/12-01

DATAA (F8H) PA port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	PA3	PA2	PA1	PA0
R/W	_	_	_	_	R/W	R/W	R/W	R/W
Reset value	_	_	_	_	1	1	1	1

Bit number	Bit symbol	Description
		PA data register, you can configure the output level of the
3~0	58:35 -	PA group IO port as GPIO port, the read value is the current level state of the IO port (input) or the configured output value (output)

PWM INT CTRL (FAH) PWM interrupt enable control register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	ı	_	_	-	
R/W	_	_	_	-	_	_	R/W	R/W
Reset value	_	_	_	-	_	_	0	0

Bit number	Bit symbol	Description
		PWM1 counter overflow interrupt
1		1: Interrupt enable;
		0: Interrupt disable
		PWM0 counter overflow interrupt
0		1: Interrupt enable;
BID		0: Interrupt disable

**Note:** 

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# 4.2. Secondary Bus Registers Details

$CFG0_{\_}$	_REG (	(00H)	) Config	guration w	ord re	gister	: 0	

Bit number	7	6	5	4	3	2	1	0				
Symbol					-							
R/W		R										
Reset value		FF										

#### CFG1\_REG (01H) Configuration word register 1

Bit number	7	6	5	4	3	2	1	0				
Symbol					_							
R/W	$\mathcal{D}$	N.R.										
Reset value	. o.35			abyd. Co.	64.3			programme con				

### CFG2\_REG (02H) Configuration word register 2

Bit number	7	6	1085	3	2	181
Symbol			My BAD			10 2-11 BXD
R/W			R			
Reset value			1F	7		

#### CFG3\_REG (03H) Configuration word register 3

Bit number	7	6	5	4	3	2	1	0		
Symbol		_								
R/W		R								
Reset value		FF								

#### CFG4 REG (04H) Configuration word register 4

		- ' (/ )			-473
6	5	4.00	2	1	7-190 <sub>CO2</sub>
	1 en	0007 16:26:33		1 00	001 10.
	12. De	R	•	15. DC	JULIO.
Υ,	2002	2D	Υ,	100	9/1.0
	6	6 5	6 5 4 0 3 R 2D	6 5 4 2D	6 5 4 0 3 2 1  R  2D

#### CFG5 REG (05H) Configuration word register 5

Bit number	7	6	5	4	3	2	1	0			
Symbol					_						
R/W		R									
Reset value		С9									

#### CFG6 REG (06H) Configuration word register 6

Bit number	7	6	5	4	3	2	1	0
Symbol					G			~
R/W	25				J. Coll.			
Reset value	36:33			apya 16:	3 <b>F</b>			997 C.5

#### CFG7 REG (07H) Configuration word register 7

Bit number	7	6	71115505	11/4/10	3	2	11112 V 2 1 1 2 0 D	
Symbol			17772	V ·	_		The D	

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(128.33)	(.58							
R/W R	170.3							
Reset value 1F	05-01-0							
CFG8_REG (08H) Configuration word register 8								
Bit number         7         6         5         4         3         2	1 0							
Symbol _								
R/W R								
Reset value FF								
CFG9_REG (09H) Configuration word register 9								
Bit number         7         6         5         4         3         2	1 0							
Symbol _								
R/W COTR	com							
Reset value FF	abyd. Co							
CFG10 REG (0AH) Configuration word register 10	Den (1/0:21							
Bit number 7 6 15 4 3 2	1							
Symbol _	Month Bit							
R/W R	R							
Reset value FF								
CFG11_REG (0BH) Configuration word register 11								
Bit number         7         6         5         4         3         2	1 0							
Symbol _								
R/W R								
Reset value FF								
CFG12_REG (0CH) Configuration word register 12	m							
Bit number 6 5 4 2 2	1 2000							
Symbol (5.20.3	264(0)p, 1(1)							
R/W ing. R ing.	De Will In.							
Reset value 7F	10,2-01							
CFG13_REG (0DH) Configuration word register 13								
Bit number         7         6         5         4         3         2	1 0							
Symbol _								
R/W R								
Reset value 7								
RST STAT (0FH) Reset flag register								
Bit number         7         6         5         4         3         2	1 0							
Bit flumber / 0 3 4 3 2								
BOOT DEBUG SOFT PROG ADD	WDT							
BOOT DEBUG SOFT PROG ADD	PO_F WDT RST_F							
Symbol BOOT_ DEBUG_ SOFT_ PROG_ ADD ROF_F BO_F I	PO F							

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	7()0-	
Bit number	Bit symbol	bent of Description bent of 10.3
7	BOOT_F	0: no effect;  1: A reset occurs when the configuration program space jumps
6	DEBUG_F	0: No effect; 1: Trim configuration reset occurred.
5	SOFT_F	0: No effect; 1: Software reset occurred.
4	PROG_F	0: No effect; 1: Program reset occurred.
3	ADDROF_F	0: No effect; 1: PC pointer overflow reset occurred.
2	BO_F	0: No effect; 1: Power_down reset occurred.
1	PO_F	0: No effect; 1: Power_on reset occurred.
0	WDTRST_F	0: No effect; 1: Watchdog timer overflow reset occurred.

PU PA (17H) PA pull-up resistor control register

1 0 111 (1/11) 1								
Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	_	_
R/W	_	_	_	_	R/W	R/W	R/W	R/W
Reset value	-	_	_	- ~	0	0	0	0
<sup>2</sup> co,	05			$^{\gamma}$ $c_{O_{i}}$	70%			7 COIL

	. 3(1)			
	Bit number Bit sym	bol	Description	1 000
2	Der J Oth	PA pu	ill-up resistor control register	ing period William
ر ر	3~0	1: The	pull-up resistor is enabled;	DILLO 12-01-01
	701-	0: The	e pull-up resistor is not enable	d

PU PB (18H) PB pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0	
Symbol		_							
R/W		R/W							
Reset value				(	)				

Bit number	Bit symbol	Description	
2 cox	77	PB pull-up resistor control register	y cour
720	8:22	1: The pull-up resistor is enabled;	apya. C. 2
bene 0170	, , , , , , , , , , , , , , , , , , , ,	0: The pull-up resistor is not enabled	pener 110.2

PU PC (19H) PC pull-up resistor control register

T	(17 T TO ( 17 1-17)	- FF .			9-			01111	
	Bit number	7	6	75	4	3	2		0

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	2()·2
Symbol	<u>-</u>
R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
		PC pull-up resistor control register
7~0		1: The pull-up resistor is enabled;
		0: The pull-up resistor is not enabled

PU PE (1BH) PE pull-up resistor control register

()-	- p **** **p							
Bit number	7	6	5	4	3	2	1	0
Symbol	D .				com			
R/W	6.35			Md. R	ahyd. co			
Reset value	20.2		hen(	0,10:	ben and this			
5 1 11 11			128. 1	17/11		n'i	va. V	

			~ ~ \
Bit number	Bit symbol	Description	BY
		PE pull-up resistor control register	
7~0		1: The pull-up resistor is enabled;	
		0: The pull-up resistor is not enabled	

PU PF (1CH) PF pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0			
Symbol		<u> </u>									
R/W		R/W									
Reset value	0	000									

	-1-10		-1-10	-1-1/04
4	Bit number	Bit symbol	Description	1 6000
5	729		PF pull-up resistor control register	sing by Millian
<u> </u>	7~0	<del></del>	1: The pull-up resistor is enabled;	1111 100 2-01
			0: The pull-up resistor is not enabled	

PU PG (1DH) PG pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	_	_
R/W	_	_	_	_	R/W	R/W	R/W	R/W
Reset value	_	_	_	_	0	0	0	0

Bit number	Bit symbol	Description	•
14. co		PG pull-up resistor control register	ey com
320	8:33	1: The pull-up resistor is enabled;	20)phay 6.20
period Office		0: The pull-up resistor is not enabled	period William

PU\_PH (1EH) PH pull-up resistor control register

A1		_ \	- 1		<b>&gt;</b> /	1			$\sim$ $\sim$		-	<i>_</i>	- 4	 						1			-
	B	it n	um	ıbe	er	7	6	(		5	1	)	`	4	3	2	Ţ	J	١,٠	J	Ø	0	

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Symbol	<u>-</u>
R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
		PH pull-up resistor control register
7~0		1: The pull-up resistor is enabled;
		0: The pull-up resistor is not enabled

LCD\_IO\_SEL\_1 (1FH) LCD\_SEG0-7 port selection configuration register

0
SEGOV
R/W
0/1/

Bit number	Bit symbol	Description By
7~0		LCD_SEG0-7 port selection configuration register, the corresponding bit is 1 to select SEG port function  1: Select SEGMENT port mode;
		0: Select IO port mode

LCD\_IO\_SEL\_2 (20H) LCD SEG8-15 port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	θ	0	0	(-1/90 <sub>CO</sub> )	20	0	0	3.60

Bit number	Bit symbol	Description Description
7~0		LCD SEG8-15 port selection configuration register, the corresponding bit is 1 to select SEG port function
		Select SEGMENT port mode;     Select IO port mode

LCD\_IO\_SEL\_3 (21H) LCD\_SEG16-23 port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	SEG23	SEG22	SEG21	SEG20	SEG19	SEG18	SEG17	SEG16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	Reset value 0 0			0	0	0	0	
2 co <sup>3</sup>	05				4 COLLI			

Bit number Bit symbol	Description Description
202-12-12/12	LCD_SEG16-23 port selection configuration register, the corresponding bit is 1 to select SEG port function 1: Select SEGMENT port mode;

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#### 0: Select IO port mode

LCD IO SEL 4 (22H) LCD SEG24-27 port selection configuration register

Bit number	7	6	5	4	3	2	1	0B3
Symbol	_	_	_	_	SEG27/COM7	SEG26/COM6	SEG25/COM5	SEG24/COM4
R/W	_	_	_	_	R/W	R/W	R/W	R/W
Reset value	_	_	_	_	0	0	0	0

Bit number	Bit symbol	Description
		LCD_SEG24-27 port selection configuration register,
		reserved in non-sharing mode, shared mode COM4~COM7
3~0		is LCD_SEG24-27
abyd. Co	6.32	1: Select SEG24~SEG27 port/COM4~COM7;
264(0) 1/2, 1/2.	20.2	0: Select IO port mode.

COM IO SEL (23H) COML select configuration register

Bit number	7	6	2/12	M A IV	3	2	101 27	1180
Symbol	COML7	COML6	COML5	COML4	COML3	COML2	COML1	COML0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
		In LED matrix drive mode, 4*4 mode is not selected:
		COM port select configuration register, the corresponding bit is 1,
		COMLx is common
		1: Select the COM port function.
		0: Select the I/O port mode
- 0.10		In LED matrix drive mode, select 4*4 mode:
7~0	)	COML0~ COML3 is common, and COML4~ COML7 is segment
D r		1: Select COM port function or SEG port function;
		0: Select the I/O port mode
		When the high current IO port drive is enabled:
		1: Select the high-current I/O port
		0: Select the I/O port mode

SEG IO SEL (24H) LED SEG0-7 port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	00	0	0	10000 E	250	0	0	2/9.00

- 4		, <u> </u>		
ξ,	Bit number	Bit symbol	Description ing.	
	7~0		LED_SEG0-7 port selection configuration register, the	7

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corresponding bit is 1, select SEG function

1: Select SEGMENT port mode;

0: Select IO port mode

Note: This register is only valid when the LED matrix is not 4\*4 mode.

DRAIN EN (25H) PC4/5/PE4/5 port open drain output enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	-	_	_	_	
R/W	_	_	_	_	R/W	R/W	R/W	R/W
Reset value	_	_	_	_	0	0	0	0

	-01	$\Omega$	20th
	Bit number	Bit symbol	Description
	Per (0) 21 1P.	20.2	PE5 port open drain output enable register
Ę	3-013		1. Open drain output
(	0520	>	0: CMOS output
			PE4 port open drain output enable register
	2		1: Open drain output
			0: CMOS output
			PC5 port open drain output enable register
	1		1: Open drain output
			0: CMOS output
			PC4 port open drain output enable register
	0	<del></del>	1: Open drain output
	7.co		0: CMOS output

ADC IO SEL0 (2AH) ADC function selection register 0

	(		11 2 11 1 11 1 1 1	1010101			
Bit number	7	6	3em	(4)0.	3	2	
Symbol	_	7	111202-1	ADC_	IO_SEL0	[6:0]	VIII. 202-11-01
R/W	_		111123		R/W		
Reset value	_				0		

Bit number	Bit symbol	Description
		Enable the ADC control function that disables analog input pins  1: Select ADC function;
6~0	ADC_IO_SEL0[6:0]	0: Not select ADC function 0000001=ADC0; 0000010=ADC1; 0000100=ADC2;
ben@byd. 01.16	36.33	0001000=ADC3; 0010000=ADC4; 0100000=ADC5; 1000000=ADC6

SEL LVDT VTH (2CH) LVDT threshold selection register

Bit number 7 6 5 4 3 2 1 0
----------------------------

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Symbol	_	_	_	_	ı	SE	L_LVDT_`	VTH
R/W	_	_	_	_	_	R/W	R/W	R/W
Reset value						0	0	0

Bit number	Bit symbol	Description
2~0	SEL_LVDT_VTH	LVDT threshold selection, the corresponding threshold is shown in the table "Threshold and Delay Selection" 000=2.7V; 001=3.0V;
		010=3.8V; 011=4.2V; 100=3.3V; 101=3.6V; 110=4.0V; 111=4.4V

PD ANA (2DH) Module switch control register

Bit number	7	6	5	4	3~1	0
Symbol	_	PD_LVDT	_	PD_XTAL_32K		PD_ADC
R/W	_	R/W	_	R/W	_	R/W
Reset value	_	1	_	1	_	1

Bit number	Bit symbol	Description
6	PD LVDT	LVDT control register
0	ID_LVDI	1: Closed, 0: Open, closed by default
4	PD_XTAL_32K	PA port crystal oscillator circuit (32768Hz) control register, 1: Closed, 0: Open, closed by default
5, 3~1		Reserved
		Analog ADC shutdown control register:
0 PD_ADC		0: ADC module works normally;
		1: ADC module does not work

IDLE WAKE CFG (30H) System wakeup configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	PLI	L_WAKE_	TIM
R/W	_	_	_	_	_		R/W	
Reset value	_	_	_	_	_	1	1	1
, c0 <sup>1</sup>	<u> </u>			, c0 <sup>5</sup>	D.			com

	1 60 25		1 00 25	1 6	_
	Bit number Bit symb	ool	Description	Opia. Es	0
Q	bene at 10.3	• 🗸	When PCON=1, wake up PLL timin	ng time	
7	2~0 PLL_WAKE	- 1		mins 05-01-0	
	No.		001: 0.3ms;	, Marie Lander	

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010: 0.4ms; 011: 0.5ms; 100: 0.6ms; 101: 0.7ms; 110: 0.9ms; 111: 1ms

LED DRIVE (31H) LED port drive capability configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	-	ı	_			_	
R/W	_	-	-	_	R/W	R/W	R/W	R/W
Reset value	0 -	1	-	<u>-</u> - 01	0	0	0	0.00
opyd. Co	0.35			hyd. Co	0.35			byd. Co

Bit number Bit syml	bol hen	Description	ben (0) 1 (1)
3~0	4mA~78mA,	ve capability configuration r	1000-01

ADC CFG SEL (32H) ADC configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	_		ADCWNUM			ADC_I_SEL		
R/W	_	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	_	0	0	0	0	0	0	0

Bit number	Bit symbol	Description	V
692d.co	ADCWNUM	Selection of distance conversion intersampling: (3+ADCWNUM)*TADCK	rval time after
BMD per	ADC_I_SEL[1]	ADC select comparator bias current 1: 4uA; 0: 5uA	ning per of MIO.
0	ADC_I_SEL[0]	ADC select buffer bias current 1: 4uA; 0: 5uA	1770

PWM IO SEL (33H) PWM port selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	_	_
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

	Bit number	Bit symbol	Description	4 com
	alpyd.	8:23	PWM3 port selection enable	9) July (15)
. O	ben 70170	PWM_IO_SEL[7]	1: Select PWM3 function;	perio 1/10.3
) E	J/2 0.20	\$	0: Not select PWM3 function	ning 05-01-0
	6	PWM_IO_SEL[6]	PWM2 port selection enable	JN 12

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-0	28.33	
pener 11 10		1: Select PWM2 function;
25-01-0		0: Not select PWM2 function
77/2		PWM1C port selection enable
5	PWM_IO_SEL[5]	1: Select PWM1C function;
		0: Not select PWM1C function
		PWM1B port selection enable
4	PWM_IO_SEL[4]	1: Select PWM1B function;
		0: Not select PWM1B function
		PWM1A port selection enable
3	PWM_IO_SEL[3]	1: Select PWM1A function;
		0: Not select PWM1A function
		PWM0C port selection enable
2	PWM_IO_SEL[2]	1: Select PWM0C function;
		0: Not select PWM0C function
		PWM0B port selection enable
		1: Select PWM0B function;
1	PWM_IO_SEL[1]	0: Not select PWM0B function.
		When PWM0B and PWM1D are configured at the same
		time, PWM0B is valid and PWM1D is invalid
		PWM0A port selection enable
		1: Select PWM0A function;
0	PWM_IO_SEL[0]	0: Not select PWM0A function.
. ~	0	When PWM0A and PWM1E are configured at the same
<sup>7</sup> c <sub>O</sub> ,		time, PWM0A is valid, and PWM1E is invalid

PERIPH IO SEL1 (34H) External port function selection register 1

	I DIGITAL TO DE	Die (5 iii) Die Cinai p	ort ranction beleetid	n i ogistor i	
5	Bit number	7	berg 11/10	5	ben 4 1/10.
	Symbol	UART1_IO_SEL	UARTO_	IO_SEL	IIC_IO_SEL
	R/W	R/W	R/W	R/W	R/W
	Reset value	0	0	0	1
	Bit number	3	2	1	0
	Symbol	INT3_IO_SEL	INT2_IO_SEL	INT1_IO_SEL	INTO_8_IO_SEL
	R/W	R/W	R/W	R/W	R/W
	Reset value	0	0	0	0

Bit number	Bit symbol	Description	
		UART1 port selection enable	
7	UART1_IO_SEL	0: Select UART1 (RXD1B/TXD1B) function;	
		1: Select UART1 (RXD1A/TXD1A) function	
LIADTO IO SEI		UART0 port selection enable	
6~5 UART0	UART0_IO_SEL	00: select UART0 (RXD0C/TXD0C) function;	

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$(0)_{\lambda}$	70.3	
pence 01.01 10		01: Select UART0 (RXD0A/TXD0A) function;
205-01		1x: select UART0 (RXD0B/TXD0B) function
		IIC port selection enable
4	IIC_IO_SEL	0: Select IIC (SCL0B/SDA0B) function;
		1: Select IIC (SCL0A/SDA0A) function
	INT3 IO SEL	INT3 port selection enable
3	INT3_IO_SEL	1: Select INT3 function; 0: Not select INT3 function
	INTO IO SEI	INT2 port selection enable
2 INT2_IO_SEL		1: Select INT2 function; 0: Not select INT2 function
1 INT1_IO_SEL		INT1 port selection enable
		1: Select INT1 function; 0: Not select INT1 function
INTO 8 IO SEL		INTO_8 port selection enable
Pevino, 19.	JUNIO_6_IO_SEL	1: Select INT function; 0: Not select INT function

PERIPH IO SEL2 (35H) External port function selection register 2

Bit number	7	1000 B	5	7 34 BY
Symbol	INT0_7_IO_SEL	INTO_6_IO_SEL	INT0_5_IO_SEL	INTO_4_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INTO_3_IO_SEL	INTO_2_IO_SEL	INT0_1_IO_SEL	INTO_0_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

	~~	<b>D</b>	an	an
	Bit number	Bit symbol	Description	abyd. Cox
	pen(0), 170;	INTO x IO SEL	INTO x port selection enable	ben (0) 1 /6:2
E	7-94	$(x=7\sim0)$	1. Select INT function	ning. of M. VIII
(			0: Not select INT function	0///2

PERIPH IO SEL3 (36H) External port function selection register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	INT4_7_IO_SEL	_	_	_	_	_	_	_
R/W	R/W	_	_	_	_	_	_	_
Reset value	0	_	_	_	_	_	_	_

Bit number	Bit symbol	Description
		INT4_7 port selection enable
7	INT4_7_IO_SEL	1: Select INT function;
		0: Not select INT function
6~0		Reserved

PERIPH\_IO\_SEL4 (37H) External port function selection register 4

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	· // 10-				
Bit number	7	6~3	Der (3/0.3	1	pen 0/1/0.3
Symbol	INT4_15_IO_SEL	UIU.S.	INT4_10_IO_SEL	INT4_9_IO_SEL	INT4_8_IO_SEL
R/W	R/W		R/W	R/W	R/W
Reset value	0	_	0	0	0

Bit number	Bit symbol	Description
7, 2~0	INT4_x_IO_SEL (x=15, 10~8)	INT4_x port selection enable  1: Select INT function  0: Not select INT function
6~3		Reserved

PERIPH IO SEL5 (38H) External port function selection register 5

	( ) ( ) ( ) ( )	A STOREGIST SOLD AND A STOREGIST				
Bit number	7	6 hyd.	2.35 5	4 vd. 0		
Symbol	1,20.2	INT4_22_IO_SEL	INT4_21_IO_SEL	INT4_20_IO_SEL		
R/W	<u> </u>	R/W	R/W	ng RW		
Reset value	_	0000	0	0000		
Bit number	3	2	1	0		
Symbol	INT4_19_IO_SEL	INT4_18_IO_SEL	INT4_17_IO_SEL	INT4_16_IO_SEL		
R/W	R/W	R/W	R/W	R/W		
Reset value	0	0	0	0		

Bit number	Bit symbol	Description
7		Reserved
-01	INT4 x IO SEL	INT4_x port selection enable
6~00	$(x=22\sim16)$	1: Select INT function
( 50 (O)), 1 (2)	)0.5(X 22.410)	0: Not select INT function

EXT INT CON1 (39H) External Interrupt configuration register 1

Bit number	7	6	75/75	4	3	2		1/80
Symbol	INT3_POLARITY		INT2_POLARITY		INT1_POLARITY		INT08_POLARITY	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	1	0	1	0	1	0	1

Bit number	Bit symbol	Description
		External interrupt 3 trigger polarity selection:
	INT3 POLARITY	01: Falling edge (low level wake-up in Sleep mode)
7~6	INI3_POLARITY	10: rising edge (high level wake up in Sleep mode)
		00/11: Double edge (low level wake up in Sleep mode)
		External interrupt 2 trigger polarity selection:
- 41	INITO DOLADITY	01: Falling edge (low level wake-up in Sleep mode)
5~4	INT2_POLARITY	10: rising edge (high level wake up in Sleep mode)
y ·		00/11: Double edge (low level wake up in Sleep mode)

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$\overline{(0)}$	70.2	
pen 2 01 10	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	External interrupt 1 trigger polarity selection:
3~2	INITA DOLADITY	01: Falling edge (low level wake-up in Sleep mode)
	INT1_POLARITY	10: rising edge (high level wake up in Sleep mode)
		00/11: Double edge (low level wake up in Sleep mode)
		External interrupt 0-8 trigger polarity selection:
	INITOO DOL ADITY	01: Falling edge (low level wake-up in Sleep mode)
1~0	INT08_POLARITY	10: rising edge (high level wake-up in Sleep mode)
		00/11: Double edge (low level wake up in Sleep mode)

EXT INT CON2 (3AH) External Interrupt configuration register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	0 -	_	_	_	- 010	INT4_POLARITY	INTO_PO	DLARITY
R/W	62.03	_	_	- 🔿	19. CO.	R/W	R/W	R/W
Reset value	70.2	-	_	hen (d)	7 -16:	0	000	N I

Bit number	Bit symbol	Description Description					
	INT4	External Interrupt4_x trigger polarity selection:					
2	POLARITY	1: Rising edge (high level wake-up in Sleep mode)					
	POLAKITI	0: Falling edge (low-level wake-up in Sleep mode)					
		External Interrupt0_0~0_7 trigger polarity selection:					
1.0	INTO_	01: Falling edge (low level wake-up in Sleep mode)					
1~0	POLARITY	10: rising edge (high level wake up in Sleep mode)					
		00/11: Double edge (low level wake up in Sleep mode)					

SPI TX START ADDR (3EH) SPI high speed mode transmit buffer first address

Bit number 7	6	5	4000	2	1	19.00U
Symbol			John (":28:33			6
R/W		20. Perio	R/W	• ,	o perio	U/ 10.
Reset value	D)	1118 J.	0	71	71907-	

Bit number	Bit symbol	Description
7~0		In SPI high-speed mode, the first address of the transmit data buffer, SPI_TX_START_ADDR*16

SPI RX START ADDR (3FH) SPI high-speed mode receive cache header Address

		(0 ) ~									
Bit number	7	6	5	4	3	2	1	0			
Symbol		_									
R/W		R/W									
Reset value	1 com										

Bit number	Bit symbol	pente 1/10.30	Description	pental 110.
0200	)	In SPI high-speed mod	le, the first addre	ss of the receive data
7/~00		buffer, SPI_RX_STAR	AT_ADDR*16	J) 12

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SPI NUM L (40H) SPI high speed mode data cache address number low 8 bits

Bit number	7	6	ning 55 0 40	3	2 1100
Symbol			SPI_NUN	/L[7:0]	Mrs. Br.
R/W			R/	W	
Reset value			(	)	

Bit number	Bit symbol	Description
7~0	SPI_NUM_L[7:0]	SPI high speed mode data cache address number low 8 bits

SPI NUM H (41H) SPI high speed mode data cache address number high 4 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	<u>n</u>	-	ı	- c07	0	SPI_NU	M_H [3:0]	com
R/W	5.35	ı	-	abyd. Co	R/W	R/W	R/W	R/W
Reset value	20	-	benl	7/0	20.0	0	genl	0/0/:

Bit number	Bit symbol	Description BY
3~0	SPI_NUM_H[3:0]	SPI high speed mode data cache address number high 4 bits

ADC CFG SEL1 (42H) ADC comparator offset cancellation selection register

Bit number	7	6	5	4
Symbol	_	•	ADC_VREF_SEL	ADC_VREF_VOL_SEL
R/W	_	ı	R/W	R/W
Reset value	-	ı	0	0
Bit number	3	2	1	0
Symbol	VREF IN ADC SEL		C'	ΓRL_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	(0) 16:Do.	00000

0 1 10	7118	
Bit number	Bit symbol	Description Description
		ADC reference voltage selection:
5	ADC VREF SEL	0: Select VCC as the output signal;
5	ADC_VREF_SEL	1: Select the voltage output by the ADC_VREF module as the reference voltage.
	ADC VREF VOL SEL	ADC_VREF output mode selection:
		0: 2V as ADC reference voltage;
4		1: 4V as ADC reference voltage.
4	ADC_VKLI_VOL_SLL	When ADC_VREF output mode selects 2V/4V, it is
		recommended to select 3MHz for ADC frequency
		division clock
		Voltage selection input to the internal ADC channel of
3~2	VREF_IN_ADC_SEL	the chip
<b>y</b>		00: 1.362V; 01: 2.253V;

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(0)	.70.3	
pene Will	5.5	10: 3.111V; 11: 4.082V;
1~0	CTRL_SEL	ADC offset elimination timing selection, the default value is 10: 00/01: first offset elimination and then sampling; 10/11: offset elimination and sampling are performed at the same time, 10 first-stage comparator switches are turned off at the end;
		11: all switches are turned off at the same time open;

IIC FIL MODE (50H) IIC filter selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	Ω _	_	_	_	- (	m -	IIC_AFIL_SEL	IIC_DFIL_SEL
R/W	035	_	_	_	12/d. C	20-35	R/W	R/W
Reset value	20.2	_	_	1-02	00,7/1	1.20.3	1	1000 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

7				
(	Bit number	Bit symbol	Description	11 J-1 BYD
			IIC port analog filter selection enable	
	1	IIC_AFIL_SEL	1: Select analog filter function;	
			0: Not select analog filter function.	
			IIC port digital filter selection enable	
	0	IIC_DFIL_SEL	1: Select digital filter function;	
			0: Not select digital filter function.	

ADC IO SEL1 (53H) ADC select enable register 1

112 0 10 0221	( /							
Bit number	7	6	5	4	3	2	1	0
Symbol	25		_	ADC_IO_S	SEL1 [7:0]			y com
R/W	9:22			R/	W			6
Reset value		•,	va. perro	10) 10.	)	•	og. perio	W 10.

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL1 [7:0]	Enable the ADC control function that disables analog input pins
	[,]	1: Select ADC function;
		0: Not select ADC function
		00000001=ADC7; 00000010=ADC8
		00000100=ADC9; 00001000=ADC10;
		00010000=ADC11; 00100000=ADC12;
2 00%		01000000=ADC13; 10000000=ADC14

ADC IO SEL2 (54H) ADC select enable register 2

Bit number	7	6	500 4 0 3	2
Symbol		0	ADC_IO_SEL2 [7:	:0] ning of 1
R/W			R/W	7777

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Reset value

	,	
Bit number	Bit symbol	Description
7~0	ADC_IO_SEL2 [7:0]	Enable the ADC control function that disables analog input pins  1: Select ADC function;  0: Not select ADC function  00000001=ADC15; 00000010=ADC16  00000100=ADC17; 00001000=ADC18;  00010000=ADC19; 00100000=ADC20;  01000000=ADC21; 10000000=ADC22

ADC\_IO\_SEL3 (55H) ADC select enable register 3

Bit number	20.7	6	5,000,4\0,003	2	100000
Symbol			ADC_IO_SEL3[7:0]		vs. 2 1 11 10.
R/W		1/7	R/W	10	000
Reset value			0		MA

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL3 [7:0]	Enable the ADC control function that disables analog input pins  1: Select ADC function;  0: Not select ADC function  00000001=ADC23; 00000010=ADC24  00000100=ADC25; 00001000=ADC26;  00010000=ADC27; 00100000=ADC28;  01000000=ADC29; 10000000=ADC30

ADC IO SEL4 (56H) ADC select enable register 4

		(3011) 110	C SCICCI C	naoic regis				_ (	111111	
C	Bit number	7	6	15/23	4	3	2		77	0
	Symbol			-	ADC_IO_S	SEL4 [7:0]				
	R/W				R/	W				
	Reset value				(	)				

Bit number	Bit symbol	Description				
7~0 BVD	ADC_IO_SEL4 [7:0]	Enable the ADC control function that disables analog input pins  1: Select ADC function;  0: Not select ADC function  00000001=ADC31; 00000010=ADC32;  00000100=ADC33; 00001000=ADC34;  00010000=ADC35; 00100000=ADC36;				

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pen Will	, ,		01000000	)=ADC37;	10000000=ADC38				
ADC IO SEL5	(57H) AD	C select	nable regis	ter 5		71	050	10	
Bit number	7	6	73/13	4	3	2		0	
Symbol	_	_	_		ADC IO SEL5 [4:0]				
R/W	_	_	_		R/W				
Reset value	_	_	_			0			

Bit number	Bit symbol	Description
7~5		Reserved
4~0	ADC_IO_SEL5 [4:0]	Enable the ADC control function that disables analog input pins  1: Select ADC function;  0: Not select ADC function  00001=ADC39; 00010=ADC40;  00100=ADC41; 01000=ADC42;  10000=ADC43;

LED IO START(58H) LED scan start selection register

	(, —							
Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	_	_
R/W	_	_	_	_	_	R/W	R/W	R/W
Reset value	_	_	_	_	_	0	0	0

Bit number	Bit symbol	Description
-1-1/d. COM		LED port serial dot matrix start PAD selection (only for
1 = (0)0 / 1		LED serial dot matrix scan, and DUTY_SEL[2] needs to be
DC		configured to 0)
RID	ζ,	000: PB0 port;
		001: PB1 port;
		010: PB2 port;
2~0		011: PB3 port;
		100: PB4 port;
		101: PB5 port;
		110: PB6 port;
		111: PB7 port;
~0		See the table "LED dot matrix drive LEDX arrangement order"

PWM IO SEL1 (59H) PWM port selection register, 1

Bit number	$\begin{array}{c c} 7 & 6 \end{array}$	5	4 (	3	2	100	0(:5
Symbol		: 25: - C	1 7) I	_	_	72 V	W. ro
R/W)		2002	<b>)</b> '	R/W	R/W	R/W)	R/W
10						70-	

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(11)6, (2)		111)	1 1100		
Reset value _	- Den	W/	0	0	(10)0.

202-0, 21 D	<u> </u>	
Bit number	Bit symbol	Description
3	PWM_IO_SEL[3]	PWM1E selection enable
		1: PWM1E function is selected;
		0: PWM1E function is not selected
		When PWM1E and PWM0_A are configured at the same time, PWM0A is valid and PWM1E is invalid
2	PWM_IO_SEL[2]	PWM1D selection enable
		1: PWM1D function is selected;
		0: PWM1D function is not selected.
		When PWM1D and PWM0_B are configured at the same time, PWM0B is valid and PWM1D is invalid
1	PWM_IO_SEL[1]	PWM0E selection enable
		1: PWM0E function is selected;
		0: PWM0E function is not selected
0	PWM_IO_SEL[0]	PWM0D selection enable
		1: PWM0D function is selected;
		0: PWM0D function is not selected

FLASH BOOT EN (5AH) BOOT mode status register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	_	FLASH_BOOT_EN
R/W	~ -	_	_	_	- ~	_	_	R
Reset value	25	_	_	_	y com	25-	_	0 d com

	~(00).	1,100	V(0),
5	Bit number	Bit symbol	Description Description
7	102-0 BIN	UI	1: Indicates that the Flash BOOT upgrade mode has been entered,
			0: Indicates that the Flash BOOT upgrade mode has been exited.
	0	FLASH_BOOT_EN	Note: In Flash BOOT upgrade mode, SPROG_ADDR_H, SPROG_ADDR_L, SPROG_DATA, SPROG_CMD, SPROG_TIM are reused as BOOT upgrade function.
			{SPROG_ADDR_H, SPROG_ADDR_L} are multiplexed into all Flash space addresses from 0x0000 to 0xFFFF.

EEP SELECT (5BH) DATA area selection register

Bit number 7	6	5 4	33	2	1 (	10490 50
Symbol	_	ben and	P. 20.	_	bend	7/0:3
R/W	_ <	ms - 11-11	_	- ×	1128 C	R/W
Reset value _	_	J0.172	_	_	JO 1.2.	0

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Bit number	Bit symbol	Description ning of the description
Mrs Br		1: Select NVR3 and NVR4 as DATA area
0		When SPROG_ADDR_H[2]=1, select NVR4; When SPROG_ADDR_H[2]=0, select NVR3
		0: Select address (0xFC00~0xFFFF) as DATA area, 1 page

PWM0 POLA SEL (60H) PWM0 polarity selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	ı	_	_	_	_	_	_
R/W	_	ı	_	R/W	R/W	R/W	R/W	R/W
Reset value	Ω _	-	_	0	0	0	0	0.00

		, (1)		
	Bit number	Bit symbol	Description	ben (0) 1 / (1)
Z	7~5		Reserved	ving: " Will to
(	152-0.	<b>\</b>	PWM0E output polarity selection	105-01
	4		1: Reverse output; 0: Normal output	LIVE .
			PWM0D output polarity selection	
	3		1: Reverse output; 0: Normal output	
			PWM0C output polarity selection	
	2		1: Reverse output; 0: Normal output	
			PWM0B output polarity selection	
	1		1: Reverse output; 0: Normal output	
			PWM0A output polarity selection	M
	0 7 00		1: Reverse output; 0: Normal output	y com

PWM1 POLA SEL (61H) PWM1 polarity selection register

Bit number	7	6	25 5 EL	7 14 10	3	2	Lag. Per	1/6/10.
Symbol	1	_ <	JII. 605	JI BYD	-	<u>-</u>	JII. 0017	11/250
R/W	-	_		R/W	R/W	R/W	R/W	R/W
Reset value	_	_	_	0	0	0	0	0

Bit number	Bit symbol	Description			
7~6		Reserved			
4		PWM1E output polarity selection			
		1: Reverse output; 0: Normal output			
3		M1D output polarity selection			
		1: Reverse output; 0: Normal output			
2		PWM1C output polarity selection			
		1: Reverse output; 0: Normal output			
10		PWM1B output polarity selection			
V F		1: Reverse output; 0: Normal output			

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PWM1A output polarity selection
1: Reverse output; 0: Normal output

XTAL CLK SEL (63H) Crystal frequency selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	-	_
R/W	_	_	_	_	_	_	_	R/W
Reset value	_	_	_	_	_	_	_	0

Bit number	Bit symbol	Description	
		Crystal frequency selection register	
0	<u></u>	1: Select 4MHz;	com
abyd. ce	0.35	0: Select 32768Hz	abyd. ce

SEL LVDT DELAY (65H) LVDT delay control register-

5.	Bit number	7	6	n85 N	1.114	3	2	1 1	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\
7	Symbol	_	_	JOJ 75-	BY	_	_	000 2-	BI
	R/W	_	_	_	_	_	_	R/W	R/W
	Reset value	_	_	_	_	_	_	0	0

Bit number	Bit symbol	Description
		Select signal, select LVDT power-down delay
1~0	SEL_LVDT_DELAY	00: Delay time 1; 01: Delay time 2;
		10: Delay time 3; 11: Delay time 4

BOR SEL (66H) BOR control register

Bit number	75	6	5	4	3.25	2	1 10.0
Symbol	76.2	_	_	-	SEL_BOR_DELAY	SEI	_BOR_VTH
R/W	_	_	_	in	R/W	ing	R/W
Reset value	_	_	_	The	0	Dire	100-0

Bit number	Bit symbol	Description				
3	SEL_BOR_DELAY	Select the signal, select the power-down delay of BOR 0: Delay time 1; 1: Delay time 2				
2~0	SEL_BOR_VTH	BOR threshold selection 00x: 2.3V; 010: 2.8V; 011: 3.3V; 100: 3.7V; 1xx: 4.2V;				

UART BD EXT (67H) UART0/1/2 baud rate configuration extension bit register

	Bit number 7	6	5	4000	2	1	y COUL
	Symbol	_	- ~(0	10/0. (28:3)	_	- ~ (6)	070.
5	R/W		perio	W.10.	-	or perior	R/W
ار م	Reset value _	- D	1118		- D1,	12002-1	0
	Mrs D		100			1777	

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Bit number	Bit symbol	Description Description
022-0		UARTO/1/2 baud rate configuration extension bit selection 1: Select the baud rate to extend to 12 bits;
		0: Select the baud rate without extension to maintain 10 bits

SPI IO SEL (68H) SPI communication port selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	ı	_	_	-	SPI_IO_	SEL[1:0]
R/W	_	_	ı	_	_	_	R/W	R/W
Reset value	_	_	1	_	_	-	0	0

	Bit number	Bit symbol	Description	com
	abyd. Co	8.35	SPI communication port selection regi	ster abyd.
	pen 1. 0/ 1/2.	SPI IO SEL[1:0]	01: PC2/3/4/5 selects SPI function	pen 01 /6:3
Q.			10: PE4/5/6/7 selects SPI function	ning of Mills
		<i>&gt;</i>	00/11: PG0/1/2/3 selects SPI function	1 2-0

SPI MCLK MOD (69H) SPI master mode receiver clock selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	_	_
R/W	_	_	_	_	_	_	_	R/W
Reset value	_	_	_	_	_	_	_	0

Bit number Bit symbol		Description				
4 60%		SPI master mode receiver clock selection register				
000	8:32	<ul><li>1: Select the host output as the receive clock;</li><li>0: Select the PAD port input as the receive clock</li></ul>				

BOOT CMD (6AH) Program space jump instruction register

Bit number	7	6	7 3 5 84 0	3	2				
Symbol									
R/W		R/W							
Reset value	0								

Bit number	Bit symbol	Description
		Configure the program space jump instruction, write 5 groups of data continuously (0xFF, 0x00, 0x88, 0x55,
7~0	58:355 	0xAA), jump into the main program space; write 5 groups of data continuously (0x37, 0xC8, 0x42, 0x9A, 0x65), Jump into the Boot program space; the value read out is the byte written recently.

ROM OFFSET L (6BH) Address offset of CODE area, low 8 bits

V-1-1-0-11-1	( ) .		( _ ( _ ( _ ( _ ( _ ( _ ( _ ( _ ( _				0,1,1,0	
Bit number	7	6	15/2	4	3	2		0

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Bit number	Bit symbol	Description
7~0		Address offset of CODE area (low 8 bits)

ROM OFFSET H (6CH) Address offset of CODE area, high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	_							
R/W	R							
Reset value	000						com	

Bit number Bit symbol	Description Description	16.
(7~0)	Address offset of CODE area (high 8 bits)	

#### Note:

- 1. ,-,: Reserved;
- 2. The reserved register and the reserved bit of the register are forbidden to write, otherwise it may cause the chip to be abnormal.

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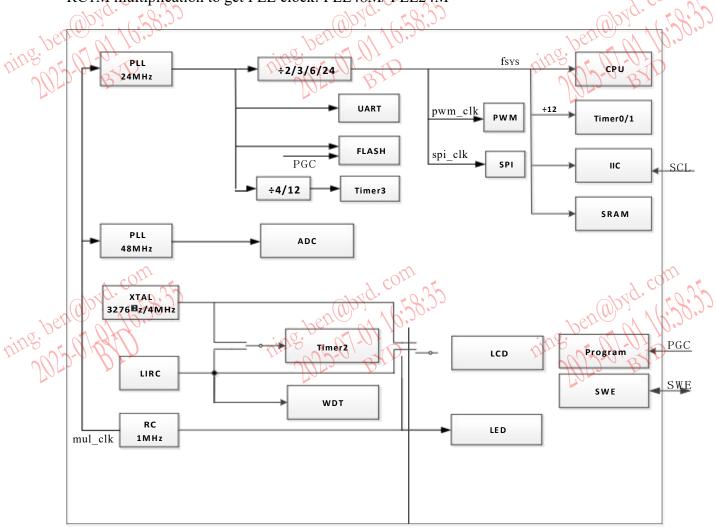
## 5. Clock, Reset, Working Mode and Watchdog

#### 5.1. Clock

#### 5.1.1. Introduction

#### Clock source:

- ' Internal high-speed RC oscillator: RC1M
- ' Internal low-speed RC oscillator: LIRC32k
- External crystal oscillator: 32768 Hz/4 MHz
- RC1M multiplication to get PLL clock: PLL48M/PLL24M



Clock block diagram

The BF7515CM44-LJTX series clock is defined as follows:

RC1MHz: Built-in RC oscillator, RC1MHz is used as LCD/LED Driver clock.

**PLL\_24MHz**: The 24MHz clock generated by the phase-locked loop is used as the main system clock after frequency division.

f<sub>SYS</sub>: PLL\_24MHz clock divided by frequency, the frequency is 12MHz/8MHz/4MHz/1MHz.

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pwm\_clk: PWM working clock, frequency 12MHz/8MHz /4MHz/1MHz optional. spi\_clk: SPI working clock, frequency 12MHz/8MHz /4MHz/1MHz optional.

PLL\_48MHz: The 48MHz clock generated by the phase-locked loop is used as the clock source of ADC.

XTAL32768Hz/4MHz: External precision clock, can be used as Timer2 or LCD Driver clock.

LIRC: The internal low-speed clock is 32 kHz, which is used as watchdog clock, Timer2 clock or LCD Driver clock.

**SCL:** The frequency is 100 kHz/400 kHz, as the IIC communication clock.

**PGC:** Flash programming clock, frequency range 100 kHz~5MHz, download clock when programming and burning programs.

#### 5.1.2 Registers

perio M	10.2	perion 1/10.		
Address	Name Name	RW	Reset	Description
0x84	TIMER3_CFG	RW	xxxx_x000b	TIMER3 configuration register
0x93	TIMER2_CFG	RW	xxxx_x000b	TIMER2 configuration register
0xAD	SYS_CLK_CFG	RW	xxx0_1000b	System clock configuration register

Secondary bus register							
Address Name RW Reset Description							
0x2D	PD_ANA	RW	x111_xx11b	Analog module switch register			
0x30	IDLE_WAKE_CFG	RW	xxxx_x111b	System wake-up configuration register			
0x63	XTAL_CLK_SEL	RW	xxxx_xxx0b	Crystal frequency selection register			

SYS CLK CFG (ADH) System clock configuration register

	Bit number	7~5	4 bent	(3)0.	2	1	pen on 10.
2	Symbol	_	IMO EN	PL	L_CLK_S	EL Ç	PD_SYS_CLK
	R/W	_	R/W	R/W	R/W	R/W	R/W
	Reset value	_	0	1	0	0	0

Bit number	Bit symbol	Description
7~5		Reserved
3~1	PLL_CLK_SEL	PLL clock divider selection register: 000/100: 12MHz; 001/101: 8MHz; 010/110: 4MHz; 011/111: 1MHz
0PMD	PD_SYS_CLK	Core clock enable 0: Turn on core working clock; 1: Turn off core working clock

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TIMER2 CFG (93H) TIMER2 configuration register

Bit number	7~4	3 ning	2	1 ning	
Symbol	ı	TIMER2_CNT_MOD	TIMER2_CLK_SEL	TIMER2_RLD	TIMER2_EN
R/W	_	R/W	R/W	R/W	R/W
Reset value	_	0	0	0	0

Bit number	Bit symbol	Description
		Timer2 clock select register
2	TIMER2_CLK_SEL	1: Select XTAL32768Hz/4MHz;
		0: Select LIRC

TIMER3 CFG (84H) TIMER3 configuration register

Bit number 7~3	2010	1 1	ONG. CO.
Symbol _	TIMER3_CLK_SEL	TIMER3_RLD	TIMER3 EN
R/W _	ing R/W	R/W	n.S. R.W.
Reset value _	2000	0	10,529

Bit number	Bit symbol	Description
		TIMER3 timing clock selection register
2	TIMER3_CLK_SEL	1: Select clk_24M/4;
		0: Select clk_24M/12

#### Secondary bus register

PD ANA (2DH) Module switch control register

Bit number	7	6	5	4	3~1	0
Symbol	2	PD_LVDT	1 21 g. COr	PD_XTAL_32K	-	PDADC
R/W	), )	R/W	$(0)^{1-1}(0)$	R/W		OR/W
Reset value	-	:46.	201 10.	1	12. pc	

Bit number	Bit symbol	Description
4	PD_XTAL_32K	PA port crystal oscillator circuit (32768Hz/4MHz) control register 1: Off; 0: On, default off

XTAL CLK SEL (63H) Crystal frequency selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_		_	_	-	- 0
R/W	77	_	_	7-cou	05-	_	-	R/W
Reset value	8:23	_	- ^(0	pyd.	8:23	_	(0)	070.0

Bit number	Bit symbol	Description	ning of Old
0		Crystal frequency selection register	

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1: Select 4MHz; 0: Select 32768Hz

IDLE WAKE CFG (30H) System wake-up configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_		_	_	PLL_WAKE_TIM		
R/W	_	_	-	_	_	R/W		
Reset value	_	_	_	_	_	1	1	1

Bit number	Bit symbol	Description
2~0	PLL_WAKE_TIM	When PCON=1, wake-up PLL timing time
		000: 0.2ms;
		001: 0.3ms;
		010: 0.4ms;
		011: 0.5ms;
		100: 0.6ms;
		101: 0.7ms;
		110: 0.9ms;
		111: 1ms

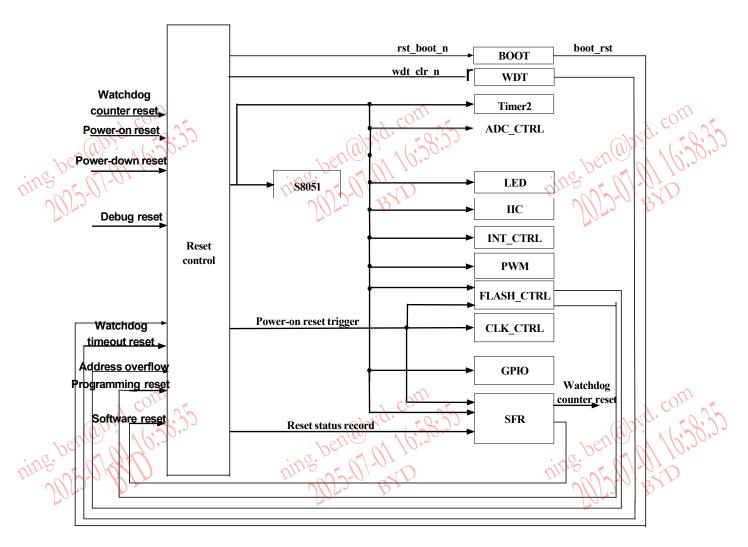
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#### 5.2. Reset System

There are eight reset modes in the BF7515CM44-LJTX: power-on reset, power-offreset, programming reset, software reset, modify configuration reset, watchdog timer overflow reset, PC pointer overflow reset, ROM address jump reset. Any one of above reset, global will make chip reset. We can judge the reset flag register which reset happen, the reset must be cleared by software.

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Reset block diagram

#### **5.2.1. Reset Sequence**

**po\_n:** Power-on reset. After the system is powered on, the analog module generates a low-level signal and lasts for 93ms. When the power-on reset is low, the entire chip is in the reset state, and after the global reset signal continues to be effective 20ms after the power-on reset is high, the system exits the reset mode.

bo\_n: brown-out reset. The analog module generates a low-level signal after the system has a

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power-down reset. When the power-down reset signal is low, the entire chip is in the reset state. After the global reset signal becomes high, the system exits the reset mode after the global reset signal continues to be valid for 20ms.

**soft\_rst: software reset**. The soft reset signal is valid by writing SFR, and the global reset signal is valid for 20ms. After 20ms, the system exits the reset mode.

**prog\_en: programming reset.** When prog\_en is high, it is the programming mode of FLASH. At this time, the global reset signal is valid. After it goes low, the global reset signal continues to be valid for 20ms.

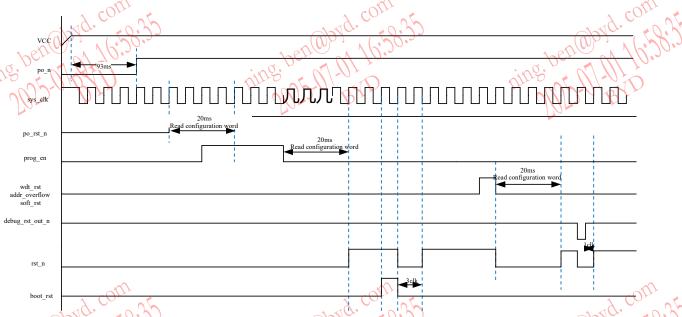
wdt\_rst: The watchdog timer overflow reset. After the watchdog timer overflows, the global reset is 20ms. After 20ms, the system exits the reset mode.

addr\_overflow: PC pointer overflow reset. If the PC pointer exceeds the valid address range of the flash when the MCU addresses the program memory, the addr\_overflow signal becomes high, and the sys\_clk clock rising edge detects the high level of addr\_overflow (requires 1 clock cycle) and resets the global 20ms, the reset signal will clear the addr\_overflow signal to zero. After 20ms, the system exits the reset mode.

**debug\_rst\_out\_n: trim configuration reset,** output a reset signal for the core trim module, low means reset is effective, chip global reset, but there will not be a 20ms initialization process, only delay 1 system clock reset low level.

**boot\_rst:** ROM Address jump reset, the boot\_rst signal becomes high after the complete ROM space jump instruction is configured, and the sys\_clk clock checks the boot\_rst high level (valid for one clock cycle) to reset the global, but there will be no 20ms read configuration word process. Only delay the reset low level of 3 System clocks.

Reset sequence description:



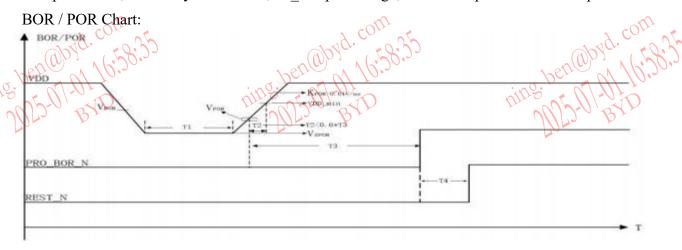
- 1. The chip has a power-on reset, and the analog POR module delays for 93ms, and poin is pulled high.
- 2. The programmer sends instructions to make the chip enter the programming mode (prog\_en is pulled high). In the programming mode, the system is in a global reset state. After the

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programming is completed, the programming mode is exited. After a delay of 20ms, rst n is pulled high and the chip enters normal operation.

- 3. During normal operation, any one of watchdog reset, address overflow reset, soft reset, ROM address jump reset occurs, rst\_n is pulled low, after a delay of 20ms, rst\_n is pulled high, and the chip enters normal operation.
- 4. After normal work, you cannot enter the programming mode.
- 5. In debug mode, configure debug reset, pull down rst\_n, pull up 1 system clock in debug rst out n, pull up rst n, and the chip enters normal operation.
- 6. When the chip supports the BOOT upgrade function, a ROM Address jump reset occurs, rst\_n is pulled low, after 3 System clocks, rst\_n is pulled high, and the chip enters normal operation.



BOR/POR chart diagram

BOR/POR reset parameters:

Symbol	Parameter -		Conditions temperature	Min	Тур	Max	Unit
Vspor	Power on reset start voltage	$\widehat{m}_{i}$	\(\)25°C	_	- 1	300	mV
Kpor	Power on reset voltage rate	10.00	25°C	0.01	ing.	172	V/ms
VPOR	Power on reset voltage		25°C	1.1	1.5	2.2	V
V <sub>BOR</sub>	Brownout reset voltage (±10%), hysteresis 0.2V	-	25°C	-	VBOR	-	V
VDD_min	Minimum operating voltage		25°C	2.7	_	_	V
T1	VDD keep VSPOR time		25°C	0.1	_	ı	ms
T2	VPOR from VDD_min time	_	25°C	_	_	0.6*T3	ms
T3	Reset POR_BOR_N duration		25°C	55	93	131	ms
T4	Global reset effective time	_	25°C	_	20	_	ms

Power on reset parameter characteristic table

Note: VBOR power-down reset voltage is selected by register BOR SEL [2:0].

When VDD is affected by the load or severely disturbed, if the voltage drops into the voltage dead zone and the chip is not within the working voltage range, it may cause the system to work abnormally. The function of power-down reset (BOR) is to monitor when VDD drops to the BOR voltage, the MCU can generate a power-down reset in advance to avoid system errors.

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Suggestions to prevent entering the voltage dead zone and reduce the probability of system error: Increase the voltage drop slope

#### 5.2.2. Registers

	SFR register							
Add	lress	Name	RW	Reset	Description			
0x8I	Ξ	SOFT_RST	RW	0000_0000b	Soft reset register			

Secondary bus register							
Address Name RW		Reset	Description				
0x0F	RST_STAT	RW	0000_0010b <sup>2</sup>	Reset flag register	y Gy. Corr		
0x66	BOR_SEL	RW	xxxx 0000b 3	BOR control register	7.00		

- 2: The power-on reset is 1. Other resets: Reset to 0 after power-on and 1 after corresponding reset.
  - 3: The register is reset after power-on. Other resets do not change the configuration value.

SOFT RST (8EH) Soft reset register

Bit number	7	6	5	4	3	2	1	0		
Symbol		SOFT_RST[7:0]								
R/W		R/W								
Reset value				(	)					

Bit number	Bit symbol	Description
7~0	SOFT_RST[7:0]	Soft reset register, only when the register value is 0x55, the software reset is generated

#### Secondary Bus Register:

Secondary Bus	100			$\sim (0)$	0,40.50	2000 V ( 2000 C			
BOR SEL (66H	BOR SEL (66H) BOR control register								
Bit number	7	6	3178	4	3	2111900			
Symbol	_	_	_		SEL_BOR_DELAY	SEL_BOR_VTH			
R/W	_	_	_	_	R/W	R/W			
Reset value	_	_	_	_	0	0			

Bit number	Bit symbol	Description
3	SEL_BOR_DELAY	Select the signal, select the power-down delay of BOR 0: Delay time 1; 1: Delay time 2
2~0 co	SEL_BOR_VTH	BOR threshold selection 00x: 2.3V; 010: 2.8V; 011: 3.3V; 100: 3.7V; 1xx: 4.2V;

				11-	
	CELL DOD DEL AV	SEL DOD VIII	BOR	ning of (	
1	SEL_BOR_DELAY	SEL_BOR_VTH Power down	Recovery	Hysteresis	Delay

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threshold (V) threshold (V) (mV) (µs) 000 ning 2.3 143 2.4 68.1 143 001 2.3 2.4 68.1 010 2.8 2.9 140 84.5 0 011 3.3 145 98.3 3.4 100 108 3.7 3.8 120 101/110/111 4.2 4.3 130 118.1 000 2.3 2.4 135.2 146 001 2.3 2.4 146 135.2 168.5 010 2.8 2.9 144 011 3.3 150 196.5 3.4 3.7 127 216 100 3.8 101/110/111 4.2 4.3 1350 236.3

RST STAT (0FH) Reset flag register

Bit number	7	6	1023	8 4	3	2	JUJ-7	Bo
Cymah al	BOOT_	DEBUG_	SOFT_	PROG_	ADD	BO F	PO F	WDT
Symbol	F	F	F	F	ROF_F	BO_F	PO_F	RST_F
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	1	0

Bit number	Bit symbol	Description
7	BOOT_F	<ul><li>0: No effect;</li><li>1: A reset occurs when the configuration program space jumps.</li></ul>
6	DEBUG_F	0: No effect; 1: trim configuration reset occurred.
5	SOFT_F	0: No effect; 1: software reset occurred.
4	PROG_F	0: No effect; 1: program reset occurred.
3	ADDROF_F	0: No effect; 1: PC pointer overflow reset occurred.
2	BO_F	0: No effect; 1: Power_down reset occurred.
1	PO_F	0: No effect; 1: Power_on reset occurred.
0	WDTRST_F	0: No effect; 1: watchdog timer overflow reset occurred.

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#### 5.3. Working Mode



# ning ben @ 10:58

#### 5.3.1. Introduction

BF7515CM44-LJTX series working mode: active mode, standby mode.

BF7515CM44-LJTX provides SYS\_CLK\_CFG register, configure Bit4 of this register to control MCU to enter idle mode 0. BF7515CM44-LJTX provides PCON register, configure Bit0 of this register to control MCU to enter idle mode 1.

#### **Active Mode**

RC1M, PLL, LIRC work, XTAL depends on software configuration. The core runs, the peripherals keep working normally, and the functions of each peripheral are controlled by software configuration.

#### Standby mode is divided into idle mode 0 and idle mode 1

#### Idle Mode 0

RC1M, PLL, LIRC work, XTAL depends on software configuration. The core stops running, the UART, PWM, SPI peripherals do not work, and the rest of the peripherals can work.

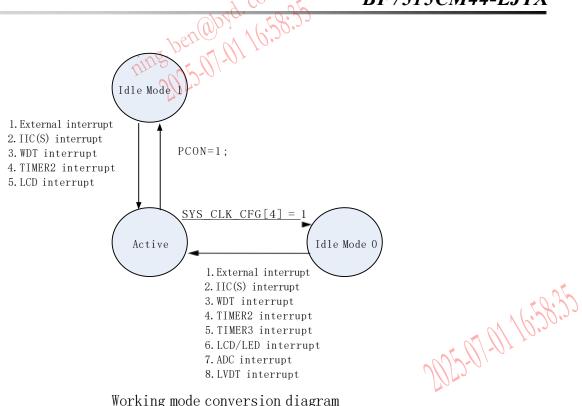
#### **Idle Mode 1**

RC1M and PLL are off, LIRC works, XTAL depends on software configuration. The core is stopped and the peripherals work fine using the LIRC clock.

Mode	Conditions	Effect	t on clock results
		RC1M	Work
		PLL	Work
Active Mode	Wake-up from power-on	LIRC	Work
	reset/standby mode	XTAL32K/4M	Depends on software configuration
		RC1M	Work
	SYS_CLK_CFG[4] =1	PLL	Work
Idle Mode O		LIRC	Work
		XTAL32K/4M	Depends on software configuration
		RC1M	Close
		PLL	Close
Idle Mode 1	PCON=1	LIRC	Work
		XTAL32K/4M	Depends on software configuration

The working state of the clock source in each mode

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Working mode conversion diagram

#### 5.3.2. Low power management

All CPU states are saved before entering standby mode, SRAM and register contents are preserved, and GPIOs remain in run-time state. In addition, all modules can be individually configured to close the gate, thereby reducing power consumption.

The working status of BF7515CM44-LJTX series is shown in the following table

NO	Module Name	Clock source	Active Mode	Idle Mode 0	Idle Mode 1
1	\$8051	fsys	16:28:33	×	× 00/
2	UARTO~1	PLL_24M	0) 10.	× .,, g.	0× ~ U/ 10.
3	PWMO~3	PLL_48M	0	× mire	(X-1)/-3
4	Timer0	fsys	0	×	
5	Timer1	fsys	0	×	×
6	Timer2	LIRC/ XTAL	0	0	0
7	Timer3	PLL_24M	0	0	×
8	LED	RC1M	0	0	×
9	LCD	LIRC/XTAL/RC1M	0	0	0
10	WDT	LIRC	0	0	0
11	ADC_CTRL	PLL_48M	0	0	×
12	IIC(S)	$f_{ ext{SYS}}$	0	0	0
13	SPI	PLL_48M	0	0	×

Note: , According Configuration

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#### Ways to exit the Idle Mode 0:

Enabling any one of IIC, External Interrupt 0/1/2/3/4, WDT, Timer 3, Timer 2, LCD, LED, ADC, LVDT to wake up the chip; Exit the Idle Mode 0, and the CPU executes the interrupt service routine.

#### Ways to exit Low power mode:

Enabling IIC, External Interrupt0/1/2/3/4, WDT, Timer2, LCD interrupt generation can wake up the chip; Exit Low\_power mode, after the interrupt response is generated. The CPU executes the interrupt service program related to the interrupt vector, and returns to the next instruction after the execution of the RETI return instruction to make the CPU enter the Low\_power mode to continue running the program.

### 5.3.3. Register

SYS CLK CFG (ADH) System clock configuration register

Bit number	7~5	1411805-	30	2	1 5	MS OF D
Symbol	_	IM0_EN	PL	L_CLK_S	EL	PD_SYS_CLK
R/W	_	R/W	R/W	R/W	R/W	R/W
Reset value	_	0	1	0	0	0

Bit number	Bit symbol	Description
4	IM0_EN	Idle Mode 0 enable 1: Enter Idle Mode 0; 0: Exit Idle Mode 0

PCON(87H) Idle mode 1 select register

Bit number 7	6	5	8:33	2	1	01/0, co
Symbol	_	pen 01 10.	_	-	bente	IM1_EN
R/W	- "	1118.0201-01	ı	- 0	11.8	R/W
Reset value _	_		ı	_	1/1/2	0

Bit number	Bit symbol	Description
7~1		Reserve
0	IM1_EN	Idle Mode 1 Enable 1: Idle mode 1; 0: Active mode, automatically cleared after wake-up Note: The software delay must be ≥100μsafter wake-up, otherwise the wake-up function is abnormal



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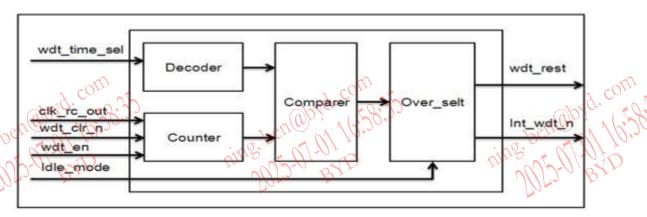


5.4. WDT

#### 5.4.1. Introduction

The watchdog timer counting circuit uses the internal low-speed clock LIRC for timing, and the configurable timing time is  $2^n*18ms$  (n=0, 1, 2, 3, 4, 5, 6, 7) ----- here n is the configuration value of the timing configuration register.

ning. ben abyd com



Due to the particularity of the system application, the watchdog timer overflow signal is classified:

In the normal working mode, if the watchdog timer overflow occurs, the overflow signal is the watchdog overflow reset signal at this time, and the watchdog overflow reset affects the global reset. At this time, the system realizes the global reset action and reloads the configuration information;

In the idle mode 1, if a watchdog timer overflow occurs, the overflow signal is the watchdog interrupt signal at this time, and the interrupt wakes up the chip to exit the idle mode 1 and execute the watchdog interrupt service function.

The watchdog module is a timing counting module. Its count clock is the internal low-speed clock LIRC. Its timing clear signal is composed of global reset and configuration clear. This signal is synchronously released by the watchdog timing clock in the reset module; The clearing action is generated every time the CPU configures the watchdog timer configuration register (WDT\_CTRL), and the watchdog restarts timing; at the same time, the watchdog counter has the watchdog count enable control, when the count enable is valid, After the watchdog generates a timing overflow (reset or interrupt), as long as the watchdog counting enable is not turned off, the watchdog counter will restart counting.

#### 5.4.2. WDT Related Register

COLLE		COLL	COLL
27.75		SFR register	byd. co
Address	RW	Reset	Description Co.
0x91 WDT_CTRL	RW	xxxx x000b Watc regist	hdog overflow timing configuration er

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0x92	WDT_EN	RW	0000_0000ь	WDT timing enable configuration register
0xAE	INT_PE_STAT	RW	0000_0000Ь	Interrupt status register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register1

#### WDT SFR register list

WDT CTRL (91H) Watchdog overflow timing configuration register

WD1 CTRE (7111) Watchdog Overnow thining configuration register								
Bit number	7	6	5	4	3	2	1	0
Symbol	_	-	_	_	_	WDT_TIME_SEL		SEL
R/W	_	_	_	_	_		R/W	
Reset value	0		_		-		0	com

(4)111		
Bit number	Bit symbol	Description Description
2-0	WDT_TIME_SEL	Watchdog overflow timing configuration register, the timing
JO DO	<i>&gt;</i>	length is as follows:
		0x00: 18ms; 0x01: 36ms;
		0x02: 72ms; 0x03: 144ms;
		0x04: 288ms; 0x05: 576ms;
		0x06: 1152ms; 0x07: 2304ms;

The watchdog uses the internal low-speed clock LIRC to complete the timing function and can achieve timing from 18ms to 2.3s. The timing length is controlled by SFR (WDT\_CTRL).

WDT EN (92H) Watchdog timer enable configuration register

	,	0		,	,			
Bit number	7	6	5	4	3	2	1	0
Symbol	,			, WD1	Γ_EN			y. com
R/W			200	R/	W		0	7.5
Reset value			va. per	(	)	°, i	va. per	Win.

Turn off WDT when writing 0x55, write other values to enable WDT, the WDT always works after the reset is over. Clearing the WDT is done by writing to the WDT\_CTRL register. Whichever values is written to this register will clear the WDT.

INT PE STAT (AEH) Interrupt status register

Bit number	7	6	5	4
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
		<del>-</del>	_	•
Symbol O	INT_TIMER2_STAT	INT_PWMQ_STAT	INT_LCD_STAT	INT_LED_STATE
Symbol CO	INT_TIMER2_STAT  R/W	INT_PWM0_\$TAT	INT_LCD_STAT  R/W	INT_LED_STATE
40.	0 R/W	INT_PWMO_STAT	INT_LCD_STAT  R/W  0	INT_LED_STATE

Bit number Bit symbol Description

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INT\_WDT\_STAT

WDT interrupt status flag, this bit is cleared by writing 0 to zero, and it can also be cleared by writing WDT\_CTRL.

1: Interrupt is valid; 0: Interrupt is invalid

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	_	_
R/W	R/W	R/W	R/W	R/W	R/W	R/W	_	_
Reset value	0	0	0	0	0	0	_	_

	Bit number	Bit symbol	Description	om
	abyd. Co	0.35	WDT/Timer2/PWM0 interrupt enable	abyd. co
	2007, 16	EX7	1: WDT/Timer2/PWM0 interrupt enable;	Petr (0) 1 / (1)
Ę	00		0: WDT/Timer2/PWM0 interrupt disable	00 11 11 10.

IRCON1 (F1H) Interrupt flag register 1

	1	0 0	, 11 1 1 2 -	<b>\</b> /			\ <b>\ \ \</b> \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	<b>\</b> /
Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	_	IE4	IE3	IE2	_	-
R/W	R/W	R/W	_	R/W	R/W	R/W	-	_
Reset value	0	0	_	0	0	0		_

Bit number	Bit symbol	Description
		WDT/Timer2/PWM0 interrupt flag
7	IE7	1: With interrupt flag;
2 cox	105	0: Without interrupt flag

IPL1 (F6H) Interrupt priority register1

Bit number	7	6	5 Serry	7 (4 )0	3	2	Deriver 1	(0/)	900
Symbol	IPL1.7	IPL1.6	TILE OF	IPL1.4	IPL1.3	IPL1.2 \( \sqrt{2} \)	TILE COL	1/-0,	
R/W	R/W	R/W		R/W	R/W	R/W	1777	_	
Reset value	0	0	-	0	0	0	_	_	

Bit number	Bit symbol	Description
	7 IPL1.7	WDT/Timer 2/PWM0 interrupt priority bit
7		1: WDT/Timer 2/PWM0 interrupt is high priority;
		0: WDT/Timer 2/PWM0 interrupt is low priority

BYD

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6. GPIO

Some pins of the GPIO port are multiplexed with device peripheral functions, and cannot be configured as multiple clock functions at the same time, otherwise it will cause malfunction. IIC communication port, open-drain output, pull-up resister required.

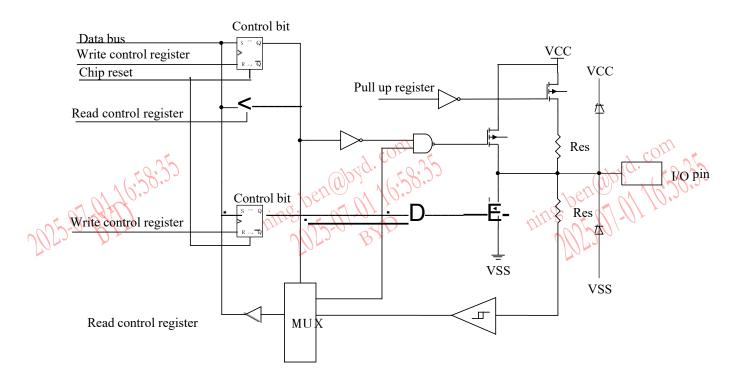
TRISX register (Direction Register): TRISX set to 1 can be configured as input pin, set to 0 can be configured as output pin.

DATAX register (Data Register): DATAX set to 1 the data in DATAX will be configured as high, set to 0 the data in DATAX will be configured as low.

PU\_PX register (pull-up resistor enable register): the pin corresponding to PU\_PX is set to 1 is enabled, and the corresponding pin is cleared to disable the pull-up resistor, and the pull-up resistor is 35k.

ODRAIN\_EN register: Set ODRAIN\_EN to 1 to enable open-drain output on the corresponding pin. Clear it to disable open-drain output. After enabling IIC function, open-drain output is automatically turned on. IIC/UART recommends using external pull-up resistors.

Supports high current drive function of 8 GPIO ports.

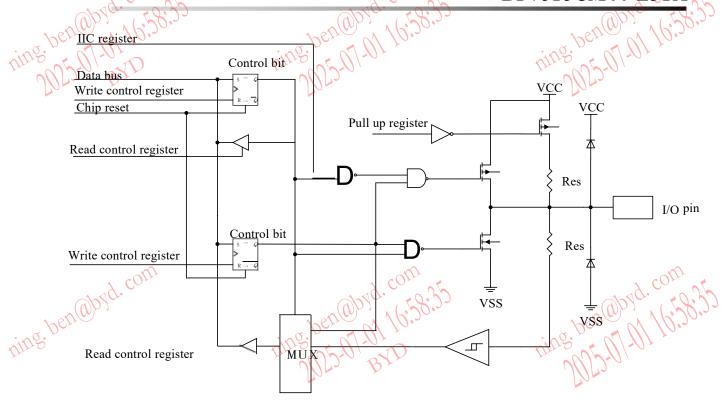


General IO structure

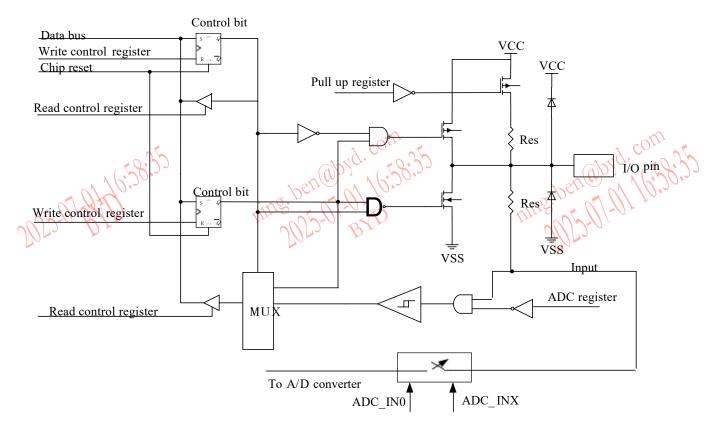
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## BF7515CM44-LJTX



Open-drain output structure



ADC IO structure

Mg Mg

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		DI / 313CN144-LJ1A					
O Poloted Dogi	at an	ben 0) pyd. 16	1.58.33 ping ben @ 19.58				
O Refated Regi	ster		ping of Mill				
	<u> </u>	SFR register	B				
Name	RW	Reset	Description				
DATAB	RW	1111_1111b	PB port data register				
DATAC	RW	1111_1111b	PC port data register				
DATAE	RW	1111_1111b	PE port data register				
DP_CON	RW	x000_0000b	LCD, LED control register				
DATAF	RW	1111_1111b	PF port data register				
DATAG	RW	xxxx_1111b	PG port data register				
DATAH	RW	1111_1111b	PH port data register				
TRISA	RW	xxxx_1111b	PA direction register				
TRISB	RW	1111_1111b	PB direction register				
TRISC	RW	1111_1111b	PC direction register				
TRISE	RW	1111_1111b	PE direction register				
TRISF	RW	1111_1111b	PF direction register				
TRISG	RW	xxxx_1111b	PG direction register				
TRISH	RW	1111_1111b	PH direction register				
DATAA	RW	xxxx_1111b	PA port data register				
	Name DATAB DATAC DATAE DP_CON DATAF DATAG DATAH TRISA TRISB TRISC TRISE TRISF TRISG TRISH	NameRWDATABRWDATACRWDATAERWDP_CONRWDATAFRWDATAGRWDATAHRWTRISARWTRISBRWTRISERWTRISFRWTRISGRWTRISHRW	Name         RW         Reset           DATAB         RW         1111_1111b           DATAC         RW         1111_1111b           DATAE         RW         1111_111b           DP_CON         RW         x000_0000b           DATAF         RW         1111_111b           DATAG         RW         xxxxx_1111b           DATAH         RW         1111_111b           TRISA         RW         xxxxx_1111b           TRISB         RW         1111_111b           TRISC         RW         1111_111b           TRISF         RW         1111_111b           TRISG         RW         xxxxx_1111b           TRISH         RW         1111_111b				

Port configuration SFR register list

	Secondary bus register							
Address	Name	RW	Reset	Description				
0x17	PU_PA	RW	xxxx_0000b	PA pull-up resistor control register				
0x18	PU_PB	RW	0000_0000Ь	PB pull-up resistor control register				
0x19	PU_PC	RW	0000_0000Ь	PC pull-up resistor control register				
0x1B	PU_PE	RW	0000_0000Ь	PE pull-up resistor control register				
0x1C	PU_PF	RW	0000_0000Ь	PF pull-up resistor control register				
0x1D	PU_PG	RW	xxxx_0000b	PG pull-up resistor control register				
0x1E	PU_PH	RW	0000_0000Ь	PH pull-up resistor control register				
0x23	COM_IO_SEL	RW	0000_0000Ь	COM selection configuration register				
0x25	ODRAIN_EN	RW	xxxx_0000b	PC4/5/PE4/5 port open drain output enable register				

Port configuration secondary bus register list

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## 6.2. GPIO Register Description

## 6.2.1. Port Data Register

DATAA (F8H) PA port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	PA3	PA2	PA1	PA0
R/W	_	_	_	_	R/W	R/W	R/W	R/W
Reset value	_	_	_	_	1	1	1	1

	Bit number	) Bit symbol	Description
	2097g.co		PA data register, you can configure the output level of the
5	ber 3~0	<del></del>	PA group IO port as GPIO port, the read value is the current level state of the IO port (input) or the configured output
		`	value (output)

DATAB (80H) PB port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
	0	PB data register, configurable PB group IO port as GPIO
7~0		port output level, the read value is the current level state of
(a)	26.33	IO port (input) or configured output value (output).

DATAC (90H) PC port data register.

Bit number	7	6	11002	40	3	2 👊		0
Symbol	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0		PC data register, configurable PC group IO port as GPIO port output level, the read value is the current level state of IO port (input) or configured output value (output).

DATAE (B0H) PE port data register

211112 (404)				\	♠ \ _			\
Bit number	8:57	6	5	by 4 5	8:23	2	1	210.0 Z
Symbol	PE7	PE6	PES	PE4	PE3	PE2	REI	PEO .
R/W	R/W	R/W 🚫	R/W	R/W	R/W	R/W 🚫	R/W	R/W
Reset value	1	1		1	1	1	177	1

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Bit number	Bit symbol	Description ning
Mrs Br		PE data register, configurable PE group IO port as GPIO
7~0		port output level, the read value is the current level state of
		IO port (input) or configured output value (output).

DATAF (C0H) PF port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

ann	om om
Bit number Bit symbol	Description
Dev (0) 1 /0.20.2	PF data register, you can configure the output level of the PF
2000	group IO port as a GPIO port, and the read value is the
	current level state of the IO port (input) or the configured
	output value (output)

DATAG (C8H) PG port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	PG3	PG2	PG1	PG0
R/W	_	_	-	_	R/W	R/W	R/W	R/W
Reset value	_	_	_	_	1	1	1	1

	Bit number	Bit symbol	Description
	320. 16.	26:35	PG data register, configurable PG group IO port as GPIO port output level, the read value is the current level state of
5	per 20 mg	•	IO port (input) or configured output value (output).

DATAH (D8H) PH port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0		PH data register, configurable PH group IO port as GPIO port output level, the read value is the current level state of IO port (input) or configured output value (output).



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## 6.2.2. Direction Register

(D)	))))icollade	toi			05	<b>BF</b> 7	515CM	44-LJTX	
6.2.2. Direct			7075	01.01.16	9.3		3052-	70116:5	,b
Bit number	7	6	5	4	3	2	1	0	
Symbol	_	_	_	_	_	_	_	_	
R/W	_	_	_	_	R/W	R/W	R/W	R/W	
Reset value	_	_	_	_	1	1	1	1	

Bit number	Bit symbol	Description	
		Bit[3]~Bit[1]: Direction of PA3~PA0 port pins	
3~0		0: PAx port is output;	om
abyd. Co.	0.35	1: PAx port is input	aprd. Co.

TRISB (EBH) PB direction register

	*	$\mathcal{C}$	lar.	~ /\ \ \ \	•		Lat. F	~ // ///
Bit number	7	6	ng.5	1-4	3	2	181.	0
Symbol	_	_	0000	a, BAD	_	_	0000	J. BID
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	<del></del>	Bit[7]~ Bit[1]: Direction of PB7~PB0 port pins 0: PBx port is output;
		1: PBx port is input

TRISC (ECH) PC direction register

Bit number	27	6	5	4. co,	3	2	1	$\sqrt{90}$
Symbol	9:33	-	. <b>-</b> an	00/2/6		ı		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1 5		1	1	1		1

Bit number	Bit symbol	Description
7~0		Bit[7]~ Bit[1]: Direction of PC7~PC0 port pins 0: PCx port is output; 1: PCx port is input

TRISE (EEH) PE direction register

Bit number	7	6	5	4	3	2	1	0
Symbol		_	_	_	_	_	_	_
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	28:5 <u>1</u>	1	1	1/1	8:27	1	1 (	1 .5

Bit number	Bit symbol	Description Description	
7~0		Bit[7]~ Bit[1]: Direction of PE7~PE0 port pins	) •

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0: PEx port is output; 1: PEx port is input

TRISF (EFH) PF direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	_	_
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description	
		Bit[7]~Bit[1]: Direction of PF7~PF0 port pins	
7~0	<u></u>	0: PFx port is output;	com
ahyd. ce	0.35	1: PFx port is input	aprid. co

TRISG (F2H) PG direction register

Bit number	7	6	1285	1-4	3	2	ng 1 - n	1.00
Symbol	ı	_	2000	BAD	ı	_	JU 2	J. BALL
R/W	ı	_	_	-	R/W	R/W	R/W	R/W
Reset value	_	_	_		1	1	1	1

Bit number	Bit symbol	Description
3~0	<del></del>	Bit[3]~ Bit[1]: Direction of PG3~PG0 port pins 0: PGx port is output;
		1: PGx port is input

TRISH (F7H) PH direction register

Bit number	24	6	5	4. cos	23	2	1	1 2/90COTE
Symbol	50.5	_	- an	00%	26.2	_	1- and	100 TV (20)
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1		1	1	1 5		1

Bit number	Bit symbol	Description
7~0		Bit[7]~ Bit[1]: Direction of PH7~PH0 port pins 0: PHx port is output; 1: PHx port is input

## 6.2.3. Pull-up Enable Register

## Secondary bus register:

PU PA (17H) PA pull-up resistor control register

			1101011070707			/ /	
Bit number	7	6	5 en (4 /6)	3	2	Henle	0/0/0:2
Symbol	-	_ <	ing I Want	_	-	mg.	1-02
R/W	_		0012	R/W	R/W	RW	R/W

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Recet value	he'	VA 10:30.	0 0	men 10/0.
incoct values _	- ~ ~	1 1-1 -	0   0	( V )
0.1311		0.1.41.2	•	0.171

Bit number	Bit symbol	Description
		PA pull-up resistor control register
3~0		1: The pull-up resistor is enabled;
		0: The pull-up resistor is not enabled

PU PB (18H) PB pull-up resistor control register

1 C 1 D (1011) 1	D pair ap	esistor eor	mor regist	C1					
Bit number	7	6	5	4	3	2	1	0	
Symbol		_							
R/W		R/W							
Reset value	0	000							
1 ()				1 ()				1 (0	

Bit number	Bit symbol	Description	pen(0) 1/13
	· · · · · · · · · · · · · · · · · · ·	PB pull-up resistor control register	ning. of Milling
7~0	<del></del>	1: The pull-up resistor is enabled;	1652-01
		0: The pull-up resistor is not enabled	

PU PC (19H) PC pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0		
Symbol		_								
R/W		R/W								
Reset value				(	)					

Bit number	Bit symbol	Description	art)
alayd. co,	0.35	PC pull-up resistor control register	2/2/J. COL
7~0	26.33 <u>-</u>	1: The pull-up resistor is enabled;	
E De L'OFT		0. The pull-up resistor is not enabled	: 2. pc. 1 1 10.

PU PE (1BH) PE pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0		
Symbol		_								
R/W		R/W								
Reset value				(	0					

Bit number	Bit symbol	Description	
		PE pull-up resistor control register	
7~0		1: The pull-up resistor is enabled;	$\sim$
7 001		0: The pull-up resistor is not enabled	COLL

PU PE (ICH) PF pull-up resistor control register

	TIP GIT OF TO	DIDUCT COL	101011051001		
Bit number	7	6	3	2	0/0/0
Symbol		77	1118	D)	
R/W			R/W		

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Reset value

Bit number	Bit symbol	Description
		PF pull-up resistor control register
7~0		1: The pull-up resistor is enabled;
		0: The pull-up resistor is not enabled

PU PG (1DH) PG pull-up resistor control register

10 10 (1D11)	Te Te (1911) Te pair up resistor control register							
Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	1	_	-	_	_	_
R/W	_	_	-	_	R/W	R/W	R/W	R/W
Reset value	D _	_	ı	- 601	0 (	0	0	0.00

	Bit number	Bit symbol	Description	ben as I lis
5	: " W.M.	K	PG pull-up resistor control register	ning.
	3~0	<u></u>	1: The pull-up resistor is enabled;	1652-01
			0: The pull-up resistor is not enabled	

PU PH (1EH) PH pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0		
Symbol		_								
R/W		R/W								
Reset value				(	)					

	Bit number	Bit symbol	Description	m
	21-x1d. co,		PH pull-up resistor control register	21-x1d. CO1
	0		1: The pull-up resistor is enabled;	1.000
Z	DC,		0. The pull-up resistor is not enabled	ing be

## 6.2.4. Large Current Sink

DP\_CON (R1H) LCD\_LED\_control register

DI_CON (DIII)		, LLD COII	10110	513101				
Bit number	7	6	5	4	3	2	1	0
Symbol	_	IO_ON	DU	DUTY SEL		DPSEL	SCAN_MODE	COM_MOD
R/W	_	R/W		R/W		R/W	R/W	R/W
Reset value	_	0	0	0	0	0	0	0

Bit number	Bit symbol	Description COM
5025-0.09/J	COM_MOD	High-current IO port driver enable  1: COM port function is locked and works as a high-current IO port;  0: COM port function is not locked and can be configured as

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other functions;
When COM port function is locked to high-current IO port,
by configuring GPIO register output drive timing, LED/LCD
scan configuration is invalid

COM IO SEL (23H) COML select configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	COML7	COML6	COML5	COML4	COML3	COML2	COML1	COML0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

	Bit number	Bit symbol	Description Off
	abyd. c	20.35	In LED matrix drive mode, 4*4 mode is not selected:
	Per (0) 2, 11.	2:20.2	COM port select configuration register, the corresponding bit is 1,
18	1/1/1/		COMLx is common
0	1520,		1: Select the COM port function.
	N		0: Select the I/O port mode
	7.0		In LED matrix drive mode, select 4*4 mode:
	7~0		COML0~ COML3 is common, and COML4~ COML7 is segment
			1: Select COM port function or SEG port function;
			0: Select the I/O port mode
			When the high current IO port drive is enabled:
			1: Select the high-current I/O port
			0: Select the I/O port mode

## 6.2.5. Open Drain Enable Register

## Secondary bus register:

DRAIN EN (25H) PC4/5/PE4/5 port open drain output enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	_	_
R/W	_	_	_	_	R/W	R/W	R/W	R/W
Reset value	_	_	_	_	0	0	0	0

Bit number	Bit symbol	Description
		PE5 port open drain output enable register
3		1: Open-drain output; 0: CMOS output
		PE4 port open drain output enable register
2		1: Open-drain output; 0: CMOS output
PC5 port open drain output enable register		PC5 port open drain output enable register
1		1: Open-drain output; 0: CMOS output

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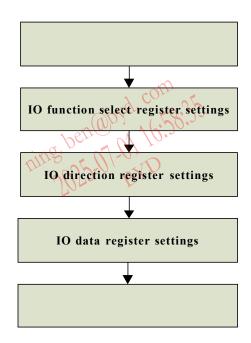


PC4 port open drain output enable register

1: Open-drain output; 0: CMOS output

## 6.3. GPIO Configuration Process

When setting the port as GPIO, the following three sets of registers need to be set accordingly.



IO configuration flow chart

#### Note:

The default source current drive capability of the IO port is typically 16mA, and the sink current drive capability is typically 68mA @5V 0.9VCC. When using IO to drive the LED/digital tube, you need to pay attention to the Ifp current of the LED lamp. It is recommended to add a current-limiting resistor to limit the IO drive peak current within the LED/digital tube Ifp current.

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## 7. Interrupt

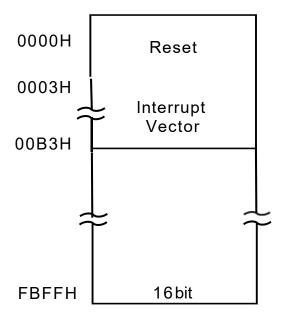
## 7.1. Interrupt Sources and Entry Address

Interrupt source	Condition	Sign	Enable control	Priority control	Interrupt vector	Query priority	Interrupt number	Flag removal method	wakeup idle mode 1
INT0	condition is met	IE0	IEN0[0]	IPL0[0]	0x0003	1	0		Yes
Timer0	Timer0 overflow	TF0	IEN0[1]	IPL0[1]	0x000B	2	1		No
INT1	condition is met	IE1	IEN0[2]	IPL0[2]	0x0013	3	2		Yes
Timer1	Timer1 overflow	TF1	IEN0[3]	IPL0[3]	0x001B	4	3		No
INT2	condition is met	IE2	IEN1[2]	IPL1[2]	0x004B	5	9		Yes
IIC	Receive or send completed	IE3	IEN1[3]	IPL1[3]	0x0053	6	10		Yes
ADC	ADC conversion completed	IE4	IEN1[4]	IPL1[4]	0x005B	7	11		No
LED/ LCD	Scan complete	IE6	IEN1[6]	IPL1[6]	0x006B	9	13		No
WDT/ Timer2 /PWM0	WDT/Timer2/ PWM0 overflow	IE7	IEN1[7]	IPL1[7]	0x0073	10	14		WDT/ Timer2 yes, PWM0 no
UART2	Receive or send completed	IE8	IEN2[0]	IPL2[0]	0x007B	11	15		No
LVDT	Voltage Conditions meet	IE9	IEN2[1]	IPL2[1]	0x0083	12	16		No
UART0	Receive or send completed	IE10	IEN2[2]	IPL2[2]	0x008B	13	17		No
UART1	Receive or send completed	IE11	IEN2[3]	IPL2[3]	0x0093	14	18		No
Timer3/PW M1	Timer3/PWM1 overflow	IE12	IEN2[4]	IPL2[4]	0x009B	15	19		No
SPI	Receive or send completed	IE13	IEN2[5]	IPL2[5]	0x00A3	16	20		No
INT3	condition is met	IE14	IEN2[6]	IPL2[6]	0x00AB	17	21		Yes
INT4	condition is met	IE15	IEN2[7]	IPL2[7]	0x00B3	18	22		Yes

List of interrupt information

NOTE: ' ,: User must clear.

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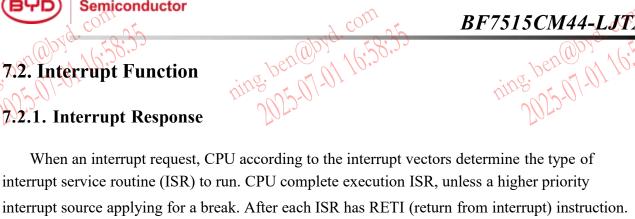
When the chip generates a reset signal, the program starts from the 0x0000 address. When an interrupt signal occurs, the program will jump to the interrupt vector program address to execute the interrupt service routine.

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## 7.2. Interrupt Function

## 7.2.1. Interrupt Response



ISR can only be a higher priority interrupt request interrupt. That is, the low-priority ISR can be interrupted by a high-priority interrupt request.

After RETI instruction, CPU continues to execute the program before the interrupt did not happen.

The BF7515CM44-LJTX response interrupt request until the current instruction finished. If the RETI instruction is being executed or read IP, IEN register, after an additional instruction then respond the interrupt request.

#### 7.2.2. Interrupt Priority

The BF7515CM44-LJTX have two interrupt priority levels: interrupt level and the default priority. Interrupt level (top, high and low) override the default priority. The priority set to high is the first to respond. When the priority is set to the same level, the response will be queued by default. Power-down interrupt is the only high-level interrupt source if allowed. All interrupt sources can be set to high priority or low priority.

Each interrupt source can be assigned a priority level (high or low), and the default priority. The same level of interrupt sources (such as both high priority) the priority is the default priority decision. Interrupt service routine in progress can only be a high-priority interrupt request interrupt.

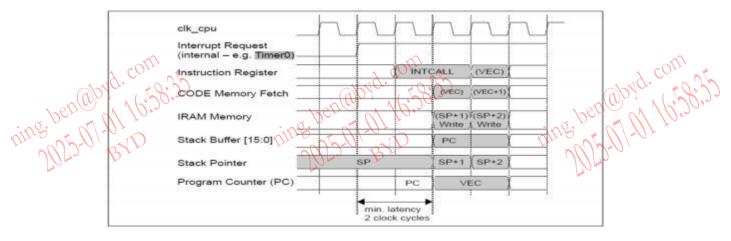
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## 7.2.3. Interrupt Sampling

Internal modules such as internal timers and serial ports generate interrupt requests through interrupt flag bits in their respective SFR. When the first clock cycle (C1) of each instruction cycle ends, the External Interrupt is sampled on the rising edge of the clock.

In order to ensure that the edge-triggered interrupt is detected, the corresponding port must first maintain the high level of 2 clocks, and then keep the low level of 2 clocks. The following figure shows the timing diagram of interrupt sampling:



#### 7.2.4. Interrupt Wait

Interrupt response time is determined by current state. Fastest response time is five instruction cycles: one cycle to detect the interrupt request, the other 4 used to execute long call (LCALL) to ISR.

When the system is executing a RETI instruction and is followed by a MUL or DIV instruction, the interrupt waits for the longest time (13 instruction cycles). This 13 instruction cycles are as follows: one cycle to detect the interrupt request, three to complete the RETI, five used to execute DIV or MUL instruction, 4 used to execute long call (LCALL) to ISR. In this case, the response time is 13 clock cycles.

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# 7.3. Interrupt Related Register

10130 B31			SFR register	1013 Bit
Address	Name	RW	Reset	Description
0x88	TCON	RW	0000_0x0xb	Timer control register
0xA8	IEN0	RW	0xxx_0000b	Interrupt enable register
0xAE	INT_PE_STAT	RW	0000_0000ь	Interrupt status register
0xB8	IPL0	RW	xxxx_0000b	Interrupt priority register 0
0xC7	EXINT_STAT	RW	0000_0000ь	External interrupt status register
0xD5	INT_POBO_STAT	RW	xxxx_xx00b	LVDT boost/buck interrupt status register
0xE1	IRCON2	RW	0000_0000ь	Interrupt flag register 2
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xE7	IEN2	RW	0000_0000ь	Interrupt enable register 2
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 2
0xF4	IPL2	RW	0000_0000ь	Interrupt priority register 2
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xFA	PWM_INT_CTRL	RW	xxxx_xx00b	PWM interrupt enable control register

List of interrupt SFR registers

## 7.3.1. Interrupt enable register

IEN0 (A8H) Interrupt enable register

Bit number	7	6	5	14c0 <sup>ff</sup>	3	2	1	7 60W
Symbol	EA	_	(1	pio.	ET1	EX1	ETO	EX0
PEN R/W	R/W	_	pend	1/1/10.	R/W	R/W	R/W	R/W
Reset value	0	_ %	11.8.		0	0 0	05	0

Bit number	Bit symbol	Description				
		Interrupt enable bit.				
	ΕA	0: Mask all interrupts (EA has priority over the respective interrupt enable bits ofthe interrupt sources);				
7	EA	1: The interrupt is turned on. Whether the interrupt request of each interrupt source is allowed or forbidden is				
		determined by the respective enable bit.				
6~4		Reserved				
		Timer 1 overflow interrupt enable bit				
3	ET1	0: Disable timer 1 (TF1) to apply for interrupt;				
(Transition)		1: Allow TF1 flag bit to request interrupt.				

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	$(0)_{i,j}$	70.3	
pener 1/10.3		.5	INT_EXT1 enable bit.
	05-02	EX1	0: Disable INT_EXT1 to apply for interrupt;
7			1: Allow INT_EXT1 to apply for interrupt.
			Timer 0 overflow interrupt enable bit
	1	ET0	0: Disable timer 0 (TF0) to apply for interrupt;
			1: Allow TF0 flag bit to request interrupt.
	0 EX0		INT_EXT0 enable bit
			0: Disable INT_EXT0 to apply for interrupt;
			1: Allow INT_EXT0 to apply for interrupt.

IEN1 (E6H) Interrupt enable register 1

	Bit number	7	6	5	4	3	2	1	0
	Symbol.	EX7	EX6	_	EX4	EX3	EX2	_	7-19 <del>-</del> COL
	RW	R/W	R/W	4- 37	R/W	R/W	R/W	4-01	100%
Į	Reset value	0	0	12:- C	7.00	0	0	12 C	1 11 10.
	105-0 BYD		7	Clock	J'BYD		ζ,	111	JIBAD

11117 12 12		
Bit number	Bit symbol	Description
		WDT/Timer2/PWM0 interrupt enable
7	EX7	1: WDT/Timer2/PWM0 interrupt enable;
		0: WDT/Timer2/PWM0 interrupt disable
		LED/LCD interrupt enable
6	EX6	1: LED/LCD enable;
		0: LED/LCD disable
		ADC interrupt enable
4	EX4	1: ADC interrupt enable;
		0: ADC interrupt disable
		IIC interrupt enable
3	EX3	1: IIC interrupt enable;
Pir		0: IIC interrupt disable
		External Interrupt2 interrupt enable
2	EX2	1: External Interrupt2 interrupt enable;
		0: External Interrupt2 interrupt disable
5, 1~0	_	Reserved

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	EX15	EX14	EX13	EX12	EX11	EX10	EX9	EX8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	20 00	0.0	0	0	70com

	10		~ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Bit number	Bit symbol	Description	perio 110.
1022-02BID	EX15	External Interrupt4 interrupt enable 1: External Interrupt4 interrupt enable	", 502-0/-0

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0: External Interrupt4 interrupt disable External Interrupt3 interrupt enable EX14 1: External Interrupt3 enable; 0: External Interrupt3 disable SPI interrupt enable 5 **EX13** 1: SPI interrupt enable; 0: SPI interrupt disable Timer3 interrupt enable **EX12** 1: Timer3 interrupt enable; 4 0: Timer3 interrupt disable UART1 interrupt enable EX11 1: UART1 interrupt enable; 3 0: UART1 interrupt disable **UART0** interrupt EX10 1: UART0 enable; 2 0: UART0 disable LVDT interrupt enable EX9 1: LVDT interrupt enable; 1 0: LVDT interrupt disable UART2 interrupt enable EX8 1: UART2 interrupt enable; 0 0: UART2 interrupt disable

PWM INT CTRL (FAH) PWM interrupt enable control register

Bit number 7	6	5	4 600 3	2	1	0.00
Symbol	_	-	19/9. (8:3)	_	- (	byd.
pen R/W 1000 _	_	ben	0,7/0,20.	_	R/W	R/W)
Reset value _	- (	mg.		- 5	mgo -	0

Bit number	Bit symbol	Description					
		PWM1 counter overflow interrupt					
1		1: Interrupt enable; 0: Interrupt disable					
		PWM0 counter overflow interrupt					
0		1: Interrupt enable; 0: Interrupt disabled					

## 7.3.2. Interrupt Priority Register

IPL0 (B8H) Interrupt priority register0

	- L 1	, ,		~ ' b ' \		
Bit number	5.7	6	5 0 4	3	2	1 0 0 0
Symbol	_	_	varper of Will	PT1	PX2	PTO PX0
R/W	_	_ ′	111005-01-0	R/W	R/W <sup>5</sup>	R/W R/W
			, Mar			

4 com

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Reset value \_ \_ \_ \_ \_ 0 0 0

Bit number	Bit symbol	Description
7~4	ı	Reserved
		TF1 (Timer1 interrupt) priority selection bit.
3	PT1	0: Timer1 interrupt is low priority;
		1: Timer1 interrupt is high priority
		INT_EXT1 interrupt priority selection bit.
2	PX2	0: External Interrupt1 is low priority;
		1: External Interrupt1 is high priority
		TF0 (Timer0 interrupt) priority selection bit.
1	PT0	0: Timer0 interrupt is low priority;
		1: Timer0 interrupt is high priority
		INT_EXT0 interrupt priority selection bit.
0	PX0	0: External Interrupt0 is low priority;
		1: External Interrupt0 is high priority

IPL2 (F4H) Interrupt priority register2

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL2.7	IPL2.6	IPL2.5	IPL2.4	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description		
		External Interrupt4 priority selection bit.		
7	IPL2.7	1: External Interrupt4 interrupt is high priority;		
		0: External Interrupt4 interrupt is low priority		
		External Interrupt3 priority selection bit.		
6	IPL2.6	1: External Interrupt3 interrupt is high priority;		
		0: External Interrupt3 interrupt is low priority		
		SPI priority selection bit.		
5	IPL2.5	1: SPI interrupt is high priority;		
		0: SPI interrupt is low priority		
		Timer3 priority selection bit.		
4	IPL2.4	1: Timer3 interrupt is high priority;		
		0: Timer3 interrupt is low priority		
		UART1 priority selection bit.		
3	IPL2.3	1: UART1 interrupt is high priority;		
	-	0: UART1 interrupt is low priority		
	101.0.0	UART0 priority selection bit.		
2	IPL2.2	1: UART0 interrupt is high priority;		

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	70.0					
pena Wip	,50	0: UART0 interrupt is low priority				
05-01-0		LVDT priority selection bit.				
1	IPL2.1	1: LVDT interrupt is high priority;				
		0: LVDT interrupt is low priority				
		UART2 priority selection bit.				
0	IPL2.0	1: UART2 interrupt is high priority;				
		0: UART2 interrupt is low priority				

IPL1 (F6H) Interrupt priority register1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	_	IPL1.4	IPL1.3	IPL1.2	_	_
R/W	R/W	R/W	_	R/W	R/W	R/W	_	-com
Reset value	0.00	0	- (	10/0.	0.0	0	- (6	programme

	76710 V 100		Perro V 10.2						
Ę	Bit number	Bit symbol	Description ing						
(	Ors. BAD	<b>)</b>	WDT/Timer 2/PWM0 interrupt priority bit						
	7	IPL1.7	1: WDT/Timer 2/PWM0 interrupt is high priority;						
			0: WDT/Timer 2/PWM0 interrupt is low priority						
			LED/LCD interrupt priority bit						
	6	IPL1.6	1: LED/LCD interrupt is high priority;						
			0: LED/LCD interrupt is low priority						
			ADC interrupt priority bit						
	4	IPL1.4	1: ADC interrupt is high priority;						
			0: ADC interrupt is low priority						
			IIC interrupt priority bit						
	3	IPL1.3	1: IIC interrupt is high priority;						
	$\Omega_{\rm b}$		0: IIC interrupt is low priority						
	Bin		External Interrupt2 interrupt priority bit						
	2	IPL1.2	1: External Interrupt2 is high priority;						
			0: External Interrupt2 is low priority						
	5, 1~0		Reserved						

## 7.3.3. Interrupt Flag Register

TCON (88H) Timer control register

	Bit number	7	6	5	4	3	2	1	0
	Symbol	TF1	TR1	TF0	TR0	IE1	_	IE0	· FOM
	R/W	R/W	R/W	R/W	R/W	R/W	_	R/W	oyd 129
	Reset value	20.0	0	10enly	0/0/0:	0	_	1 Prilling	7/2:21
ζ.	NIII N			7 7	1111			7 V	

Bit number Bit symbol Description

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Timer 1 overflow flag TF1 The hardware is set to 1 when Timer1 overflows, or TH0 of Timer0 overflows in mode 3. Timer1 start enable TR1 6 Set to 1, start Timer1 or start Time0 mode, TH0 count at three o'clock Timer 0 overflow flag TF0 5 Set by hardware when Timer0 overflows Timer0 start enable TR0 4 Start Timer0 counting when set to 1 External Interrupt1 flag IE1 3 Set by hardware, clear by software External Interrupt0 flag IE0 1 Set by hardware, clear by software 0, 2 Reserved

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	IE15	IE14	IE13	IE12	IE11	IE10	IE9	IE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
		External Interrupt4 interrupt flag
7	IE15	1: With External Interrupt4 interrupt flag
		0: Clear External Interrupt4 interrupt flag
		External Interrupt3 interrupt flag
6	IE14	1: With External Interrupt3 interrupt flag
		0: Clear External Interrupt3 interrupt flag
		SPI interrupt flag
5	IE13	1: With SPI interrupt flag
		0: Clear SPI interrupt flag
		Timer3/PWM1 interrupt flag
4	IE12	1: With Timer3/PWM1 interrupt flag
		0: Clear Timer3/PWM1 interrupt flag
		UART1 interrupt flag
3	IE11	1: UART1 interrupt flag is present
		0: Clear UART1 interrupt flag
		UART0 interrupt flag
2	IE10	1: There is UART0 interrupt flag
		0: Clear UART0 interrupt flag

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(0)	(,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	
benes My	10.30	LVDT interrupt flag
25-01	IE9	1: With LVDT interrupt flag
J772		0: Clear LVDT interrupt flag
		UART2 interrupt flag
0	IE8	1: UART2 interrupt flag
		0: Clear LVDT interrupt flag

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	_	IE4	IE3	IE2	_	_
R/W	R/W	R/W	_	R/W	R/W	R/W	_	_
Reset value	0	0	_	0 ~	0	0	_	-00
-1-1/2.00	10.35			-1-1/0.00	0.25			1-110.

apro.	0.73	phío. 50.1)						
Bit number	Bit symbol	Description Description						
8 . 47/11,		WDT/Timer2/PWM0 interrupt flag						
7	IE7	1: With WDT/Timer2/PWM0 interrupt flag;						
		0: Clear WDT/Timer2/PWM0 interrupt flag						
		LED/LCD interrupt flag						
6	IE6	1: With LED interrupt flag						
		0: Clear LED interrupt flag						
		ADC interrupt flag						
4	IE4	1: With ADC interrupt flag;						
		0: Clear ADC interrupt flag						
		IIC interrupt flag						
3	IE3	1: With IIC interrupt flag;						
		0: Clear IIC interrupt flag						
		External Interrupt2 interrupt flag						
201	IE2	1: With External Interrupt2 interrupt flag;						
Dr		0: Clear External Interrupt2 interrupt flag						
5, 1~0	_	Reserved						

## 7.3.4. Interrupt Status Register

INT PE STAT (AEH) Interrupt status register

		0		
Bit number	7	6	5	4
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	07 COM	0	0 y com
Bit number	3	(0)2	1	000
Symbol	INT_TIMER2_STAT.	INT_PWM0_STAT	INT_LCD_STAT	INT_LED_STAT
R/W	R/W	R/W	R/W	R/W
, Mrs.				

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Reset value 0 ben 0

10/2/V	711	10h-01 x10
Bit number	Bit symbol	Description
7	INT_PWM1_STAT	PWM1 interrupt status flag, this bit is cleared by writing 0, and it can also be cleared by closing the PWM1 channel 1: Interrupt is valid; 0: Interrupt is invalid
6	INT_TIMER3_STAT	TIMER3 interrupt status flag, this bit is cleared by writing 0, and can also be cleared by writing TIMER3_CFG, 1: Interrupt is valid; 0: Interrupt is invalid
5	INT08_STAT	INT08 port interrupt status, this bit is cleared by writing 0, and it can also be cleared by writing INT08_IO_SEL=0, 1: Interrupt is valid; 0: Interrupt is invalid
4	INT_WDT_STAT	WDT interrupt status flag, this bit is cleared by writing 0, and can also be cleared by writing WDT_CTRL, 1: Interrupt is valid; 0: Interrupt is invalid
3	INT_TIMER2_STAT	TIMER2 interrupt status flag, this bit is cleared by writing 0, and can also be cleared by writing TIMER2_CFG, 1: Interrupt is valid; 0: Interrupt is invalid
2	INT_PWM0_STAT	PWM0 interrupt status flag, this bit is cleared by writing 0, and it can also be cleared by closing the PWM0 channel.  1: Interrupt is valid; 0: Interrupt is invalid
1	INT_LCD_STAT	LCD interrupt status mark, write 0 to clear this bit, write SCAN_START operation can also be cleared, 1: Interrupt is valid; 0: Interrupt is invalid
0	INT_LED_STAT	LED interrupt status mark, this bit is cleared by writing 0, and it can also be cleared by writing SCAN_START, 1: Interrupt is valid; 0: Interrupt is invalid

EXINT\_STAT (C7H) External interrupt status register

Bit number	7	6	5	4
Symbol	INT07_STAT	INT06_STAT	INT05_STAT	INT04_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0 000
Symbol	INT03_STAT	INT02_STAT	INT01_STAT	INTOO_STAT
PR/W	R/W	R/W \	R/W	NETRYW \ \\
Reset value	0	ing of 01-11	0	ing. 2 10 -11

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Bit number	Bit symbol	Description bentally
7~0	INT0x_STAT (x=7~0)	INT0x port interrupt status, this bit is cleared by writing 0, and it can also be cleared by writing INT0x_IO_SEL=0 1: interrupt is valid; 0: interrupt is invalid

INT\_POBO\_STAT(D5H) LVDT boost/buck interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	INT_PO_STAT	INT_BO_STAT
R/W	_	_	_	_	_	_	R/W	R/W
Reset value	_	_	_	_	_	_	0	0

	Bit number	) Bit symbol	Description
	Per 0 1/9.	INT_PO_STAT	LVDT boost interrupt status  1: Boost interrupt is valid; 0: Boost interrupt is invalid
ر م	05-0	INT_BO_STAT	LVDT boost interrupt status  1: Boost interrupt is valid; 0: Boost interrupt is invalid

## 7.4. Secondary Bus Register

	Secondary bus register						
Address	Name	RW	Reset	Description			
0x34	PERIPH_IO_SEL1	RW	0001_0000b	External port function selection register 1			
0x35	PERIPH_IO_SEL2	RW	0000_0000ь	External port function selection register 2			
0x36	PERIPH_IO_SEL3	RW	1xxx_xxxxb	External port function selection register 3			
0x37	PERIPH_IO_SEL4	RW	0xxx_x000b	External port function selection register 4			
0x38	PERIPH_IO_SEL5	RW	0000_0000ь	External port function selection register 5			
0x39	EXT_INT_CON1	RW	0101_0101b	External Interrupt configuration register 1			
0x3A	EXT INT CON2	RW	xxxx x001b	External Interrupt configuration register 2			

List of interrupt secondary bus registers

## 7.4.1. External Port Function Selection Register

PERIPH IO SEL1 (34H) External port function selection register 1

Bit number	7	6	5	4
Symbol	UART1_IO_SEL	UARTO SEL		IIC_IO_SEL
R/W	R/W	R/W.d.	R/W.d.	
Reset value	0	100000000000000000000000000000000000000	0	16:5
Bit number	3	108. 27	1	108. 10 11
Symbol	INT3_IO_SEL	INT2_IO_SEL	INT1_IO_SEL	INTO_8_IO_SEL

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(0)	70.5			
P/W/	R/W	R/W	R/W	R/W
Reset value	0	0	0	02-6/-01

Bit number	Bit symbol	Description
2	INT3 IO SEL	INT3 port selection enable
3	INTS_IO_SEL	1: INT3 function is selected; 0: INT3 function is not selected
	DITO IO CEI	INT2 port selection enable
2	2 INT2_IO_SEL	1: INT2 function is selected; 0: INT2 function is not selected
_	DIT1 IO CEI	INT1 port selection enable
1	INT1_IO_SEL	1: select INT1 function; 0: not select INT1 function
		INTO_8 port selection enable
		1: INT function is selected; 0: INT function is not selected

PERIPH IO SEL2 (35H) External port function selection register 2

	thurst he br	2D2 (3311) DAtolliul	ore randeron selection	11 10515101 2	Sister 2		
5	Bit number	7	ing. 61-11	5	m8 4 -11		
0	Symbol	INTO_7_IO_SEL	INTO 6 IO SEL	INTO_5_IO_SEL	INTO_4_IO_SEL		
	R/W	R/W	R/W	R/W	R/W		
	Reset value	0	0	0	0		
	Bit number	3	2	1	0		
	Symbol	INTO_3_IO_SEL	INTO_2_IO_SEL	INTO_1_IO_SEL	INTO_0_IO_SEL		
	R/W	R/W	R/W	R/W	R/W		
	Reset value	0	0	0	0		

Bit number	Bit symbol	Description
abyd. Co	INT0_x_IO_SEL	INT0_x port selection enable
pen 120 16	(x=7~0)	1: INT function is selected; 0: INT function is not selected

PERIPH IO SEL3 (36H) External port function selection register 3

Bit number	7	6	5 B	4	3	2	0037	BO
Symbol	INT4_7_IO_SEL	_	_	_	_	_		_
R/W	R/W	_	_	_	_	_	_	-
Reset value	0	_	_	_	_	_	_	-

Bit number	Bit symbol	Description
7	INT4_7_IO_SEL	INT4_7 port selection enable 1: INT function is selected; 0: INT function is not selected
6~0		Reserved

PERIPH IO SEL4 (37H) External port function selection register 4

Bit number	7	6~3	216.56.3	1	000
Symbol	INT4_15_IO_SEL	125.	INT4_10_IO_SEL	INT4_9_IO_SEL	INT4_8_IO_SEL
R/W	R/W	Jun o	R/W	R/W	R/W

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Reset value 0	- pen 10.3	0	ben on

Bit number	Bit symbol	Description
7.2.0	INT4_x_IO_SEL	INT4_x port selection enable
7, 2~0	$(x=15, 10 \sim 8)$	1: INT function is selected; 0: INT function is not selected
6~3		Reserved

PERIPH IO SEL5 (38H) External port function selection register 5

Bit number	7	6	5	4
Symbol	_	INT4_22_IO_SEL	INT4_21_IO_SEL	INT4_20_IO_SEL
R/W	_	R/W	R/W	R/W
Reset value	<u> </u>	0	0	0 000
Bit number	3	21110.00	2.35 1	6/10. Co
Symbol \	INT4_19_IO_SEL	INT4_18_IO_SEL	INT4_17_IO_SEL	INT4_16_IO_SEL
R/W	R/W	INS RW	R/W	ng R/W
Reset value	0	00550	0	0 20

Bit number	Bit symbol	Description				
7		Reserved				
6.0	INT4_x_IO_SEL	INT4_x port selection enable				
6~0	$(x=22\sim16)$	1: INT function is selected; 0: INT function is not selected				

## 7.4.2. External Interrupt configuration register

EXT INT CON1 (39H) External Interrupt configuration register 1

	Bit number	8.7	6	5	1) 4 (	8.3	2	1 00	by a life
J_	Symbol	INT3_POI	LARITY	INT2_PO	LARITY	INT1_PC	LARITY	INT08_P	OLARITY
7	R/W	R/W	R/W	R/W	R/W	R/W	R/W S	R/W	R/W
( '	Reset value	0	1	0	1	0	1	0	1

Bit number	Bit symbol	Description
		External Interrupt3 trigger polarity selection:
7.6	INT2 DOLADITY	01: Falling edge (low-level wake-up in Sleep mode)
7~6	INT3_POLARITY	10: Rising edge (high level wake-up in Sleep mode)
		00/11: Double edge (low-level wake-up in Sleep mode)
		External Interrupt2 trigger polarity selection:
	INT2_POLARITY	01: Falling edge (low-level wake-up in Sleep mode)
5~4		10: Rising edge (high level wake-up in Sleep mode)
		00/11: Double edge (low-level wake-up in Sleep mode)
Va.	INT1_POLARITY	External Interrupt1 trigger polarity selection:
3~2		01: Falling edge (low-level wake-up in Sleep mode)

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$(0)_{j,j}$	.50.3			
bence of	2.3	10: Rising edge (high level wake-up in Sleep mode)		
305.01-0		00/11: Double edge (low-level wake-up in Sleep mode)		
J77 2		External Interrupt0_8 trigger polarity selection:		
1.0	INT08_POLARITY	01: Falling edge (low-level wake-up in Sleep mode)		
1~0		10: Rising edge (high level wake-up in Sleep mode)		
		00/11: Double edge (low-level wake-up in Sleep mode)		

EXT INT CON2 (3AH) External Interrupt configuration register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	1	INT4_POLARITY	INTO_PO	DLARITY
R/W	_	_	_	_	_	R/W	R/W	R/W
Reset value	02 -	_	_	_	00	0	0	1000
abyd. co	c6.95		obyd. 50.35				obyd. co	

				1.1
	Bit number	Bit symbol	Description Description	
5	1701,	nin.	External Interrupt4_x trigger polarity selection:	
<u></u>	2	INT4_POLARITY	1: Rising edge (high level wake-up in Sleep mode)	
	70		0: Falling edge (low-level wake-up in Sleep mode)	
			External Interrupt0_0~0_7 trigger polarity selection:	
	1.0	INITO DOL ADITY	01: Falling edge (low-level wake-up in Sleep mode)	
	1~0	INT0_POLARITY	10: Rising edge (high level wake-up in Sleep mode)	
			00/11: Double edge (low-level wake-up in Sleep mode)	

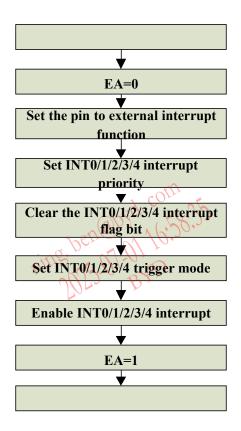
#### Note:

INT4X shares an interrupt vector, and can only respond to one External Interrupt at the same time. When the rising or falling edge of the multi-channel pin External Interrupt is triggered, the external Interrupt pins must be released during the detection process to respond to the current trigger. Signal (when the falling edge is triggered, the release is high, when the rising edge is triggered, the release is low).

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## 7.5. External Interrupt Configuration Process



INT configuration flow chart

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8. Timer

The BF7515CM44-LJTX series contains 2 timers (Timer0, Timer1) and 2 external Timers (Timer2, 3) inside the core. Each Timer contains a 16-bit register. When accessed, it appears in the form of two bytes: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). The registers of Timer2 are the low byte TIMER2 SET L and the high byte TIMER2 SET H. The registers of Timer3 are the low byte TIMER3 SET L and the high byte TIMER3 SET H.

#### The features of Timer are as follows:

- 16-bit Timer0/1/3, 32-bit Timer2;
- Timer0 clock source: fsys, the internal frequency of the timer clock is fsys 1/12;
- Timer1 clock source: fsys, the internal frequency of the timer clock is fsys 1/12;
- Timer2 clock source: LIRC 32kHz or XTAL 32768Hz/4MHz;
- Timer3 is connected to PLL 24MHz, the internal part of the clock is System clock 1/12 or 1/4;
- Timer0 supports 8bits automatic reload timing, 16bits manual reload timing function;
- Timer1 supports 8bits automatic reload timing, 16bits manual reload timing function;
- Timer2 supports 32bits automatic reload timing and manual reload timing, and supports interrupt wake-up function;
- Timer3 supports 16bits automatic reload timing, manual reload timing function.

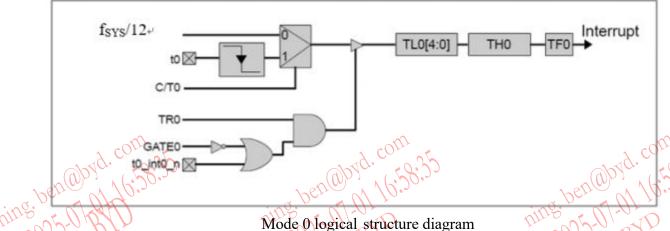
#### 8.1. Timer0 and Timer1

Timer 0/1 has four operating modes, which are controlled by TMOD SFR and TCON SFR. 2025-07-01-10-58:35

The four modes of Timer 0/1 are as follows:

- Mode 0: 13-bit timer
- Mode 1: 16-bit timer
- Mode 2: 8-bit timer with automatic reloading of initial value
- Mode 3: Two 8-bit timers

#### Mode 0: 13-bit timer



Mode 0 logical structure diagram

As shown in the figure, the working process of timer 0 and timer 1 is the same. In mode 0,

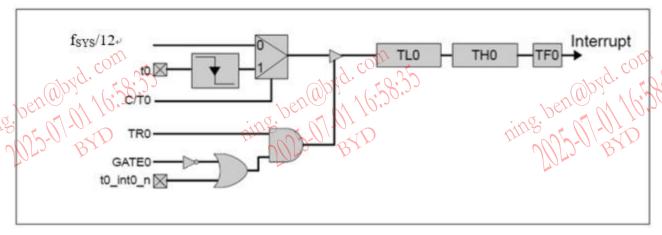
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Timer 0 is a 13-bit counter, and the 13-bit register consists of 8 bits of TH0 and the lower 5 bits of TL0. Timer 1 is a 13-bit counter, and the 13-bit register consists of 8 bits of TH1 and the lower 5 bits of TL1. The upper three bits of TL0 and TL1 should be ignored. The enable bit (TR0/TR1) in the TCON register controls the on and off of the timer.

The timer counts the selected System clock source (fsys/12). When the 13-bit counter counts up to all 1, the counter is cleared to 0 (all 0), and TF0 (or TF1) is set. t0/t1, C/T0 and C/T1 are all 0, t0\_int0\_n/t1\_int1\_n are all 1, and counting enable is only determined by TR0/1.

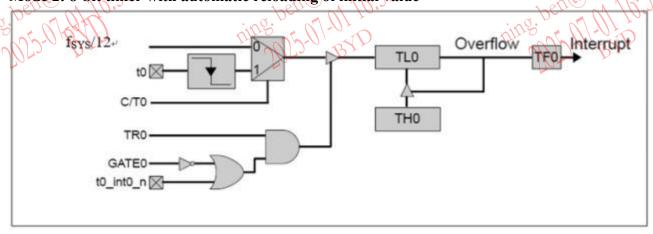
Mode 1: 16-bit timer



Mode 1 logical structure diagram

As shown in the figure, Mode 1 of Timer 0 and Timer 1 are the same. In Mode 1, Timer 0 and Timer 1 are 16-bit counters. The 16-bit register consists of 8 bits TH0 and 8 bits TL0. When the counter counts up to 0xFFFF, the counter is cleared to all 0s. Otherwise, mode 1 and mode 0 are the same. t0/t1, C/T0, C/T1 are all 0, t0\_int0\_n/t1\_int1\_n are all 1, and counting enable is only determined by TR0/1.

Mode 2: 8-bit timer with automatic reloading of initial value



Mode 2 logical structure diagram

Mode 2 of Timer 0 and Timer 1 are the same. In mode 2, the timer is an 8-bit counter with an automatic reload initial value. This counter is the LSB register (TL0 or TL1), and the initial value that needs to be reloaded is stored in the MSB register (TH0 or TH1).

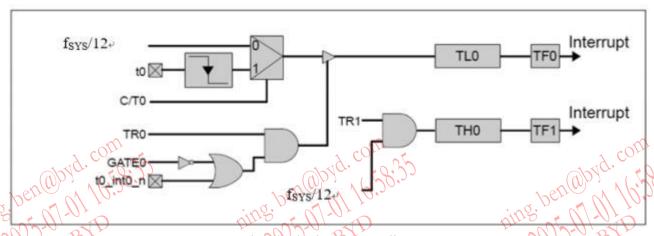
As shown in the figure, the counter control of Mode 2 is the same as Mode 0 and Mode 1.

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However, in mode 2, when TLn accumulates to FFh, the value stored in THn is reloaded to TLn t0/t1, C/T0, C/T1 are all 0, t0\_int0\_n/t1\_int1\_n are all 1, and counting enable is only determined by TR0/1.

#### Mode 3: Two 8-bit timers



Mode 3 logical structure diagram

In mode 3, Timer 0 is two 8-bit timers, at this time Timer 1 stops counting and saves its value. As shown in Figure 5, TL0 is an 8-bit register controlled by the timer 0 control bit. The counter uses GATE as the enable terminal to control the INT\_EXT signal reception.

TH0 is a separate 8-bit timer. TH0 can only be used to calculate the clock period (divide by 12). The control bit and flag bit (TR1 and TF1) of Timer 1 are used as the control bit and flag bit of TH0.

When Timer 0 works in Mode 3, the use of Timer 1 is restricted, because Timer 0 uses the control bit (TR1) and interrupt flag (TF1) of Timer 1. Timer 1 can still be used to generate the baud rate, and the value of Timer 1 in the TL1 and TH1 registers is still valid.

When timer 0 works in mode 3, timer 1 is controlled by the mode bit of timer 1. To start timer 1, you need to set timer 1 to mode 0, 1, or 2. To turn off timer 1, set the mode of timer 1 to 3. Timer 1 can be used as a timer (clock is clk/12), but because TR1 and TF1 are borrowed, overflow interrupts cannot be generated. When timer 0 is working in mode 3, the GATE of timer 1 is valid. t0/t1, C/T0, C/T1 are all 0, t0\_int0\_n/t1\_int1\_n are all 1, and counting enable is only determined by TR0/1.

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## 8.1.1. Timer 0/1 Related Register

D B			SFR registe	r				
Address	Name	RW	Reset	Description				
0x88	TCON	RW	0000_0x0xb	Timer control register				
0x89	TMOD	RW	xx00_xx00b	Timer mode register				
0x8A	TL0	RW	0000_0000b	Timer 0 counter low 8 bit				
0x8B	TL1	RW	0000_0000b	Timer 1 counter low 8 bit				
0x8C	TH0	RW	0000_0000b	Timer 0 counter high 8 bit				
0x8D	TH1	RW	0000_0000b	Timer 1 counter high 8 bit				
0xA8	IEN0	RW	0000b	Interrupt enable register				
0xB8	IPL0	RW	xxxx_0000b	Interrupt priority register0				
		Tiı	mer0/1 SFR regi	ister list				
8.1.1.1. Timer Control Register								
TCON (88)	H) Timer control	register						

## 8.1.1.1. Timer Control Register

1001 (0011) 1	10 01 ( 0 011) 1 mior 10 mior 10 gistor							
Bit number	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	_	IE0	-
R/W	R/W	R/W	R/W	R/W	R/W	_	R/W	-
Reset value	0	0	0	0	0	_	0	_

	Bit number	Bit symbol	Description			
	7,2.00	TF1	Timer 1 overflow flag bit, set by hardware when Timer 1			
	00		overflows, or TH0 of Timer0 overflows in mode 3.			
5.	ben 6	TR1	Timer1 start enable, when set to1, start Timer1, or start			
0	BID	\$	Time0 mode three, TH0 count.			
	5	TF0	Timer 0 overflow flag, set by hardware when Timer0 overflows.			
	4	TR0	Timer0 start enable, set to 1 to start Timer0 counting.			

## 8.1.1.2. Timer Mode Register

TMOD (89H) Timer mode register

Bit number	7	6	5	4	3	2	1	0
Symbol	0 -	_	M1[	1:0]	_	_	M0[	[1:0]
R/W	0.35	_	R/	W.J. COS	35	_	R	WJ. CO
Reset value	20.3	_	0000	0/0/	9.3	_	000	0(:)
170, 71 10	_	_	176	~~ / / / /		_	170	· ~ · · · ·

Bit symbol Description

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(0)5, (20.2						
7~6, 3~2		Reserved				
5-5-4	M1[1:0]	Timer 1 mode selection bit				
77/2		00: Mode 0-13-bit timer				
		01: Mode 1-16-bit timer				
		10: Mode 2-8-bit timer with automatic reloading of initial value				
		11: Mode 3-two 8-bit timers				
1~0	M0[1:0]	Timer 0 mode selection bit				
		00: Mode 0-13-bit timer				
		01: Mode 1-16-bit timer				
		10: Mode 2-8-bit timer with automatic reloading of initial value				
		11: Mode 3-two 8-bit timers				

# 8.1,1.3. Timer 0 Timer

UÉ	TL0 (8AH) Tim	H) Timer 0 timer low 8 bits 118					ning. of Million			
	Bit number	7	6	73/2	84	3	2	1/7/2	80	
	Symbol		TL0[7:0]							
	R/W	R/W								
	Reset value				(	O				

TH0 (8CH) Timer 0 timer high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol		TH0[7:0]						
R/W		R/W						
Reset value	0							

### 8.1.1.4. Timer 1 Timer

TL1 (8BH) Timer 1 timer low 8 bits

. 1	4 4 3 2 ( 0 2 1 1 ) 1 1111									
	Bit number	7	7 6 5 4 3 2 1 0							
	Symbol	TL1[7:0]								
	R/W	R/W								
	Reset value	0								

TH1 (8DH) Timer 1 timer high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol		TH1[7:0]						
R/W		R/W						
Reset value				(	)			

### 8.1.1.5. Interrupt Enable Register

IEN0 (A8H) Interrupt enable register

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	(10)	7(100		( ( )		(()00		((1)	P
<	Bit number	7	6	5ence	14/D.	3	2	o prince	0/0/0
7	Symbol	EA	_ \$	11.8.		ET1	EX1	ETO (	EX0
٢	R/W	R/W	_		_	R/W	R/W	R/W	R/W
	Reset value	0	_		_	0	0	0	0

Bit number	Bit symbol	Description
		Interrupt enable bit
		0: Mask all interrupts (EA takes precedence over the
	EA	respective interrupt enable bits ofthe interrupt sources);
7	ĽΑ	1: Interrupts are enabled. Whether the interrupt request of
		each interrupt source is allowed or disabled is determined by
		the respective enable bit.
		Timer1 interrupt enable bit
3	ET1	0: Disable Timer 1 to request interrupt;
		1: Allow Timer 1 to request interrupt.
		Timer 0 interrupt enable bit
1	ET0	0: Disable timer 0 (TF0) from requesting interrupt;
		1: Enable TF0 flag bit to request interrupt.

# 8.1.1.6. Interrupt Priority Register 0

IPL0 (B8H) Interrupt priority register 0

Bit number	7	6	5	1	3	2	1	0
Dit Hullioci	/	U	3	7	3		1	U
Symbol	0 -	_	_	- ~	PT1	PX2	PT0	PX0
R/W	0.25	_	_	101/g. CO.	R/W	R/W	R/W	R/W
Reset value	20.2	_	-en	3) 1 - 1 (c)	20.0	0	0.00	0/5

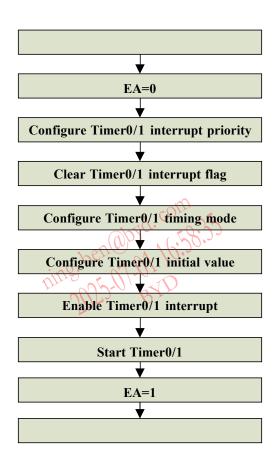
Bit number	Bit symbol	Description Description
3	PT1	Timer1 interrupt priority selection bit.
		0: Timer1 interrupt is low priority;
		1: Timer1 interrupt is high priority
1	PT0	Timer0 interrupt priority selection bit.
		0: Timer0 interrupt is low priority;
		1: Timer0 interrupt is high priority

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# 8.1.2. Timer0/1 Configure Process



Timer0/1 configure process

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## 8.2. Timer 2

ning ben abyd com role ant M. M. 16:5 Timer2 module plays a timing role. The internal main structure of the Timer2 module is a 32bit counter. The timer function is achieved by counting the input clock.he timer function is achieved by counting the input clock. The counting principle of Timer2 is accumulative counting. An interrupt is generated when the count reaches the set value.

Timer2 count clock can choose external XTAL32768Hz/4MHz and internal low-speed clock LIRC 32kHz, which is determined by clock selection register. Timer2has two working modes: single timer mode and auto-reload mode. In either mode, an interrupt will be generated when the timer is completed.

Configure Timer2 function enable through register TIMER2 EN, TIMER2 RLD configure automatic reload mode or manual reload mode, the timing time is determined by registers

TIMER2 SET L and TIMER2 SET H. Timer2 supports interrupt wake-up idle mode 1 function. In the interrupt processing function, software is required to clear the interrupt flag.

Timer2 timing duration formula:

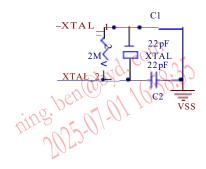
TIMER2 CNT MOD=0:

Ttimer2=Ttimer2\_clk \*({TIMER2 SET H, TIMER2 SET L}+1)

TIMER2 CNT MOD=1:

Ttimer2=65536\*Ttimer2\_clk \*({TIMER2\_SET\_H, TIMER2\_SET\_L}+1)

Note: T<sub>TIMER2</sub> CLK = 1/32768 (s) or T<sub>TIMER2</sub> CLK = 1/4M(s)



External crystal oscillator circuit reference

### Note:

- Any configuration of TIMER2 SET H, TIMER2 SET L, TIMER2 CFG can clear the
- 2. External crystal oscillator circuit is for reference only, the actual Parameter refers to the crystal oscillator specifications;
- XTAL 32768Hz excitation power is recommended to be greater than 1μW; 3.
- 4. XTAL 32768Hz recommends a parallel resistance of  $2M\Omega$ ;
- XTAL 4M recommends a parallel resistance of  $1M\Omega$ .

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D B		(	SFR register	ning. 1507-111
Address	Name	RW	Reset	Description
0x93	TIMER2_CFG	RW	xxxx_x000b	TIMER2 configuration register
0x94	TIMER2_SET_H	RW	0000_0000ь	TIMER2 counter configuration register, high 8 bit.
0x95	TIMER2_SET_L	RW	0000_0000ь	TIMER2 counter configuration register, low 8 bit.
0xAE	INT_PE_STAT	RW	0000_0000Ь	Interrupt status register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register1

Timer2 SFR register list

# 8.2.1.1. TIMER2 Configuration Register

TIMER2 CFG (93H) TIMER2 configuration register

Bit number	7~4	3	2	1	0
Symbol	_	TIMER2_CNT_MOD	TIMER2_CLK_SEL	TIMER2_RLD	TIMER2_EN
R/W	_	R/W	R/W	R/W	R/W
Reset value		0	0	0	0

Bit number	Bit symbol	Description 1 COM
a abya.	8:23	TIMER2 counting step mode selection register
ben 301	TIMER2_CNT_MOD	I. The counting step is 65536 clocks
2000	nine	0: The counting step is one clock
7772		Timer2 clock selection register
2	TIMER2_CLK_SEL	1: Select XTAL32768Hz/4MHz
		0: Select LIRC
		TIMER2 auto reload enable register
1	TIMER2_RLD	1: Auto reload mode
		0: Manual reload mode
		TIMER2 count enable register
		Configuration 1 start timing, configuration 0 stop
		timing; In manual reload mode, the hardware will
0	TIMER2_EN	automatically clear this register after the count is
		completed, stop counting, and in automatic reload mode,
aya		the enable register will be maintained after the count is completed, and the count will automatically restart from

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zero. No matter which mode, configuring this register to
1 during the counting process will start counting from
zero

### 8.2.1.2. TIMER2 Count Value Configuration Register

TIMER2 SET H (94H) TIMER2 count value configuration register, high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol		TIMER2_SET_H[7:0]						
R/W		R/W						
Reset value								
7. co.	25	25 d. com						

	Bit number	Bit symbol	2000	Description	7.00
5	2-0/	TIMER2_SET_H[7:0]	TIMER2 count value	configuration register	, high 8 bits,
0	05-01	Dire	the register will count		7 11 0
`	MIL	,	scanning.		

TIMER2 SET L (95H) TIMER2 count value configuration register, low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol		TIMER2_SET_L[7:0]						
R/W		R/W						
Reset value		0						

	Bit number	Bit symbol	Description
V	ben aby d. cor	TIMER2_SET_L[7:0]	TIMER2 count value configuration register, low 8 bits, the register will re-count when configured during scanning
يا	-	1,10	

### 8.2.1.3. Interrupt Register

INT PE STAT (AEH) Interrupt status register

Bit number	7	6	5	4
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT_TIMER2_STAT	INT_PWM0_STAT	INT_LCD_STAT	INT_LED_STATO
R/W	R/W	R/W. CO	R/W	R/WA.
Reset value	0	1600 16:20.	0	16:3

Bit number Bit symbol Description

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(0)	
3 INT_TIMER2_STAT	TIMER2 interrupt status flag, this bit is cleared by writing
150/00	0, and it can also be cleared by writing TIMER2_CFG
L <sup>3</sup>	1: Interrupt is valid; 0: Interrupt is invalid

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	_	EX4	EX3	EX2	_	_
R/W	R/W	R/W	_	R/W	R/W	R/W	_	_
Reset value	0	0	_	0	0	0	_	_

	Bit number	Bit symbol	Description	
	7 .0	EX7	WDT/Timer2/PWM0 interrupt enable	com
	hyd. Co.	0.35	1: WDT/Timer2/PWM0 interrupt enable;	abyd. Co.
2	200), 16	20.3	0: WDT/Timer2/PWM0 interrupt disable	1-50 (0) (1/2)

			o. WEITHING 27 WIVE Interrupt disable						
300	IRCON1 (F1H)	Interrupt	flag registe	rolg.	1011			108.	
III	Bit number	7	6	202	4	3	2	J. (M)	1/80
	Symbol	IE7	IE6		IE4	IE3	IE2		_
	R/W	R/W	R/W	_	R/W	R/W	R/W	_	_
	Reset value	0	0	_	0	0	0	_	_

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2/PWM0 interrupt flag
		1: WDT/Timer2/PWM0 interrupt flag;
		0: Clear WDT/Timer2/PWM0 interrupt flag

IPL1 (F6H) Interrupt priority register1

	Bit number 7	6	5	DD14	8:3	2	1 0000
7	Symbol IPL1.	7 IPL1.6	perio	IPL1.4	IPL1.3	IPL1.2	per William
ع ا	R/W R/W	R/W	MILE OF	R/W	R/W	R/W S	111.8
	Reset value 0	0		0	0	0	

Bit number	Bit symbol	Description
7	IPL1.7	WDT/Timer 2/PWM0 interrupt priority bit
		1: WDT/Timer 2/PWM0 interrupt is high priority;
		0: WDT/Timer 2/PWM0 interrupt is low priority

# 8.2.2. Timer2 Secondary Bus Register

om	om	om
ahyd. co.35	Secondary bus regis	iter)
Address Name	RWReset	Description
0x2D PD_ANA	RW x111_xx11b	Analog module switch register
0x63 XTAL_CLK_SEL	RW xxxx_xxx0b	Crystal frequency selection register

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### Timer2 List of secondary bus registers

# 8.2.2.1. Analog Module Switch Register

PD ANA (2DH) Analog module switch register

Bit number	7	6	5	4	3~1	0
Symbol	_	PD_LVDT	_	PD_XTAL_32K	-	PD_ADC
R/W	_	R/W	_	R/W	_	R/W
Reset value	_	1	_	1	_	1

Bit number	Bit symbol	Description
g, ben abyd, co	PD_XTAL_32K	PA port crystal oscillator circuit (32768Hz/4MHz) control register 1: Off; 0: On, default off

### 8.2.2.2. Crystal Frequency Selection Register

XTAL CLK SEL (63H) Crystal frequency selection register

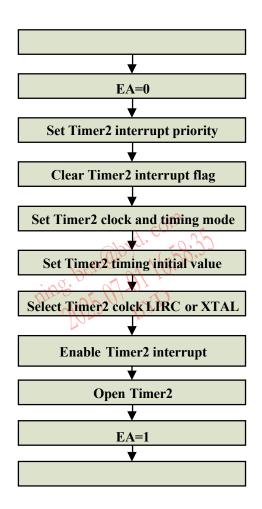
Bit number	7	6	5	4	3	2	1	0
Symbol	_						_	
R/W	_	_		_	_	_	_	R/W
Reset value	_			_		_	_	0

COLL A	COMP.	c Oliv
Bit number Bit symbol	Description	ahyd. co
Dev (1) 70:20.	Crystal frequency selection register	ben as 1/1:30
(100/11)	1: Select 4MHz;	ning of Milli
J 172 Dr.	0: Select 32768Hz	1/1/2-0

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## 8.2.3. Timer2 Configure Process



Timer2 configure process table

### Timer2 configure process:

- 1. Configure the timer setting register TIMER2\_SET\_H/TIMER2\_SET\_L and step configuration TIMER2\_CNT\_MOD;
- 2. Then configure the auto-reload enable register TIMER2\_RLD as needed, and set it to 1 if automatic cycle counting is needed, otherwise it is set to 0;
- 3. Finally, in the configuration timing enable register TIMER2\_EN, turn on the timing configuration TIMER2\_EN=1;
- 4. Stop timing: TIMER2 EN=0.

### **Note:**

- 1. TIMER2\_EN=0x01 operation should be placed at the end ofall configurations;
- 2. During the timing of TIMER2, it is forbidden to change the related configuration of Timer2. If you want to modify it, you need to stop the timing first.
- 3. For precise timing, in the automatic reload mode, the three registers of TIMER2 are not allowed to be configured during interrupt processing.

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### 8.3. Timer3

Timer3 is a 16-bit timer. Configure Timer3 function enable through register TIMER3\_EN.

TIMER3\_RLD configures automatic reload mode or manual reload mode. The timing time is determined by registers TIMER3\_SET\_L and TIMER3\_SET\_H.

ning ben@byd 16:5

The timer clock can be divided by 12 or 4 of the 24MHz clock, which is determined by the clock selection register. Timer3 supports the interrupt wake-up idle mode 0 function.

Single timing mode: After a timing is completed, the hardware will automatically pull down TIMER3 EN to stop timing.

Automatic reset mode: The hardware will automatically reload the setting value, and TIMER3\_EN will continue to be maintained at 1 to restart the next timing; the software will stop TIMER3 counting by writing 0 to the register TIMER3\_EN, or modify the timing mode midway. The TIMER3 timing duration formula is:

At 12 frequency,  $T_{TIMER3} = T_{CLK\_24M}*(\{TIEMR3\_SET\_H, TIMER3\_SETL\} + 1)*12$  At 4 frequency,  $T_{TIMER3} = T_{CLK\_24M}*(\{TIEMR3\_SET\_H, TIMER3\_SETL\} + 1)*4$ 

### Note:

Configure any TIMER3 SET H, TIMER3 SET L, TIMER3 CFG to clear the counter.

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# 8.3.1. Timer3 Related Registers

AddressNameRWResetDescription0x84TIMER3_CFGRWxxxx_x000bTIMER3 configuration register0x85TIMER3_SET_HRW0000_000bTIMER3 count value configuration register, high 8 bits0x86TIMER3_SET_LRW0000_000bTIMER3 count value configuration register, low 8 bits0xAEINT_PE_STATRW0000_000bInterrupt status register0xE1IRCON2RW0000_000bInterrupt flag register 20xE7IEN2RW0000_000bInterrupt enable register 20xF4IPL2RW0000_000bInterrupt priority register2Timer3 SFR register list	SFR register							
0x85       TIMER3_SET_H       RW       0000_0000b       TIMER3 count value configuration register, high 8 bits         0x86       TIMER3_SET_L       RW       0000_0000b       TIMER3 count value configuration register, low 8 bits         0xAE       INT_PE_STAT       RW       0000_0000b       Interrupt status register         0xE1       IRCON2       RW       0000_0000b       Interrupt flag register 2         0xE7       IEN2       RW       0000_0000b       Interrupt enable register 2         0xF4       IPL2       RW       0000_0000b       Interrupt priority register2         Timer3 SFR register list	Address	Name	RW	Reset	Description			
0x85TIMERS_SET_HRW0000_0000bregister, high 8 bits0x86TIMER3_SET_LRW0000_0000bTIMER3 count value configuration register, low 8 bits0xAEINT_PE_STATRW0000_0000bInterrupt status register0xE1IRCON2RW0000_0000bInterrupt flag register 20xE7IEN2RW0000_0000bInterrupt enable register 20xF4IPL2RW0000_0000bInterrupt priority register2Timer3 SFR register list	0x84	TIMER3_CFG	RW	xxxx_x000b	TIMER3 configuration register			
0x86       TiMER3_SET_L       RW       0000_0000b       register, low 8 bits         0xAE       INT_PE_STAT       RW       0000_0000b       Interrupt status register         0xE1       IRCON2       RW       0000_0000b       Interrupt flag register 2         0xE7       IEN2       RW       0000_0000b       Interrupt enable register 2         0xF4       IPL2       RW       0000_0000b       Interrupt priority register2         Timer3 SFR register list	0x85	TIMER3_SET_H	RW	0000_0000Ь				
0xE1     IRCON2     RW     0000_0000b     Interrupt flag register 2       0xE7     IEN2     RW     0000_0000b     Interrupt enable register 2       0xF4     IPL2     RW     0000_0000b     Interrupt priority register2       Timer3 SFR register list	0x86	TIMER3_SET_L	RW	0000_0000ь				
0xE7     IEN2     RW     0000_0000b     Interrupt enable register 2       0xF4     IPL2     RW     0000_0000b     Interrupt priority register2       Timer3 SFR register list	0xAE	INT_PE_STAT	RW	0000_0000b	Interrupt status register			
0xF4 IPL2 RW 0000_0000b Interrupt priority register2 Timer3 SFR register list	0xE1	IRCON2	RW	0000_0000b	Interrupt flag register 2			
Timer3 SFR register list	0xE7	IEN2	RW	0000_0000ь	Interrupt enable register 2			
$M_{2}$	0xF4	IPL2	RW	0000_0000ь	Interrupt priority register2			
3.3.1.1. TIMER3 Configuration Register	Timer3 SFR register list							
3.3.1.1. TIMER3 Configuration Register	$M_{D-A}$							
	8.3.1.1. TIMER3 Configuration Register							

## 8.3.1.1. TIMER3 Configuration Register

TIMER3 CFG (84H) TIMER3 configuration register

	(* 12) 221223 21223						
Bit number	7~3		1	0			
Symbol	_	TIMER3_CLK_SEL	TIMER3_RLD	TIMER3_EN			
R/W	_	R/W	R/W	R/W			
Reset value	_	0	0	0			

Bit number	Bit symbol	Description COM				
all pyd.	28:23	TIMER3 timing clock selection register.				
bern 201	TIMER3_CLK_SEL	1: Select clk_24M/4;				
しんりしょう	nit	0: Select clk_24M/12				
Mrs Dr	TIMER3 RLD	TIMER3 auto reload enable register				
1	TIMEKS_KLD	1: Auto reload mode; 0: Manual reload mode.				
		TIMER3 count enable register Configure 1 to start timing,				
		configure 0 to stop timing In manual reload mode, the				
0	TIMER3_EN	hardware will automatically clear this register after the				
		timing is completed.				
		Configure the register during the scan process to re-count.				

### 8.3.1.2. TIMER3 Count Value Configuration Register

TIMER3 SET H (85H) TIMER3 count value configuration register, high 8 bits

Symbol TIMER3 SET H[7:0]	Bit number	7 6	3 3 4	3	2	og. Penic	
11 2	Symbol			SH I HI / · () I	77	5-00	BYD

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OCO R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
7~0	TIMER3_SET_H[7:0]	TIMER3 count value configuration register, high 8 bits, the register will count again when configured during scanning.

TIMER3 SET L (86H) TIMER3 count value configuration register, low 8 bits

	_ ( = = - / -				<del></del>					
Bit number	7	6	5	4	3	2	1	0		
Symbol		TIMER3_SET_L[7:0]								
R/W	0	R/W								
Reset value	6.35			myd. co	6.6.6			Mg. Co		

5	Bit number	Bit symbol	Description in the second
	My BAL	(	TIMER3 count value configuration register, low 8 bits,
	7~0	TIMER3_SET_L[7:0]	the register will re-count when configured during
			scanning.

### 8.3.1.3. Interrupt Register

INT\_PE\_STAT (AEH) Interrupt status register

	\ / I	8		
Bit number	7	6	5	4
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT
R/W	R/W	R/W COTT	R/W	R/W COM
Reset value	28:22		0	(1) (1) (1) (1) (1) (1) (1) (1) (1) (1)
Bit number	3	ben 2/1/0.3	1	pen 001/00
Symbol	INT TIMER2 STATU	INT PWM0 STAT	INT LCD STATE	INT LAD STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
		TIMER3 interrupt status flag, this bit is cleared by writing
6	INT_TIMER3_STAT	0, and it can also be cleared by writing TIMER3_CFG
		1: Interrupt is valid; 0: Interrupt is invalid

IRCON2 (E1H) Interrupt flag register 2

Bit number 7	6	5	4 000 3	2	1	0.00
Symbol IB15	IE14	IE13	IE12 IE11	IE10	IE9	10 PE8, 29
R/W R/W	R/W	RXWET	R/W R/W	R/W	RAW	RMO
Reset value 0	0 (	11,80 5	0 0	0	mgo C	1-00

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		7().5		$(0)_{\Sigma}$ , $(2)$
ζ.	Bit number	Bit symbol	Description	pena Wip.
9	25-01-0	×	Timer3/PWM1 interrupt enable	ning of Ol-O.
	4	IE12	1: Timer3/PWM1 interrupt enable;	J) [2
Į			0: Timer3/PWM1 interrupt disable	

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	EX15	EX14	EX13	EX12	EX11	EX10	EX9	EX8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

	Bit number	Bit symbol	Description	oth
	abyd. Co	6.35	Timer3/PWM1 interrupt enable	abyd. co
	ber 04, 16;	EX12	1: Timer3/PWM1 interrupt enable;	pen(0) 1 / (1)
Ę			0: Timer3/PWM1 interrupt disable	sing. I die

IPL2 (F4H) Interrupt priority register2

()	1 1	J B					111110	
Bit number	7	6	5	4	3	2	1	0
Symbol	IPL2.7	IPL2.6	IPL2.5	IPL2.4	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

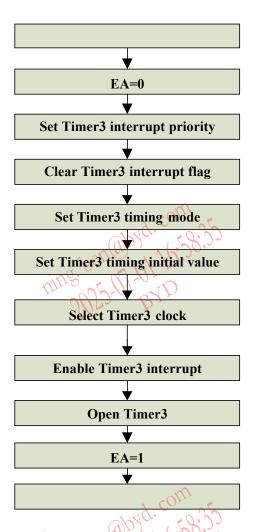
Bit number	Bit symbol	Description
		Timer3/PWM1 priority selection bit.
4	IPL2.4	1: Timer3/PWM1 interrupt is high priority;
		0: Timer3/PWM1 interrupt is low priority



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# 8.3.2. Timer3 Configure Process



Timer3 Configuration flow chart

### Timer3 Configuration process:

- 1. Configure the timer setting register TIMER3\_SET\_H/TIMER3\_SET\_L and step configuration TIMER3 CNT MOD;
- 2. Then configure the auto-reload enable register TIMER3\_RLD as needed, and set it to 1 if automatic cycle counting is needed, otherwise it is set to 0;
- 3. Finally, in the configuration timing enable register TIMER3\_EN, turn on the timing configuration TIMER3\_EN=1;
- 4. Stop timing: TIMER3 EN=0.

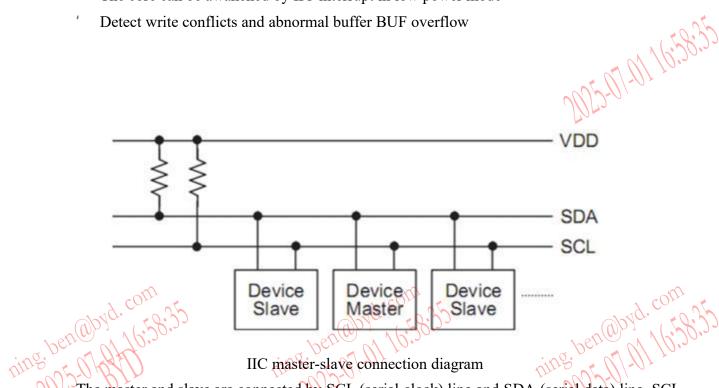
### Note:

- 1. TIMER3\_EN=0x01 operation should be placed at the end ofall configurations;
- 2. During the timing of TIMER3, it is forbidden to change the related configuration of Timer.If you want to modify it, you need to stop the timing first;
- 3. If accurate timing is required, in the automatic reload mode, it is not allowed to configure TIMER3\_EN=0x01 during interrupt processing.

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The BF7515CM44-LJTX supports standard and fast IIC communication, and has the following characteristics:

- Two serial interfaces: serial data line SDA and serial clock line SCL
- Comply with philips standard communication protocol
- Transmission rate: 100 kHz, 400 kHz
- Support 7-bit address addrring
- With the function of extending the low level of the clock
- The core can be awakened by IIC interrupt in low power mode
- Detect write conflicts and abnormal buffer BUF overflow



The master and slave are connected by SCL (serial clock) line and SDA (serial data) line. SCL and SDA must be connected with pull-up resistors (4.7k~10k recommended).

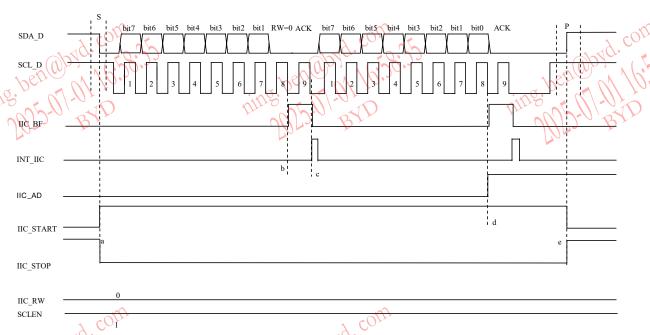
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# 9.1. Communication Timing

The BF7515CM44-LJTX uses hardware slave. When host read /write data, after the slave receives the address, if the address matches, an interrupt is generated and a valid response signal is sent. And an interrupt is generated after the host computer writes the eighth clock of the data, and the host will not generate an interrupt signal when sending the stop signal. IIC timing diagram as follows:

### IIC host write timing diagram



IIC write not pull down clock line diagram

As shown in the above figure, the schematic diagram of the clock line is not pulled down during the host write operation. From this, you can see the changes of the IIC bus and some internal signal changes.

First the host sends a start signal IIC\_START, and the slave sets the IIC\_START status bit after detecting the IIC\_START signal, as shown by the dotted line a in the figure.

Then the host sends the address bytes and write flag bit, and the slave automatically compares with its own address after receiving the address byte. Set IIC\_BF after the falling edge of the eighth clock if the address matches, as shown by the dotted line b in the figure.

An interrupt signal INT\_IIC is generated after the falling edge of the ninth clock, as shown by the dotted line c.The MCU executes interrupt subroutine device needs to read IICBUF. Even if this data is not useful, it needs to be operated. Reading the IICBUF operation will indirectly clear the START\_BF.

The host continues to send messages. The IIC\_BF is also set after the falling edge of the 8th clock of the 2nd byte, and the IIC\_AD flag is also set. The currently received byte of the flag is data, and the stop signal has no effect on the IIC\_STOP flag. That is, the stop signal IIC\_STOP is detected, as shown by the dotted line d. And the IIC\_AD flag will not be cleared; The interrupt is

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IIC STOP

IIC RW

SCLEN

generated after the falling edge of the ninth clock, and the interrupt subroutine requires the same operation.

If the host wants to send multiple bytes, it can continue to send. The figure above only shows the case where the host sends a data. Finally, the host sends a stop signal IIC\_STOP after sending all the data, indicating the end of the communication, releasing the IIC bus, and the bus enters the idle state.

# HC host write pull low timing diagram SDA\_D SCL\_D IIC\_AD IIC\_START

IIC write low clock line diagram

Software set, need to read IICBUF before

Pulled down by hardware

As shown in the above figure, it is a schematic diagram of pulling down the clock line during the host write operation, from which you can see the changes of the IIC bus and some internal signal changes.

First the host sends a start signal IIC\_START, and the slave sets the IIC\_START status bit after detecting the IIC\_START signal, as shown by the dotted line a.

Then the host sends the address bytes and write flag bit, and the slave automatically compares with its own address after receiving the address byte. Set IIC\_BF after the falling edge of the eighth clock if the address matches, as shown by the dotted line b. An interrupt signal INT\_IIC is generated after the falling edge of the ninth clock, as shown by the dotted line c.

SCLEN will be automatically cleared by hardware after the falling edge of the 9th clock. This process is used to process or read data from the slave. Even if this data is not useful, reading IICBUF will cause IIC\_BUF to be cleared indirectly, as shown by the dotted line d. Software sets SCLEN to release the clock line. As shown by the dotted line e.

After the master detects that the slave releases the SCL, it continues to send the synchronous clock. The IIC\_BF is also set after the falling edge of the 8th clock of the 2nd byte, and the IIC\_AD flag is also set, he currently received byte of the flag is data, as shown by the dotted line f, and the stop signal has no effect on the IIC\_STOP flag. Hat is, the stop signal IIC\_STOP is detected, and the IIC\_AD flag will not be cleared; The interrupt is generated after the falling edge of the ninth clock

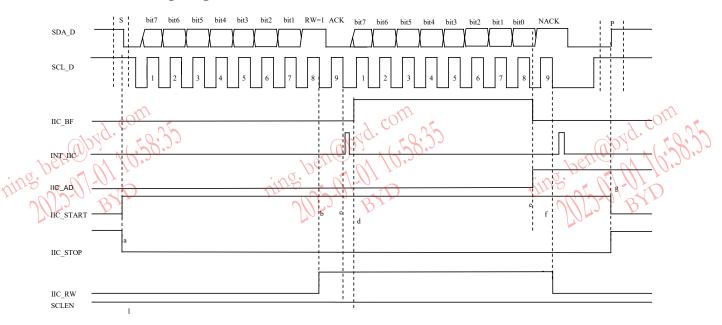
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If the host wants to send multiple bytes, it can continue to send, as shown in the figure above, it only indicates that the host sends one piece of data. The situation that needs to be noted is that when the host sends the last data, the function of pulling down the clock line is not enabled.

Finally, the host sends a stop signal IIC\_STOP after sending all the data, indicating the end of the communication, releasing the IIC bus, and the bus enters the idle state.

### IIC host read timing diagram



IIC master reading does not pull down the clock line diagram

As shown in the above figure, it is a schematic diagram of pulling down the clock line during the host write operation, from which you can see the changes of the IIC bus and some internal signal changes.

First the host sends a start signal IIC\_START, marking the beginning of communication. As shown by the dotted line a. The internal circuit detects the IIC\_START signal timing and sets the status flag IIC\_START.

Then the host sends the address bytes and write flag bit, IIC\_RW = 1, indicates that the host reads the slave. In the case of address match, after the falling edge of the eighth clock, the status bit IIC\_RW is set. As shown by the dotted line b; If Address does not match, IIC\_RW will not be set.

An interrupt signal INT\_IIC is generated after the falling edge of the ninth clock. As shown by the dotted line c. Ballast the data in IICBUFFER to IICBUF, IIC is set, as shown by the dotted line d, and the highest bit is sent to the bus. After the eighth clock, one byte of data is sent, IIC\_BF is set to clear. At the same time, the address data flag will also be set. As shown by the dotted line e.

An interrupt signal INT\_IIC is generated after the falling edge of the ninth clock. If the host needs to read the slave, the host replies with a valid acknowledge bit ACK and continues to communicate. If the data require by the host has been read, the host replies with an invalid response NACK, and then sends a stop signal IIC\_STOP to stop the communication. In the diagram, the host only reads one piece of data, and then responds with NACK, and then sends the IIC\_STOP signal to terminate the communication. When the NACK is detected, the read/write flag IIC RW is cleared

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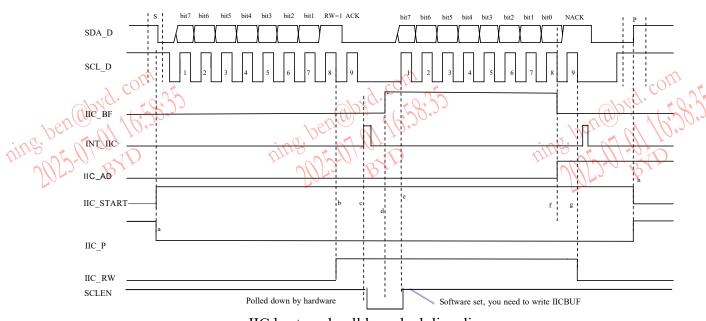


by hardware. As shown by the dotted line f.

If the host sends a NACK, the slave SCLEN will not be automatically pulled low

Finally, the host sends a stop signal IIC STOP after reading all the data, indicating the end of the communication. When the IIC STOP signal is detected the status bit IIC STOP is set and IIC START is cleared. Release IIC bus. As shown by the dotted line g. The bus enters the idle state.

### IIC host read pull low timing diagram



IIC host read pull low clock line diagram

As shown in the figure above, it is the timing diagram of the master reading the slave clock line low. From the figure, we can know the changes of the bus and the changes of the internal signals of some circuits

First the host sends a start signal IIC START, marking the beginning of communication. As shown by the dotted line a. The internal circuit detects the IIC START signal timing and sets the status flag IIC START.

Then the host sends the address byte after the IIC START signal. IIC RW = 1, indicates that the host reads the slave. In the case of Address matching, after the falling edge of the eighth clock, status bit IIC RW set. As shown by the dotted line b. Will not be set ifthe addresses do not match

An interrupt signal INT IIC is generated after the falling edge of the ninth clock. As shown by the dotted line c. SCLEN will also be automatically pulled low by the hardware after the falling edge of the ninth clock. This period is used to process or prepare data from the slave, then write the prepared data to IICBUF, set SCLEN in software, and release the clock line. As shown by the dotted line d. In writing the data to the IICBUF, the IICBUF will be set, indicating that the IIC is full at this time. As shown by the dotted line e. Software sets SCLEN, releases the clock line

After the master detects that the slave releases the SCL, it continues to send the synchronous clock and read the slave data. After the falling edge of the 8th clock, one byte of data has been sent and IIC BF cleared. At the same time, the address data flag will also be set, indicating the currently

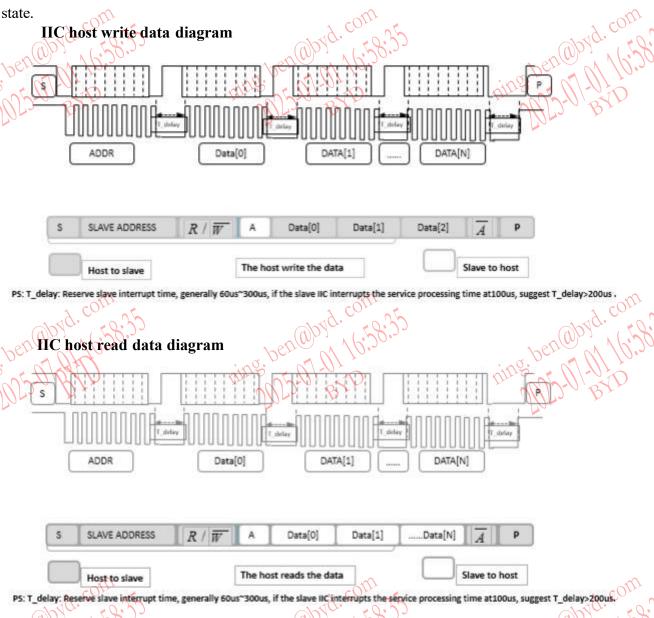
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transmitted byte data. As shown by the dotted line f.

An interrupt signal INT\_IIC is generated after the falling edge of the ninth clock. If the host needs to continue to read the slave, the host replies with a valid acknowledge bit ACK and continues to communicate; If the data require by the host has been read, the host replies with an invalid response NACK, and then sends a stop signal IIC\_STOP to stop the communication. When the NACK is detected, the read/write flag IIC\_RW is cleared by hardware. As shown by the dotted line g.

Finally, the host sends a stop signal IIC\_STOP after reading all the data, indicating the end of the communication. When the IIC\_STOP signal is detected the status bit IIC\_STOP is set and IIC\_START is cleared. Release IIC bus. As shown by the dotted line h. The bus enters the idle



At the eighth clock slave send ack, IIC interrupt occurs at the ninth clock fulling edge. It is recommended that the host delay 60us~300us when the ninth clock fulling edge is sent. Reserve the

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slave IIC interrupt service data preparation time, and then send the clock signal.

# 9.2. IIC Port Configuration

The BF7515CM44-LJTX provides secondary bus register PERIPH IO SEL1, configure Bit4 of this register to select IIC port.

Write 1 in register PERIPH IO SEL1.4, then PE4, PE5 will be configured as IIC function:

SCL0A, PE4 is IIC serial clock line;

SDA0A, PE5 is IIC serial data line.

Write 0 in register PERIPH IO SEL1.4, then PC4, PC5 will be configured as IIC function:

SCL0B, PC4 is IIC serial clock line;

# 9.3. IIC Related Register

SCLUI	o, i C <del>a</del> is iiC sciia	i clock line,	<b>√</b>	$\sim$
SDA0	B, PC5 is IIC seria	ıl data line.	7. co,	d. com
(b)	. (.28:33		abya.	9:33 (19:4)
9.3. HC	Related Regis	ter	pen(m) 1/0.	pente 1 10:10.
8 - 11-1		oine	2 11-11	ning of 11-11
JOIN B	37.0	,	SFR register	11/12-0, BX
Address	Name	RW	Reset	Description
0xE3	IICADD	RW	0000_000xb	IIC address register
0xE4	IICBUF	RW	0000_0000b	IIC transmit receive data register
0xE5	IICCON	RW	xx01_0000b	IIC configuration register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xE8	IICSTAT	R/RW	0100_0100b	IIC status register
0xE9	IICBUFFER	RW	0000_0000b	IIC transmit receive data buffer register
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register1

IIC SFR register list



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### 9.3.1. IIC Address Register

70	111				20	<b>BF</b> 7	515CM	44-LJTX
9.3.1. IIC Ad			2025	0/01/6	9.3		3025-	7.01.10:59
Bit number	7	6	5	4	3	2	1	0
Symbol		IICADD[7:1]						_
R/W		R/W						_
Reset value				0				_

Bit number	Bit symbol	Description
7~1	IICADD[7:1]	IIC address register

# 9.3.2. IIC Transmit Receive Data Register

1260 (0) 1 1 (2)	30.3	eceive Data Register	m 5.58:35	ing ben abyd. Com
Bit number	7	6	3	2
Symbol		IId	CBUF	
R/W		]	R/W	
Reset value			0	

Bit number	Bit symbol	Description
7~0	IICBUF	IIC transmit and receive data buffer

The specific application process is as follows:

In the send state, after the data is ballasted into the IICBUF, under the synchronous clock of the host. The data is sequentially shifted and sent out, the high position is in front. After 8 clocks, one byte is sent.

, n the rece iv e st a te, a fter hos t's 8 c 1 the 9th clock, an interrupt is generated, telling the CPU to read the data in the IICBUF.

Writing data to IICBUF is conditional, when RD SCL EN=1, only IIC RW=1, and SCLEN=0 can write data into IICBUF; Otherwise, the operation of writing IICBUF is prohibited. That is to say, if the condition is not satisfied, the operation of writing IICBUF cannot be successful, and the data cannot be written. IICBUF data will not change, but will also cause write confilicts.

For example: IICBUF already has been 55h. In case the condition of writing IICBUF is not satisfied, we want to write data 00h into IICBUF. The result is that the data in IICBUF is still 55h, and the write conflict flag IIC WCOL is set to tell the user that the operation is abnormal.

When RD SCL EN=0, the data to be the slave is the value of the ballast IICBUFFER register when the interrupt signal is generated.

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	7 60			DI'/	JIJCM44-LJIA
عار	0201-01	onfiguration Regi	-0501-01	9.33	2025-07-01 16:58
	Bit number	7	6	5	4
	Symbol	_	_	IIC_RST	RD_SCL_EN
	R/W	_	_	R/W	R/W
	Reset value	_	1	0	1
	Bit number	3	2	1	0
	Symbol	WR_SCL_EN	SCLEN	SR	IIC_EN
	R/W	R/W	R/W	R/W	R/W
	Reset value	0	0	0	0

	70.17	
Bit number	Bit symbol	ben Description
7-6		Reserved
1052-0		IIC module reset signal
5	IIC_RST	1: IIC module reset operation,
		0: IIC module works normally
	RD_SCL_E	The host reads the low clock line control bit
4	N	1: Enable the host to read and pull down the clock line function,
		0: Disable the host read and pull down clock line function
	WR_SCL_E	The host writes the low clock line control bit,
3	N	1: Enable the function of writing and pulling down the clock line,
		0: Disable the function of writing and pulling down the clock line
2	SCLEN	IIC clock enable bit:
2		1: clock works normally, 0: lows the clock line
Tra		IIC conversion rate control bit
Bli	)	1: The conversion rate control is turned off to adapt to the standard
1	SR	speed mode (100K);
		0: Conversion rate control is enabled to adapt to fast speed mode
		(400K)
		IIC work enable bit
0	IIC_EN	1: IIC works normally
		0: IIC does not work

The IICCON register is used to control the communication operation.

**IICEN** is module enable signal, when IICEN=1, the circuit works.

SR is the conversion rate control bit, SR=1 conversion rate control off, port adapted to 100Kbps communication.

**SCLEN** is clock enable control bit, although the slave cannot generate the communication clock, the slave can extend the low time of the clock according to the protocol. SCLEN=0, clock line is locked at low level; SCLEN=1, release clock line. The premise of extending the low level of

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the clock is IICEN=1, otherwise the internal circuit will not have any effect on the IIC bus. SCLEN is often used to extend low time and make the host enter the wait state, so that the slave has enough time to process the data.

**WR\_SCL\_EN** is write low line control bit. When it is 1 to enable the interrupt to pull down the clock line, when it is 0, it does not enable the interrupt to pull down the clock line.

IIC\_RW=0, according to the communication rate of the host and the time of processing the interrupt, it is determined whether to lower the clock line, that is, configure the WR SCL EN bit.

When the CPU can process the interrupt and exit the interrupt within 8 IIC clocks.

WR\_SCL\_EN=0 disable pull down the clock clock line function. At this time, the hardware will not automatically pull down the clock line when the interrupt arrives. When the CPU cannot process the interrupt and exit in the 8 IIC clocks, WR\_SCL\_EN=1 enables the clock line to be pulled down. At this point, the hardware automatically pulls down the clock line when the interrupt arrives, forcing the host to enter the wait state. When the data written to the IIC is read by the CPU, the software sets SCLEN.

**RD\_SCL\_EN** is read low line control bit. When it is 1 to enable the interrupt to pull down the clock line, when it is 0, it does not enable the interrupt to pull down the clock line.

RD\_SCL\_EN=1, when the slave receives the address byte or sends one byte and the host sends, SCLEN will be automatically pulled low by hardware, forcing the host to the enter the wait state. The release the IIC clock from the slave, the following two operations are required: first write the data to be sent to the IIC, set the software in IICBUF in SCLEN. The purpose of this design is to ensure that the data to be sent has been written in the IICBUF before the SCL is pulled high.

RD\_SCL\_EN=0, when the slave receives the address byte or sends one byte and the host sends an ACK, the slave immediately polls the data prepared in the IICBUFFER register to the transmit buffer register and then to the data line. Therefore, in order to ensure that data transmitted each time is correct, IICBUFFER prepares the next data to be sent in the interrupt service routine. The data received by the host is the last interrupted data, and the first time the data is received is ready for initialization.

**Note**: When you need to pull down the clock line, that is, WR\_SCL\_EN/RD\_SCL\_EN=1. Software should turn off the clock line until the last Byte data is sent and received. That is, WR\_SCL\_EN/RD\_SCL\_EN=0, the software should turn on the write low pull clock line before sending and receiving the last Byte data. This kind of operation can be self-regulated according to whether the host is software or hardware.

**IIC\_RST** is IIC module control enable bit, enable the IIC module reset function for 1 and disable the IIC module reset function when 0. Pay attention to configuration 1 reset IIC module all DFF triggers. The reset terminal of IIC\_RST is global reset, and the other reset terminal are iic\_rst\_n. All iic\_rst writes 0 first, then operate other register configurations.

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# 9.3.4. IIC Status Register

Sei Co	Semiconductor			515CM44-LJTX
9.3.4. HC St	atus Register  ) IIC status register	2025-07-01 16	9.23	2025-07-01 16:58:5
Bit number	7	6	5	4
Symbol	IIC_START	IIC_STOP	IIC_RW	IIC_AD
R/W	R	R	R	R
Reset value	0	1	0	0
Bit number	3	2	1	0
Symbol	IIC_BF	IIC_ACK	IIC_WCOL	IIC_RECOV
R/W	R	R	R/W	R/W
Reset value	0	1	0	0

2/1/0· 20:72		my (1, 10, 1)
Bit number	Bit symbol	Description Description
2 W/11 ,	W.	Start signal flag
1000	IIC_START	1: Indicates that the start bit is detected;
		0: Indicates that the start bit is not detected.
		Stop signal flag
6	IIC_STOP	1: Means in the stop state;
		0: Means that the stop bit is not detected.
		Read and write flag
		Record the read/write information obtained from the address
5	IIC_RW	byte after the last address match,
		1: Indicates read operation;
		0: Means write operation.
		Address data flag
481	IIC_AD	1: Indicates that the most recently received or sent byte is data;
<b>y</b>		0: Indicates that the most recently received or sent byte is an address.
		IICBUF full flag bit: when receiving in IIC bus mode
		1: Indicates that the reception is successful and the buffer is full;
		0: Indicates that the reception is not completed and the buffer is still empty
3	IIC_BF	When sending in IIC bus mode:
		1: Indicates that data transmission is in progress (not
		including the response bit and stop bit), and the buffer is still full;
		0: Indicates that the data transmission has been completed
		(not including the response bit and stop bit), and the buffer is

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-(0)	.50.33	
pence My	0.5	empty.
0501-0		Reply flag
2	IIC_ACK	1: Indicates an invalid response signal; 0: indicates an effective response signal.
		Write conflict flag
1	IIC_WCOL	1: Indicates that when the IIC is sending the current data, new data is trying to be written into the sending buffer; the new data cannot be written into the buffer;
		0: No write conflict occurred.
		Receive overflow flag
0	IIC_RECOV	1: Indicates that new data is received when the previous data received by IIC has not been taken away, and the new data cannot be received by the buffer;
		0: Indicates that no receive overflow has occurred.

IIC status register, used to reflect the status in the communication process, for users to query.

**IIC\_START:** Start signal status bit, IIC\_START is set when the start signal is detected, Indicating that the bus is busy.

**IIC\_STOP:** Stop signal status bit, IIC\_START is set when the start signal is detected, indicating that the bus is idle. When the start signal is detected, the hardware is cleared, indicating that communication begins.

**IIC\_AD:** Address data flag. It indicates whether the byte currently received or sent is an address or data. IIC\_AD =0, flag is currently received or sent byte is the address; IIC\_AD = 1 flag is currently received or sent byte is the data; Start signal, stop signal, non-response signal have no effect on this status bit. This status bit change occurs on the falling edge of the eighth clock.

IIC\_RW: Read and write flag. The flag bit is recorded the read and write information bits obtained from the address is matched. IIC\_RW = 1 means the host reads the slave. RW = 0 means the host writes the slave. Start signal, stop signal, non-answer signal (NACK) is cleared IIC\_RW. This status bit change occurs on the falling edge of the eighth clock.

**IIC\_BF:** BUFFER full flag. It indicates that the transceiver buffer is currently full or empty. IIC\_BF=0 indicates that the buffer does not receive data and the buffer is empty; IIC\_BF=1 indicates that the buffer receive data and the buffer is full. This status bit can only be set and cleared indirectly, not directly.

Address matching and IIC\_RW=0, IIC\_BF will be set after the falling edge of the eighth clock, indicating that the IICBUF has received the data. The IICBUF should be read during the execution of the interrupt routine, and the read IICBUF will indirectly clear the BF flag. If the host does not read IICBUF and the host continues to send data, a receive overflow will occur. Although the slave still receives the host to send data and is ballasted to the IICBUF.

IIC\_RW=1 indicates the operation of the master to read the slave, the slave operation needs to write data to the IICBUF, and the slave writes IICBUF operation to set the IICBUF. The software then sets SCLEN to release the clock line; The host The host sends the synchronous clock. After the

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8th clock is passed, the IICBUF is cleared by hardware after the data in the IICBUF is sent out.

MC\_ACK: Answer flag. Regardless of whether the host is a read or write operation, the slave samples the data line from the rising edge of the ninth clock and records the response information. The acknowledge bits are divided into a valid acknowledgment ACK and a non-valid acknowledgement bit NACK. That is to say, the rising edge of the ninth clock samples the data to 0, indicating that the ACK is valid, and the IIC\_ACK is cleared. If data 1 is sampled, NACK is set, indicating non-response. After the non-acknowledgment signal, the host will send a stop signal to announce the end of the communication. The start signal will clear this status bit.

**IIC\_WCOL:** Write conflict flag. IICBUF only when IIC\_RW=1, RD\_SCL\_EN=1 and SCLEN=0 can be written by the CPU. Any other attempt to write to IICBUF is forbidden. If the above conditions are not met, the write IICBUF operation occurs. Then the data will not be written to IICBUF, and the conflict flag IIC WCOL will be set. This flag needs to be cleared by software.

IIC\_RECOV: Receive overflow flag. In the case of IICBUF full, that is, in the case of data in the IICBUF. If IIC received new data, it will receive overflow and IIC RECOV will set. At the same time, the data in the IICBUF will not be updated, and the newly received data will be lost. This status bit also requires software to clear, otherwise it will affect the subsequent communication. This kind of situation will only appear in IICRW=0. BF=1, and the CPU will appear when it does not read IICBUF.

### 9.3.5. IIC Send and Receive Data Buffer Register

IICBUFFER (E9H) IIC send and receive data buffer register

	Bit number	7	6	5	4	3	2	1	0
	Symbol	0	IICBUFFER					com	
	R/W	0.35			R/	W			mg. co
	Reset value	20.2		hen(0	16.3	)		hen(a	16:3
Z	7/20/10		, ·	ng. N	1.01		n'i	vs. V	
	- UNSIL PAID		V.	- 70			()		

(16 (2-4 1 2)		(10)	
ning: Model		ing: Mill	ning M. J.
Bit number	Bit symbol	JUDGO BY	Description
		IIC transmit and receive	ve data buffer register; when
7~0	IICBUFFER	clocks after the interrupt, as the data sent by the slave.  prepare IICBUFFER interrupt data before interrupt	
		generation.	

# 9.3.6. Interrupt Register

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	50en (4)	3	2	Devision 1/0/0.
Symbol	EX7	EX6 S	EX4	EX3	EX2 S	1118 02 0 1-0;
R/W	R/W	R/W	R/W	R/W	R/W	

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(1))6, '', '', '', '', '', '', ''	(1)	(,\)().5		
Reset value 0	o bento	0 0	bence of	10
0.150 =	105.			

Bit number	Bit symbol	Description
		IIC interrupt enable
3	EX3	1: IIC interrupt enable;
		0: IIC interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	_	IE4	IE3	IE2	_	-
R/W	R/W	R/W	_	R/W	R/W	R/W	_	-
Reset value	$\circ$ 0	0	_	0	0	0	_	- om

Bit number	Bit symbol	Description	1000 16:3
5-03	IE3	IIC interrupt flag  1: IIC interrupt flag is present; 0: IIC	interrupt flag is cleared

IPL1 (F6H) Interrupt priority register1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	_	IPL1.4	IPL1.3	IPL1.2	_	_
R/W	R/W	R/W	_	R/W	R/W	R/W	_	_
Reset value	0	0	_	0	0	0		-

Bit number	Bit symbol	Description	
3	IPL1.3	IIC interrupt priority bit  1: IIC interrupt is high priority;  0: IIC interrupt is low priority	:35
9.4. Seconda	ry Bus Register	2025-07-07-70.3	~

# 9.4. Secondary Bus Register

Secondary bus register						
Address	Name	RW	Reset	Description		
0x34	PERIPH_IO_SEL1	RW	0001_0000b	External port function selection register1		
0x50	IIC_FIL_MODE	RW	xxxx_xx10b	IIC filter selection register		

# 9.4.1. External Port Function Selection Register 1

PERIPH IO SEL1 (34H) External port function selection register 1

5	Bit number	7	2. per 67 11 1013	5	ng. berry
	Symbol	UART1_IO_SEL	UARTO_IO_SEL	, 5	IIC_IO_SEL
1	N Page 1		The D		

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	. 11 1.		' ( ) '	
R/W	R/W	ber/w 1	R/W	R/W/
Reset value	0 5	me of a large	0 5	me of O -or
Bit number	3	2 3	1	0 8
Symbol	INT3_IO_SEL	INT2_IO_SEL	INT1_IO_SEL	INTO_8_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
		IIC port selection enable
4	IIC_IO_SEL	0: Select IIC (SCL0B/SDA0B) function;
		1: Select IIC (SCL0A/SDA0A) function

# 9.4.2. IIC Filter Selection Register

IIC FIL MODE (50H) IIC filter selection register

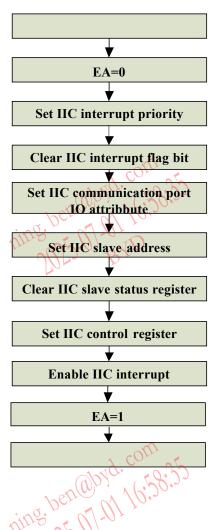
11-17	_ (= ===)			9+				
Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	1		_	_	IIC_AFIL_SEL	IIC_DFIL_SEL
R/W	_	_	-	_	_	_	R/W	R/W
Reset value	_	_	_	_	_	_	1	0

Bit number	Bit symbol	Description	
		IIC port analog filter selection enable	
1	IIC_AFIL_SEL	1: Select analog filter function;	
		0: Not select analog filter function;	
		IIC port digital filter selection enable	
0	IIC_DFIL_SEL	1: Digital filter function is selected;	
NY		0: Digital filter function is not selected;	

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# 9.5. IIC Configuration Process



IIC configuration flow chart

Note: The IIC bus pull-up resistor is 4.7k~10k, and the filter capacitor to the ground is recommended to be 10pF~100pF close to the pin chip.

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10. UART

There are 3 UART modules in the BF7515CM44-LJTX series. The BF7515CM44-LJTX provides the PERIPH\_IO\_SEL1 register. The Bit [6:5] of this register can control the selection of UART0 mapping IO port, and the Bit [7] of this register can control the selection of UART1 mapping IO port. Each module can only correspond to one set of mappings at the same time. Features of UART interface in the system:

- Support full-duplex, half-duplex serial
- Independent dual buffer receiver and single buffer transmitter
- Programmed baud rate (10bit analog-to digital divider Scalable to 12 digits)
- Interrupt-driven or polling operation:
  - send completed
  - receiving full
  - receive overflow, parity error, frame error
- Supports hardware parity production and check
- Programmable 8bit or 9bit character length
- STOP bit 1 or 2 can be selected
- Supports multiprocessor mode
- Support TXD/RXD pin position exchange
- Support TXD/RXD independent enable

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# 10.1. UART Function Description

### 10.1.1. Baud Rate Generation

The baud rate generation modulus Baud\_Mod is determined by the extension bit UART BD EXT.

UART\_BD\_EXT = 0, select the baud rate without expansion and maintain 10 bits:

Baud\_Mod = {UART BDH [1:0], UART BDL}.

UART BD EXT = 1, select the baud rate to extend to 12 bits:

Baud Mod = {UART BD ADD [1:0], UART BDH[1:0], UART BDL}.

Baud\_rate calculation formula: When Baud\_Mod=0, the baud rate clock is not generated, when Baud\_Mod>1, the baud rate = BUSCLK/(16xBaud\_Mod). BUSCLK uses the frequency division clock of System clock source and is fixed at 24M. Each time the baud rate register is configured, the internal counter will be cleared to regenerate the baud rate signal. Communication requires that the transmitter and receiver use the same baud rate. The allowable baud rate deviation range for communication: 8/(11\*16)=4.5%.

### 10.1.2. Transmitter Function

Send data flow: Trammitted by writing UART\_BUF data, sending stop bit after sending stop bit. Software clear interrupt flag and waits for the next write. The transmitter output pin (TXD) idle state defaults to a logic high state. The entire transmission process must be performed when the module is enabled.

By writing data into the data register (UART\_BUF), the data will be directly saved to the sending data buffer and the sending process will be started. In the subsequent complete sending process, the data buffer is locked, and the configuration write data register is invalid until the sending is completed after the stop bit, write UART BUF again to restart a new transmission.

The central element of the serial port transmitter is the transmit shift register with a length of 10/11/12 bits (depending on the setting in the DATA\_MODE control bit). Assuming

DATA\_MODE=0, select the normal 8-bit data mode. In 8-bit data mode, there are 1 start bit, 8 data bits, and 1/2 stop bits in the shift register.

Both sending and receiving are in little-endian mode (LSB first).

### 10.1.3. Receiver Function

The receiver is enabled by setting the RECEIVE\_ENABLE bit in UART\_CON1. Of course, the entire receiving process must be performed when the module is enabled.

Receiving data flow: When the receiving enable is valid, the data is received at any time, the receiving interrupt is set after receiving the stop bit, and the software clears the interrupt flag.

The currently received data will have a detection mechanism, which can detect three types of errors: receiving overflow, frame error, and parity error, all of which require software to clear the

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flag. It is recommended that after detecting the receiving interrupt, read the status flag, read the data buf, and finally clear the received data status flag (UART\_STATE[3:0]).

The data character is composed of a logic 0 start bit, 8 (or 9) data bits (LSB first) and a logic 1 stop bit (1bit). After receiving the stop bit into the receiving shifter, if the receiving data register is not full, the data character is transferred to the receiving data register, and the receiving data register is full status flag is set. If the receiving data register has been set to be full at this time, the overflow status flag is set, and the new data will be lost. Because the receiver is double-buffered, the program has a full character time for reading after setting the receive data register is full and before reading the data in the receive data buffer to avoid receiver overflow. When the program detects that the receive data register is full, it obtains data from the receive data register by reading UART BUF.

### 10.1.4. Receiver Sampling Method

The receiver uses a 16 times baud rate clock for sampling. The receiver searches for the falling edge on the RXD serial data input pin by extracting logic level samples at 16 times the baud rate. The falling edge is defined as logic 0 samples after 3 consecutive logic 1 samples. The 16 times baud rate clock is used to divide the bit time into 16 segments, which are labeled RT1 to RT16.

The receiver then samples each bit time of RT8, RT9 and RT10, including the start bit and stop bit, to determine the logic level of the bit. The logic level is the logic level of the vast majority of samples taken during the bit time. When the falling edge is positioned, the logic level is 0 to ensure that this is the real start bit, not noise. If at least two of these three samples are 0, the receiver assumes that it is synchronized with the receiver character and starts Shift receives the following data, if the above conditions are not met, exit the state machine and return to the state of waiting for the falling edge.

The falling edge detection logic keeps looking for a falling edge. If an edge is detected, the sample clock resynchronizes the bit time. In this way, when noise or baud rate is not matched, the reliability of the receiver can be improved.

### 10.1.5. Multiprocessor Mode

In multi-processor mode, it only works in 9-bit mode. When the received R8 bit=1, the receive interrupt is set, otherwise it is not set. The function of this mechanism is to use hardware detection to eliminate the software overhead of processing unimportant information characters. Allow receivers to ignore characters in messages used for different receivers.

In this application system, all receivers estimate the Address character (bit 9 = 1) of each message. Once it is determined that the information is intended for different receivers, subsequent data characters (bit 9 = 0) will not be received.

Configuration process: Configure receiving enable, configure multiprocessor mode, receive Address data (the 9th bit = 1), receive and generate an interrupt, the application confirms whether the Address matches, if it matches, the configuration closes the multiprocessor mode, and all subsequent data (The 9th bit = 0) can be received and interrupted, until the next Address data is

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received, the Address does not match, then the multi-processor mode is turned on, then all subsequent data will not be received, until the next Address data, in turn, loop application.

# 10.2. UART Related Register

	SFR register								
Address	Name	RW	Reset	Description					
0x98	UART2_STATE	R/RW	x000_0000b	UART2 status flag register					
0xBA	UART2_BDL	RW	0000_0000b	UART2 baud rate control register					
0xBB	UART2_CON1	RW	x000_0000b	UART2 mode control register 1					
0xBC	UART_IO_CTRL1	RW	xx00_0000b	UART pin enable register					
0xBD	UART2_BUF	RW	1111_111b	UART2 port data register					
0xC2	UART_IO_CTRL	RW	xxxx_x000b	UART TXD/RXD pin exchange register					
0xD6	UART1_BDL	RW	0000_0000b	UART1 baud rate control register					
0xD7	UART1_CON1	RW	x000_0000b	UART1 mode control register 1					
0xD9	UART1_CON2	RW	xx00_1100b	UART1 mode control register 2					
0xDA	UART1_STATE	RW	x000_0000b	UART1 status flag register					
0xDB	UART1_BUF	RW	1111_111b	UART1 port data register					
0xDC	UART0_BDL	RW	0000_0000b	UART0 baud rate control register					
0xDD	UART0_CON1	RW	x000_0000b	UART0 mode control register 1					
0xDE	UART0_CON2	RW	xx00_1100b	UART0 mode control register 2					
0xDF	UARTO_STATE	RW	x000_0000b	UART0 status flag register					
0xE1	IRCON2	RW	0000_0000b	Interrupt flag register 2					
0xE2	UART0_BUF	RW	1111_1111b	UART0 port data register					
0xE7	IEN2	RW	0000_0000b	Interrupt enable register 2					
0xED	UART2_CON2	RW	xx00_1100b	UART2 mode control register 2					
0xF4	IPL2	RW	0000_0000b	Interrupt priority register2					

UART SFR register list

	Secondary bus register							
Address	Name	RW	Reset	Description				
0x34	PERIPH_IO_SEL1	RW	0001_0000b	External port function selection register 1				
0x67	UART_BD_EXT	RW	xxxx_xxx0b	UART0/1/2 baud rate configuration extension bit register				

UART secondary bus register list

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# 10.3. UARTO Register

# 10.3.1. UARTO Status Flag Register

UARTO STATE (DFH) UARTO status flag register

Bit number	7	6	5	4
Symbol	_	UART0_R8	UART0_T8	TI0
R/W	_	R	R/W	R/W
Reset value	_	0	0	0
Bit number	3	2	1	0
Symbol	NIO RIO	UARTO_RO	UART0_F	UARTO_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	1000	0	1000

Bit number	Bit symbol	Description Description							
7		Reserved							
6	UART0_R8	The 9th data of the receiver, read only							
5	UART0_T8	The 9th data of the transmitter, read only when parity check is enabled							
		Send interrupt mark:							
4	TI0	1: The sending buffer is empty							
7	110	0: Send buffer is full, software write 0 to clear, write 1 is invalid							
		Receive interrupt mark:							
3	RI0	1: The receive buffer is full							
RND		0: The receive buffer is empty, software writes 0 to clear, writes 1 is invalid							
V	UART0_RO	Receive overflow flag:							
2		1: Receive overflow (new data is lost)							
		0: no overflow, software write 0 to clear, write 1 is invalid							
		Frame error flag:							
1	UART0_F	1: Frame error detected							
1		0: No frame error is detected, software writes 0 to clear, write 1 is invalid							
	UARTO P	Parity error flag:							
0		1: Receiver parity error							
U	0/MC10_1	0: The parity check is correct, the software writes 0 to clear and writes 1 is invalid							

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# 10.3.2. UARTO Baud Rate Control Register

7, 60,	05				20	BF/3	013CM4	4-LJ 1 2	<u> </u>
10.3.2. UARTO Baud Rate Control Register								10/10	38:
UARTO BDL (	(DCH) UART0 baud rate control register					2022-01			
Bit number	7	6	5	2	1	0			
Symbol	UART0_BDL[7:0]								
R/W	R/W								
Reset value	0								

Bit number	Bit symbol	Description
7~0	UART0_BDL[7:0]	Baud rate control register, the lower 8 bits of the baud rate modulus divisor register  UART_BD_EXT=0,  Baud_Mod = {UART0_BDH[1:0], UART0_BDL};  UART_BD_EXT=1,  Baud_Mod= {UART0_BD_ADD[1:0], UART0_BDH[1:0],  UART0_BDL};  When Baud_Mod=0, the baud rate clock is not generated;  When Baud_Mod>1,  baud rate = BUSCLK/(16xBaud Mod)

UART0 CON2 (DEH) UART0 mode control register 2

Bit number	7	6	5	4	3	2	1	0	
Symbol	_	_	UART0_l	BD_ADD	TX_EMPTY_IE	RX_FULL_IE	UART0_BDH		
R/W	~	_	R/W	R/W	R/V	V	R/	W .	
Reset value	$\overline{U}_I$	2	0	0	A CPINI	1	0	7 00 W	

	70.	(0)					
Bit number	Bit symbol	Description better 11 10.					
25-5~48	UART0_BD_ADD	The upper 2 bits ofthe baud rate modulus divisor register (it is determined by UART_BD_EXT whether to take effect)					
		Send interrupt enable					
3	TX_EMPTY_IE	1: Interrupt enable;					
		0: Interrupt disable (used in polling mode)					
		Receive interrupt enable					
2	RX_FULL_IE	1: Interrupt enable;					
		0: Interrupt disable (used in polling mode)					
1~0	UART0_BDH	The upper 2 bits ofthe baud rate modulus divisor register					

# 10.3.3. UARTO Mode Control Register 1

UARTO CON1 (DDH) UARTO mode control register 1

0	Bit number	7	Jun of	(6)	BY	5	7	1	72-1	4 6	NV	
1	) •			Nº				N				

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	1 10 -		T	
Symbol		UART0_ENABLE	RECEIVE_ENABLE	MULTI_MODE
R/W	_	R/W	R/W	R/W
Reset value	_	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
		Module enable
6	UART0_ENABLE	1: Module enable;
		0: Module close
		Receiver enable
5	RECEIVE_ENABLE	1: Receiver is on;
		0: Receiver is off
		Multi-processor communication mode
4	MULTI_MODE	1: Mode enable;
		0: Mode disable
		Stop bit width selection
3	STOP_MODE	1: 2 bits;
		0: 1 bit
		Data mode selection
2	DATA_MODE	1: 9-bit mode;
		0: 8-bit mode
		Parity check enable  1: Parity check is enabled;  0: Parity check is disabled  Parity check selection
1	PARITY_EN	1: Parity check is enabled;
		0: Parity check is disabled
		Parity check selection
0	PARITY_SEL	1: Odd check;
		0: Even check

# 10.3.4. UARTO Port Data Register

UARTO BUF (E2H) UARTO port data register

	Bit number	7	6	5	4.00	3	2	1	0,00	
	Symbol	0.35			myd. Co	ch.2			ord. Co.	0
	R/W 16	20.2		bence	R	W		pen(0)	5, 16:50	)
Ę	Reset value		· · ·	128. 1	$\Gamma$	F	rin	vs. " V.	17/1	
(	OSS-O. PIR		<b>V</b>	1000	3 '			1052-0	,	

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	7()0-		
Bit number	Bit symbol	Description	pena W 10.3
7~0		Read returns the contents of the read-of buffer, write into the write-only transf	- ^\\\

### 10.3.5. UARTO Pin Enable Register

UART IO CTRL1 (BCH) UART pin enable register

	Er (Berr) er ner pr			
Bit number	7	6	5	4
Symbol	-	-	UART2_RXD_ DIASB	UART2_TXD_ DIASB
R/W	_		R/W	R/W
Reset value	0	0 7 con	0	0 7 . COL
Bit number	3	200	1	000
Symbol	UART1_RXD_	UARTI TXD_	UART0_RXD_	UARTO_TXD_
Synthoon	DIASB	DIASB	DIASB	DIASB
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Bit symbol Description			
		UART0 RXD port disabled			
1	UART0_RXD_DIASB	0: RXD pin is enabled;			
		1: RXD pin is disabled			
		UART0 TXD port disable			
0	UART0_TXD_DIASB	0: TXD pin is enabled;			
		1: TXD pin is disabled			

# 10.3.6. UARTO TXD/RXD Pin Exchange

UART\_IO\_CTRL (C2H) UART TXD/RXD pin exchange register

Bit number	7~3	2	1	0
Symbol	_	UART2_PAD_CHANGE	UART1_PAD_CHANGE	UART0_PAD_CHANGE
R/W	_	R/W	R/W	R/W
Reset value	_	0	0	0

Bit number	Bit symbol	Description
		UART0 TXD/RXD pin exchange
0	UARTO_PAD_CHANGE	1: Pin exchange;
		0: Pin not exchange

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# 10.4. UART1 Register

# 10.4.1. UART1 Status Flag Register

UART1 STATE (DAH) UART1 status flag register

Bit number	7	6	5	4
Symbol	_	UART1_R8	UART1_T8	TI1
R/W	_	R	R/W	R/W
Reset value	_	0	0	0
Bit number	3	2	1	0
Symbol	N RI1	UART1_RO	UART1_F	UART1_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	262000	0	160 0 160

		108 1108						
Bit number	Bit symbol	Description Description						
6	UART1_R8	Reserved						
5	UART1_T8	The 9th data of the receiver, read only						
4	TI1	The 9th data of the transmitter, read only when parity check is enabled						
3	RI1	Send interrupt mark: 1: The sending buffer is empty;						
3	ΝΠ	0: Send buffer is full, software write 0 to clear, write 1 is invalid						
		Receive interrupt mark						
2	UART1 RO	1: The receive buffer is full;						
	UARTI_RO	0: The receive buffer is empty, software writes 0 to clear, writes 1 is invalid						
<b>y</b>		Receive overflow flag						
1	UART1_F	1: Receive overflow (new data is lost);						
		0: No overflow, software write 0 to clear, write 1 is invalid						
		Frame error flag						
	UART1_P	1: Frame error detected;						
0		0: No frame error is detected, software writes 0 to clear, write 1 is invalid						

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# 10.4.2 UART1 Baud Rate Control Register

### UART1\_BDL (D6H) UART1 baud rate control register

7 60,	06				20	<b>BF</b> 75	515CM4	4-LJTX
<b>10.4.2 UART</b> UART1 BDL (1			205-	1/-0,	2:22		2025-0	10116.5
Bit number	7	6	5	4	3	2	1	0
Symbol				UART1_	BDL[7:0]			
R/W		R/W						
Reset value				(	0			

Bit number	Bit symbol	Description
7~0	UART1_BDL[7:0]	Baud rate control register, the lower 8 bits of the baud rate modulus divisor register  UART_BD_EXT=0,  Baud_Mod = {UART1_BDH[1:0], UART1_BDL};  UART_BD_EXT=1,  Baud_Mod= {UART1_BD_ADD[1:0], UART1_BDH[1:0],  UART1_BDL};  When Baud_Mod=0, the baud rate clock is not generated;  when Baud_Mod>1,  baud rate = BUSCLK/(16xBaud Mod)

### UART1 CON2 (D9H) UART1 mode control register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	UART1_	BD_ADD	TX_EMPTY_IE	RX_FULL_IE	UART	1_BDH
R/W	-	_	R/W	R/W	R/W	R/W	R/	W
Reset value	77	-	0	0	1 cdy, 02	1	0	<sup>7</sup> 00,000

	(0,0)	70.2	(0b), $(0b)$ , $(0b)$
σ	Bit number	Bit symbol	Description Description
70	05-08/0	UART1_BD_ADD	The upper 2 bits of the baud rate modulus divisor register (It is determined by UART_BD_EXT whether to take effect)
	3	TX_EMPTY_IE	Send interrupt enable  1: Interrupt enable;  0: Interrupt disable (used in polling mode)
	2	RX_FULL_IE	Receive interrupt enable  1: Interrupt enable;  0: Interrupt disable (used in polling mode)
	1~0	UART1 BDH	The upper 2 bits of the baud rate modulus divisor register



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# 10.4.3. UART1 Mode Control Register 1

7.00			DI / J	IJCM44-LJIA
30501-01	<b>F1 Mode Cont</b> (D7H) UART1 m	rol Register 1	6:28:33	2025-01-10-58
Bit number	7	6	5	4
Symbol	_	UART1_ENABLE	RECEIVE_ENABLE	MULTI_MODE
R/W	_	R/W	R/W	R/W
Reset value	_	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

	STONE.	20.33	1010. 1010	
Bi	it number	Bit symbol	Description Description	16:20
305	2-6	UART1_ENABLE	Module enable 1: Module enable; 0: Module close	1 10.
	5	RECEIVE_ENABLE	Receiver enable 1: Receiver is on; 0: Receiver is off	
	4	MULTI_MODE	Multi-processor communication mode  1: Mode enable;  0: Mode disable	
	3	STOP_MODE	Stop bit width selection; 1: 2 bits; 0: 1 bit	155
	28/	DATA_MODE	Data mode selection 1: 9-bit mode; 0: 8-bit mode	10.
	1	PARITY_EN	Parity check enable  1: Parity check is enabled;  0: Parity check is disabled	
	0	PARITY_SEL	Parity check selection 1: Odd check; 0: Even check	

# 10.4.4 UART1 Port Data Register

UART1\_BUF (DBH) UART1 port data register

Bit number	7	6	(5) 2-1 84	3	2	0
No.						

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(0)	
Symbol	<u>-</u>
RW	R/W
Reset value	FF

Bit number	Bit symbol	Description
7~0		Read returns the contents of the read-only receive data buffer, write into the write-only transmit data buffer

### 10.4.5. UART1 Pin Enable Register

UART IO CTRL1 (BCH) UART pin enable register

011111_10_017	er (berr) erner pr	11 0114010 10515101		~ \
Bit number	7	6 7.00	5	4 7. 001
Symbol	26.33	1000	UART2_RXD_	UARTO TXD
Syllidoi	- ,	25. DC, 21 11 10	DIASB	O. DIASB
R/W	<u>-</u>	005-01	R/W	RW
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	UART1_RXD_	UART1_TXD_	UARTO_RXD_	UART0_TXD_
- J	DIASB	DIASB	DIASB	DIASB
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
2.00		UART2 RXD port disabled
2032/01	UART2_RXD_DIASB	0: RXD pin is enabled;
berro	0	V. RXD pin is disabled
e Bill	nitie	UART2 TXD port disable
4	UART2_TXD_DIASB	0: TXD pin is enabled;
		1: TXD pin is disabled
		UART1 RXD port disabled
3	UART1_RXD_DIASB	0: RXD pin is enabled;
		1: RXD pin is disabled
		UART1 TXD port disable
2	UART1_TXD_DIASB	0: TXD pin is enabled;
		1: TXD pin is disabled

# 10.4.6. UART1 TXD/RXD Pin Exchange

UART\_IQ\_CTRL (C2H) UART TXD/RXD pin exchange register

1	Bit number 7~3	2 1	11 00 00 BY
- T			

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Symbol	UART2_PAD_CHANGE	UART1_PAD_CHANGE	UARTO_PAD_CHANGE
R/W _	R/W	R/W	R/W
Reset value _	0	0	0

Bit num	ber	Bit symbol	Description
			UART1 TXD/RXD pin exchange
1		UART1_PAD_CHANGE	1: Pin exchange;
			0: Pin not exchange

# 10.5. UART2 Register

# 10.5.1. UART2 Status Flag Register

	10.5. UAK1					
	1 0000	<b>T2 Status Flag R</b> E (98H) UART2 stat	1 6000 1 16	28:35	ing ben abyd. com	6.55
Mine	Bit number	7	Mison 561 BYD	5	Mison 4 BYD	
	Symbol	-	UART2_R8	UART2_T8	TI2	
	R/W	_	R	R/W	R/W	
	Reset value	_	0	0	0	
	Bit number	3	2	1	0	
	Symbol	RI2	UART2_RO	UART2_F	UART2_P	
	R/W	R/W	R/W	R/W	R/W	
	Reset value	0	0	0	0	

Bit number	Bit symbol	Description COTT		
(1)6 y (1)	UART2_R8	The 9th data of the receiver, read only		
ben 5 pt	UART2_T8	The 9th data of the transmitter, read only when parity check is enabled		
		Send interrupt mark:		
4	TI2	1: The sending buffer is empty		
4	112	0: Send buffer is full, software write 0 to clear, write 1 is invalid		
		Receive interrupt mark		
3	RI2	1: The receive buffer is full		
3	KIZ	0: The receive buffer is empty, software writes 0 to clear, writes 1 is invalid		
		Receive overflow flag		
2	HADTO DO	1: Receive overflow (new data is lost)		
2	UART2_RO	0: No overflow, software write 0 to clear, write 1 is invalid		
1	UART2_F	Frame error flag		

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	0	58.33	
3	pena Will	,50	1: Frame error detected
PC	025-01-0		0: No frame error is detected, software writes 0 to clear, write 1 is invalid
			Parity error flag
	0	UART2_P	1: Receiver parity error
	U		0: The parity check is correct, the software writes 0 to clear, and writes 1 is invalid

### 10.5.2. UART2 Baud Rate Control Register

UART2\_BDL (BAH) UART2 baud rate control register

Bit number 7	6	5	4000	2	1	19°00/11
Symbol		<b>(</b> 0	UART2_BDL[7:0]			0/01/2
R/W		20. Perio	R/W	• ,	o perio	11/100
Reset value	77	7.502	0	77	1.5002	

Bit number	Bit symbol	Description
		Baud rate control register, the lower 8 bits ofthe baud rate modulus divisor register UART_BD_EXT=0,
		Baud_Mod = {UART2_BDH[1:0], UART2_BDL};
		UART_BD_EXT=1,
7~0	UART2_BDL[7:0]	Baud_Mod= {UART2_BD_ADD[1:0], UART2_BDH[1:0],
		UART2_BDL};
1 co <sup>x</sup>		When Baud Mod 0, the baud rate clock is not generated;
abyd.	8:70	when Baud_Mod>1,
pen 0170	,5	the band rate = BUSCLK/(16xBand_Mod)

UART2 CON2 (EDH) UART2 mode control register 2

Bit number	7	6	5	#17.2	B 3	2	1	Bo
Symbol	_	_	UART2_	BD_ADD	TX_EMPTY_IE	RX_FULL_IE	UAR	Γ2_BDH
R/W	_	_	R/W	R/W	R/W	R/W	F	R/W
Reset value	_	_	0	0	1	1	0	0

Bit number	Bit symbol	Description		
5~4	UART2_BD_ADD	The upper 2 bits ofthe baud rate modulus divisor register (It is determined by UART_BD_EXT whether to take effect)		
		Send interrupt enable		
3	TX_EMPTY_IE	1: Interrupt enable;		
		0: Interrupt disable (used in polling mode)		
Over	RX_FULL_IE	Receive interrupt enable		
2		1: Interrupt enable;		

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(0)	70.0	
pener W 10		0: Interrupt disable (used in polling mode)
0-1-0	UART2_BDH	The upper 2 bits of the baud rate modulus divisor register

### 10.5.3. UART2 Mode Control Register 1

UART2\_CON1 (BBH) UART2 mode control register 1

Bit number	7	6	5	4
Symbol	_	UART2_ENABLE	RECEIVE_ENABLE	MULTI_MODE
R/W	_	R/W	R/W	R/W
Reset value	_	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY SEL
R/W	R/W	R/W <sup>()</sup>	R/W	R/W
Reset value	0	10g. 00 101	0	08. pc. 10 11 10.

W. J. By		of the Barrell of the
Bit number	Bit symbol	Description
6	UART2_ENABLE	Module enable 1: Module enable, 0: Module close
5	RECEIVE_ENABLE	Receiver enable 1: Receiver is on, 0: Receiver is off
4	MULTI_MODE	Multi-processor communication mode  1: Mode enable, 0: Mode disable
3	STOP_MODE	Stop bit width selection 1: 2 bits, 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode, 0: 8-bit mode
18/1	PARITY_EN	Parity check enable  1: Parity check is enabled, 0: Parity check is disabled
0	PARITY_SEL	Parity check selection 1: Odd check, 0: Even check

### 10.5.4 UART2 Port Data Register

UART2 BUF (BDH) UART2 port data register

Bit number	7	6	5	4 📉	3	2	1	0
Symbol				UART2_1	BUF[7:0]		$\sim$ 1	ord. cor
R/W			1-01/0	R/	W		1-00	707
Reset value			vis.	F	F	ais.	vā:	

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	· 1/1/0-		$(11)^{12}$
Bit number	Bit symbol	Description	bento 1/0.2
7~0		UART2 data register  Read returns the contents ofthe read- buffer, write into the write-only trans	•

### 10.5.5. UART2 Pin Enable Register

UART IO CTRL1 (BCH) UART Pin enable register

	Er (Berr) erner in				
Bit number	7	6	5	4	
Symbol	_	<u>-</u>	UART2_RXD_ DIASB	UART2_TXD_ DIASB R/W	
R/W	-	= 17° CO1	R/W		
Reset value	0	000	0		
Bit number	3	ng. ber 2/ 1/1/10	1	5. per 0 1/10.	
Symbol	UART1_RXD_ ODIASB	UARTI_TXD_ DIASB	UART0_RXD_ <sup>(V)</sup> DIASB	DARTO_TXD_ DIASB	
R/W	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	

Bit number	Bit symbol	Description	
		UART2 RXD port disabled	
5	UART2_RXD_DIASB	0: RXD pin is enabled;	
		1: RXD pin is disabled	
		UART2 TXD port disable	
4	UART2_TXD_DIASB	0: TXD pin is enabled;	
		1: TXD pin is disabled	

### 10.5.6. UART2 TXD/RXD Pin Exchange

UART IO CTRL (C2H) UART TXD/RXD pin exchange register

		/		
Bit number	7~3	2	1	0
Symbol	_	UART2_PAD_CHANGE	UART1_PAD_CHANGE	UARTO_PAD_CHANGE
R/W	_	R/W	R/W	R/W
Reset value	_	0	0	0

Bit number	Bit symbol	Description	7
abyd. C	O <sup>r</sup>	UART2 TXD/RXD pin exchange	
(2) )	UART2_PAD_CHANGE	1: Pin exchange;	
5.00	ing	0: Pin not exchange	

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# 10.6. UART Interrupt Register

# 10.6.1. Interrupt Flag Register 2

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	IE15	IE14	IE13	IE12	IE11	IE10	IE9	IE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description	an
ben obyd. co,	IE11	UART1 interrupt flag 1: UART1 interrupt flag 0: Clear UART1 interrupt flag	ing ben @byd. co.
2	IE10	UART0 interrupt flag 1: UART0 interrupt flag 0: Clear UART0 interrupt flag	702-11
0	IE8	UART2 interrupt flag 1:UART2 interrupt flag 0: Clear LVDT interrupt flag	

### 10.6.2. Interrupt Enable Register 2

IEN2 (E7H) Interrupt enable register 2

Bit number	5:33	6	5	30/4	2.33	2	1	5400 CO
Symbol	EX15	EX14	EX13	EX120	EX11	EX10	EX9	EX8
R/W	R/W	R/W	M. R.W.	R/W	R/W	R/W	MR/W	R/W
Reset value	0	0	18/17.	0	0	0	16/13-	0

Bit number	Bit symbol	Description
		UART1 interrupt enable
3	EX11	1: UART1 interrupt enable;
		0: UART1 interrupt disable
		UART0 interrupt enable
2	EX10	1: UART0 enable;
		0: UART0 disable
		UART2 interrupt enable
0	EX8	1: UART2 interrupt enable;
		0: UART2 interrupt disable

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	7,00	25	25	BF/3	13CM4	4-LJ I X	2			
10.6.3. Interrupt Priority Register2  IPL2 (F4H) Interrupt priority register2							2025-07	01/16.5	5	
	Bit number	7	6	5	4	3	2	1	0	
	Symbol	IPL2.7	IPL2.6	IPL2.5	IPL2.4	IPL2.3	IPL2.2	IPL2.1	IPL2.0	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	Reset value	0	0	0	0	0	0	0	0	

Bit number	Bit symbol	Description	
		UART1 priority selection bit.	
3	IPL2.3	1: UART1 interrupt is high priority;	
		0: UART1 interrupt is low priority	-0
		UART0 priority selection bit.	
2	IPL2.2	1: UART0 interrupt is high priority;	. 47 11 10.
		0: UART0 interrupt is low priority	0020
		UART2 priority selection bit.	Mrs
0	IPL2.0	1: UART2 interrupt is high priority;	
		0: UART2 interrupt is low priority	

# 10.7. Secondary Bus Register

### 10.7.1. External Port Function Selection Register 1

PERIPH IO SEL1 (34H) External port function selection register 1

Bit number	29.35 7	6byd.	6)04d. (28.3) 5			
Symbol	UART1_IO_SEL	UARTO_	IO_SEL	HC_10_SEL///		
R/W	R/W	INS R/W	R/W	ing RW		
Reset value	0	0	0			
Bit number	3	2	1	0		
Symbol	Symbol INT3 IO SEL		INT1_IO_SEL	INTO_8_IO_SEL		
R/W	R/W R/W		R/W	R/W		
Reset value	0	0	0	0		

Bit number	Bit symbol	Description
7	UART1_IO_SEL	UART1 port selection enable
		0: Select UART1 (RXD1B/TXD1B) function;
		1: Select UART1 (RXD1A/TXD1A) function
6~5	UART0_IO_SEL	UART0 port selection enable
Ova		00: Select UART0 (RXD0C/TXD0C) function;
RID		01: Select UART0 (RXD0A/TXD0A) function;

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1x: Select UART0 (RXD0B/TXD0B) function

### 10.7.2. UART0/1/2 Baud Rate Configuration Extension Bit Register

UART BD EXT (67H) UART0/1/2 Baud rate configuration extension bit register

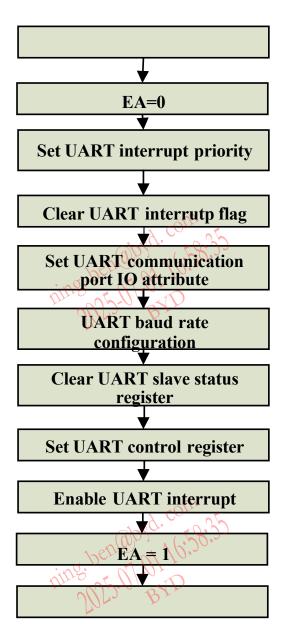
Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	_	_
R/W	_	_	_	_	_	_	_	R/W
Reset value	_	_	_	_	_	_	_	0

Bit number	Bit symbol	Description
ben @Byd. co		UART0/1/2 baud rate configuration extension bit selection  1: Select the baud rate to extend to 12 bits;  0: Select the baud rate without extension to maintain 10 bits
	ζ.	Mr. S. Miles

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### 10.8. UART Configure Process



UART initial configure process

### Recommended application process:

- 1. Configuration module enable, receive enable, mode select: UART CON1;
- 2. Configure baudrate, open interrupt enable: UART BDL, UART CON2;
- 3. Write UART\_BUF to start sending data. After detecting the sending interrupt, clear the interrupt flag TI. Once the sending process is completed, wait for the next write to UART\_BUF to start the sending process (it is not allowed to configure the next data in the sending process, including UART\_BUF and UART\_T8);
- 4. When the receiving interrupt is detected, first read the receiving status UART\_STATE, then read R8 and UART\_BUF, and finally clear the receiving status flag (UART\_STAT [3:0] =

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B0000). Once the receiving process is completed, wait for the next receiving interrupt.

- 5. If the configuration interrupt is not enabled and the program executes the UART function, it also needs to read the status flag first, then read R8 and UART\_BUF, and finally clear the status flag.
- 6. Interrupt flag bit clearing operation. In full-duplex operation, the clear flag bit operation requires writing 0 for the effective interrupt bit and writing 1 for other interrupt bits (writing 1 is an invalid operation), otherwise it is easy to misuse. For example: when the transmission interrupt is valid, you need to write UART0\_STATE = 0x0F; (that is, configure UART0\_STATE 0:3] = 0x0F, and write R8 is invalid. When t8 is in 9-bit mode and no parity, you need to configure valid transmission data).
- 7. 8-bit mode: the parity check is disabled.
  9-bit mode: When the parity bit is enabled, when the ninth bit is not enabled, the ninth bit is UART\_T8written in. There are only sending and receiving interrupts. The error flag only marks the error detection of the current data, and only the corresponding bit is cleared by writing 0. There is no error interrupt. The sending interrupt is set to 1 after the stop bit is sent, and the software is cleared to 0. The receiving interrupt is receiving Set to 1 after the stop bit is completed, cleared by software.

Multi-processor mode: only work in 9-bit mode, when the received R8 bit = 1, the receive interrupt is set, otherwise it is not set. When using the multi-processor mode, configure the receive enable, configure the multi-processor mode, receive the address data (the 9th bit = 1), receive and generate an interrupt, the application confirms whether the address matches, and the configuration closes the multi-processor mode if it matches. Data (the 9th bit = 0) can be interrupted by the receive interrupt until the next address data is received. If the address does not match, the multi-processor mode is turned on, and all subsequent data will not be received until the next address data is cycled in turn application.

Hardware response: Send data, start by writing UART\_BUF value, set the sending interrupt flag after sending the stop bit, and clear the interrupt flag by software, and wait for the next write. When the receiving data is enabled, the data can be received at any time. After receiving the stop bit, the receiving interrupt is set and the software clears the interrupt flag. The currently received data will have a detection mechanism, which can detect three types of errors: receiving overflow, frame error, and parity error, all of which require software to clear the flag. It is recommended that after detecting the receiving interrupt, read the status flag and clear all the receiving status flags UARTO/1\_STATE [0:3].

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ning, ben abyd com
1/h=1/125-07-01 16:58 SPI is a serial, synchronous, full/half duplex communication bus, the communication clock is 12MHz/8 MHz /4 MHz /1 MHz optional, the highest support 2MHz (master, slave) communication, the communication mode supports normal mode and high-speed mode. Four modes of clock idle level are selectable, SPI clock ratio is 50% (10% deviation allowed).

SPI normal mode: MCU writes SPI transmission buffer SPID through interrupt (when SPI enable is turned on, immediately generates a sending empty interrupt) or polling, the data is automatically loaded into the shift register, and sent to SPI MOSI synchronously via SCLK; SPI MISO receives data and loads it into the SPI receive buffer. When a receiving full interrupt is generated, the received data can be read from SPID.

SPI high-speed mode: MCU sends to SRAM to write and send data (up to 4K can be written). During communication, SPI reads the data to be sent directly from SRAM without interruption or polling; at the same time, every time a piece of data is received (8Bits), write the corresponding address of SRAM immediately. When the communication is completed, SPI generates a sending empty sign and a receiving full sign at the same time, and sends an interrupt. Four modes of SFR configuration:

CPOL: Select clock idle state level:

0: The idle state of the clock is low;

1: Clock idle state is high level.

CPHA: Select the data moment of each cycle.

0: Data sampling is performed on the first transition edge (rising or falling edge) of the clock:

1: Data sampling is performed on the second transition edge (rising or falling edge) of the clock;

Mode 0 (CPOL=0, CPHA=0): The idle level of the clock is low, and the master and slave sample the data on the rising edge.

Mode 1 (CPOL=0, CPHA=1): The idle level of the clock is low, and the master and slave sample the data on the rising edge.

Mode 2 (CPOL=1, CPHA=0): The idle level of the clock is high, and the master and slave will sample the data on the rising edge.

Mode 3 (CPOL=1, CPHA=1): The clock idle level is high, and the master and slave machines sample data on the rising edge.

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Clock signal SPI\_CLK(CPOL=0) Polarity 0 SPI\_CLK(CPOL=1) Polarity 1 Slave selection Clock phase is 0 CPHA=0 Clock leading edge Cycle # CPHA=0 data sampling b Cl ock back MOSI(CPHA=0) Xbit6 bit7 bit8 bit5 Data output on the back edge of the X bit3 bit7\bit8 Xb it1 (bit2 bit5 Xbit6 MISO(CPHA=0) clock Clock phase is 1 CPHA=1 Clock leading edge Cl ock l eadi ng X 6 Cycle # CPHA=1 data output MOSI(CPHA=1) \bit6 Data sampling on the back edge of the bit7 bit8 bit2 bit3 bit4 bit5 bit6 clock

SPI working mode timing diagram

Description: SI: Slave sampling data; SO: Slave sending data; MI: Host sampling data; MO: Host sending data. PI\_CS high level minimum time requirement is 1 SPI clock cycle.

### 11.1. SPI Port Configuration

To use the SPI function, you need to configure the relevant port as an SPI channel, and select the corresponding port input through the SPI communication port selection register. For example, configure PC0, PC1, PC2, and PC3 as SPI communication ports. Configure SPI\_IO\_SEL = 0x01:

SPI0B CS: SPI chip select signal

SPI0B CLK: SPI clock

SPI0B\_MOSI: SPI master data output SPI0B\_MISO: SPI master data input

SPI IO SEL (68H) SPI communication port selection register

DIPLO DEL (U	of 10 SEL (0011) St I communication port selection register							
Bit number	7	6	5	4	3	2	1	0
Symbol	_	-	_	_	_	_	SPI_IO_	SEL[1:0]
R/W	_		_	_	_	_	R/W	R/W
Reset value	_	_	_	_	_	_	0	0

Bit number	Bit symbol	Description
		SPI communication port selection register
1.0	SPI_IO_SEL[1:0]	01: PC2/3/4/5 selects SPI function
1~0		10: PE4/5/6/7 selects SPI function
		00/11: PG0/1/2/3 selects SPI function

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# 11.2. SPI Related Registers

Mrs Br			SFR register	J. 3 By
Address	Name	RW	Reset	Description
0xB5	SPI_CFG1	RW	0001_0101b	SPI configuration register1
0xB6	SPI_CFG2	RW	x001_1000b	SPI configuration register2
0xBE	SPI_STATE	RW	xxxx_x001b	SPI status register
0xBF	SPI_SPID	RW	0000_0000b	SPI cache operation register
0xE1	IRCON2	RW	0000_0000Ь	Interrupt flag register 2
0xE7	IEN2	RW	0000_0000Ь	Interrupt enable register 2
0xF4	IPL2	RW	0000_0000b	Interrupt priority register2

SPI SFR register list

pen (a)	Secondary bus register						
Address	Name	RW	Reset	Description			
0x3E	SPI_TX_START_ADDR	RW	0000_0000Ь	SPI high-speed mode transmit buffer first address			
0x3F	SPI_RX_START_ADDR	RW	0000_0000Ь	SPI high-speed mode receive buffer first address			
0x40	SPI_NUM_L	RW	0000_0000Ь	SPI high-speed mode data buffer address number, low 8 bits			
0x41	SPI_NUM_H	RW	xxxx_0000b	SPI high-speed mode data cache address number, high 4 bits			
0x68	SPI_IO_SEL	RW	xxxx_xx00b	SPI communication port selection register			
0x69	SPI_MCLK_MOD	RW	xxxx_xxx0b	SPI master mode receiver clock selection register			

SPI Secondary bus register list

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	7 60	20%	BF/313CM4					44-LJ1X	
SPI CFG1 (B5H) SPI control register 1						7025-1	7.01.16:5		
	Bit number	7	6	5	4	3	2	1	0
	Symbol	RX_IE	SPI_EN	TX_IE	MSTR	CPOL	СРНА	LSBFE	CS_N
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset value	0	0	0	1	0	1	0	1

Bit number	Bit symbol	Description
7	RX_IE	Receive enable- SPI receive buffer is full (SPRF) interrupt enable 1: Interrupt is valid; 0: Interrupt is disabled (using polling)
6	SPI_EN	SPI enable: 1: module enable open; 0: module enable close
5	TX_IE	Transmit enable -SPI transmit buffer empty (SPTEF) interrupt enable 1: Interrupt is valid; 0: Interrupt is disabled (using polling)
4	MSTR	Master-slave mode selection 1: master mode; 0: slave mode
3	CPOL	SCLK active level selection 1: Active low; 0: Active high
2	СРНА	SCLK phase selection  1: Send data at the first valid clock edge  0: Sample data at the first valid clock edge
1	LSBFE	LSB first (shifter direction)  1: SPI serial data transmission starts from the lowest bit  0: SPI serial data transmission starts from the highest bit
0	CS_N	Chip select signal 0: Pull down CS; 1: Pull up CS

# 11.2.2. SPI Control Register 2

SPI CFG2 (B6H) SPI control register 2

211 01 02 (20)	ii, sii tomatti iigist	· -		
Bit number	7	6	5	4
Symbol	<u> </u>	FEEDBACK	HSPEED_START	HALF_FUPLEX
R/W	- 35	R/W	R/W	R/W
Reset value		76200 1/6	0	76:01 16:01
Bit number	3	ing. 27-11	1	128. 0
Symbol	BIDIR_SELECT	My-C. BAD	SPR	My-0, BAD

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$(11)$ $\sim$	7()00			
P/W	R/W	R/W	R/W	R/W
Reset value	1	0	0	02-0

Bit number	Bit symbol	Description				
6	FEEDBACK	Send the received data to the master\slave  1: Send the received data to the master\slave  0: Send the data written by MCU to the master\slave				
5	HSPEED_START	The high-speed SPI communication mode is turned on ar the hardware is automatically pulled down after the work completed  1: High-speed SPI communication mode is on;  0: High-speed SPI communication mode is off  In high-speed SPI mode, whether in slave or master mode the chip select signal cannot be pulled high, which will cause the data sent by SPI to be lost				
4	HALF_FUPLEX	Half-duplex mode selection:  1: Select half-duplex mode; 0: Select full-duplex mode				
3	BIDIR_SELECT	Half-duplex mode, transmission and reception direction selection 1: Send; 0: Seceive				
2~0	SPR	SPI baud rate coefficient: maximum communication frequency 2MHz  000: spi_clk/2; 001: spi_clk /4;  010: spi_clk/6; 011: spi_clk /8;  100: spi_clk/10; 101: spi_clk /12;  110: spi_clk/14; 111: spi_clk /16;				

# 11.2.3. SPI Status Flag Register

SPI\_STATE (BEH) SPI status flag register

Bit number	7~3	2	1	0
Symbol	_	SPRF	OVERFLOW_RX	SPTEF
R/W	_	R/W	R/W	R/W
Reset value	_	0	0	1

	Bit number	) Bit symbol	Description	
	7~30.	· · · · · · · · · · · · · · · · · · ·	Reserved 10 25	
	260 00 1 16	20.2	Read buffer full mark, software write 0 to clear	) '
Q	2	SPRF	0: No data is available in the receive data buffer;	
	1520 PIE	\ <u></u>	1. There is data in the receive data buffer	

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(0)	70.33	
1 bente 01 10	OVERFLOW_RX	In the normal communication mode, when the receiving overflow is caused by not reading in time,  OVERFLOW_RX=1, the signal does not generate an interrupt, only the mark  In high-speed SPI communication mode, it is invalid (when the number of received data is equal to the configured {SPI_NUM_H, SPI_NUM_L}, the work will end, SPRF will be set, and a full interrupt will be generated).
0	SPTEF	Send buffer empty mark, write into SPID hardware to clear automatically. In the SPI idle state, the first data written to SPID will be directly stored in the shift register, and the second data written will be loaded into the transmit buffer, and SPTEF will be automatically pulled low.  1: The data buffer is empty and data can be written;  0: The data buffer is not empty

### 11.2.4. SPI Port Data Register

SPI\_SPID (BFH) SPI port data register

Bit number	7	6	5	4	3	2	1	0		
Symbol		SPI_SPID[7:0]								
R/W		R/W								
Reset value		0								
-010				-010	<b>)</b>			-010		

1 600		1 (0)
Bit number Bit symb	ol	Description
7~0 SPI_SPID[	7:0]	SPID reading this register will return the data read from the receive data buffer rx_reg. Writing to this register will write data into the transmit data buffer tx_reg.  Data should not be written into the transmit data buffer, unless the SPI transmit buffer empty flag (SPTEF) is set, indicating that there is a certain space in the transmit buffer to queue new transmit bytes.  After setting the SPRF and before completing another transmission, you can read data from the SPID at any time. If the data is not read from the receive data buffer before the end of the new transmission, the receive overflow will result and the newly transmitted data will be lost.

# 11.2.5. SPI Interrupt Register

IRCON2 (E1H) Interrupt flag register 2

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111115	, // / a		\		1/ 10		1.1	
Bit number	7	6	35en	14/0	3	2	Devid	0/0/0.2
Symbol	IE15	IE14 <b>〈</b>	IE13	IE12	IE11	IE10 🌣	III PES	IE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	RW	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
5	IE13	SPI interrupt flag  1: With SPI interrupt flag 0: Clear SPI interrupt flag

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	©EX15	EX14	EX13	EX12	• EX11	EX10	EX9	EX8
R/W	RW	R/W	R/W	RW	RW	R/W	R/W	R/W
Reset value	20.0	0	Qen!	0/0/	20.0	0	1gen (	0/1/2
			ing.	17/11			128.	

Bit number	Bit symbol	1052-0 BAD	Description	W 2-1 BXD
		SPI interrupt enable		No.
5	EX13	1: SPI interrupt enable;		
		0: SPI interrupt disable		

IPL2 (F4H) Interrupt priority register2

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL2.7	IPL2.6	IPL2.5	IPL2.4	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0_0
14.co	25			y. cor	25			y. cor

Bit number	Bit symbol	Description	7.00
S CONTRACT		SPI priority selection bit.	ving. per U. M. In.
122-05/1	IPL2.5	1: SPI priority is high;	111 1117-01
		0: SPI priority is low	

# 11.3. SPI Secondary Bus Register

### 11.3.1. SPI High-speed Mode Transmit Buffer First Address

SPI TX START ADDR (3EH) SPI high speed mode transmit buffer first address

	~		(/							
	Bit number	7	6	5	4	3	2	1	0	
	Symbol	0	com				com			
	R/W	6.35	R/W			$\mathcal{C}_{\mathbf{W}}$			ovd. co	
	Reset value	20.	Den(0) 1 10.90.			9	pen(0) 1/0:3			
5			: 20:				*	20.		

Bit number Bit symbol Description

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	71	100	
02-02-01 10	,5,	<del></del>	In SPI high-speed mode, the first address of the transmit data buffer, SPI_TX_START_ADDR*16

### 11.3.2. SPI High-speed Mode Receiving Buffer First Address

SPI RX START ADDR (3FH) SPI High-speed mode receiving buffer first address

		(							
Bit number	7	6	5	4	3	2	1	0	
Symbol		_							
R/W		R/W							
Reset value				(	0				

	Bit number	Bit symbol	Description
	1 80 (0) 0 1 (1)	26.33	In SPI high-speed mode, the first address of the receive data
5	Dr. 1-01 10		buffer, SPI_RX_START_ADDR*16

### 11.3.3. SPI Number of Data Cache Addresses in High-speed Mode

SPI NUM L (40H) SPI high-speed mode data buffer address number low 8 bits

Bit number	7	6	5	4	3	2	1	0	
Symbol		SPI_NUM_L[7:0]							
R/W		R/W							
Reset value				(	)				

Bit number Bit symbol	Description COM
SPI_NUM_L[7:0]	Number of data buffer addresses in SPI high-speed mode, low 8 bits
CDI AUTA II (41II) CDI 1 : 1	

of involving the strain of the spectation of the strain of								
Bit number	7	6	37.7.	4	3	2	1/1/2	B <sub>0</sub>
Symbol	_	_	_	_		SPI_NU	M_H [3:0]	
R/W	_	_	_	_	R/W	R/W	R/W	R/W
Reset value	_	_	_	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	SPI_NUM_H[3:0]	Number of data buffer addresses in SPI high-speed mode, high 4 bits

### 11.3.4. SPI Communication Port selection Register

SPI\_IO\_SEL (68H) SPI communication port selection register

Bit number	7	6	25-7	B41	3	2	2-11	50

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	7(10-							
Symbol	_	_	-	_	_	_	SPI_IO_	SEL[1:0]
R/W	_	_	_	_	_	_	R/W	R/W
Reset value	_	_	_	_	_	_	0	0

Bit number	Bit symbol	Description		
		SPI communication port selection register		
1.0	SPI IO SEL[1:0]	01: PC2/3/4/5 selects SPI function		
1~0	SFI_IO_SEL[1.0]	10: PE4/5/6/7 selects SPI function		
		00/11: PG0/1/2/3 selects SPI function		

# 11.3.5. SPI Master Mode Receiver Clock Selection Register

SPI MCLK MOD (69H) SPI master mode receiver clock selection register

		()						_ 4 \ \ \ \ \	
Į	Bit number	7	6	. 2.3em	1 1 4 10.	3	2	og. Perso	0/0
	Symbol	_	_ ~	77.50	BYD	_	- 77	1-600	BID
	R/W	_	_		_	_	_	77723	R/W
	Reset value	_	_		_		_	_	0

Bit number	Bit symbol	Description
		SPI master mode receiver clock selection register
0		1: Select the host output as the receive clock;
		0: Select the PAD port input as the receive clock

BAD

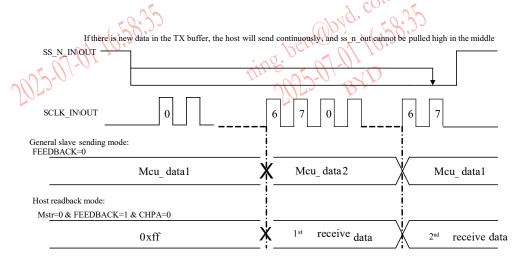
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### 11.4. Communication Timing

There are three flag bits, two interrupt mask bits and an interrupt vector related to the SPI system. The SPI receive interrupt enable bit (RX IE) allows interrupts from the SPI receiver full flag (SPRF) to occur. The SPI transmit interrupt enable bit (TX IE) allows interrupts from the SPI transmit buffer empty flag (SPTIEF) to occur. When a flag bit is set and the related interrupt enable bit is set, the hardware interrupt request is sent to the CPU. If the interrupt enable bit is cleared, the software can poll the relevant flag bit without interruption. The SPI interrupt service routine (ISR) should check the flag bit to determine the event that caused the interrupt. Before returning from the ISR (usually near the starting point of the ISR), the service program should also clear the flag bit.

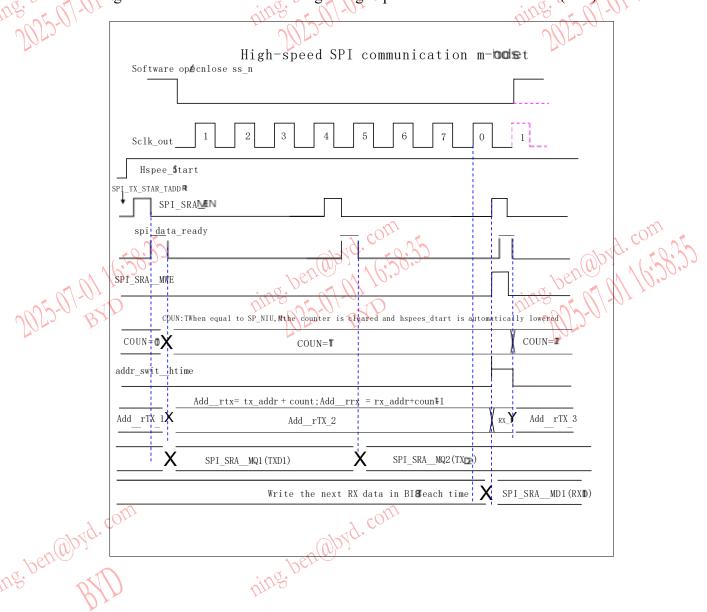
Schematic diagram of SPI continuous working in normal communication mode: 2025-07-01-16:58:35



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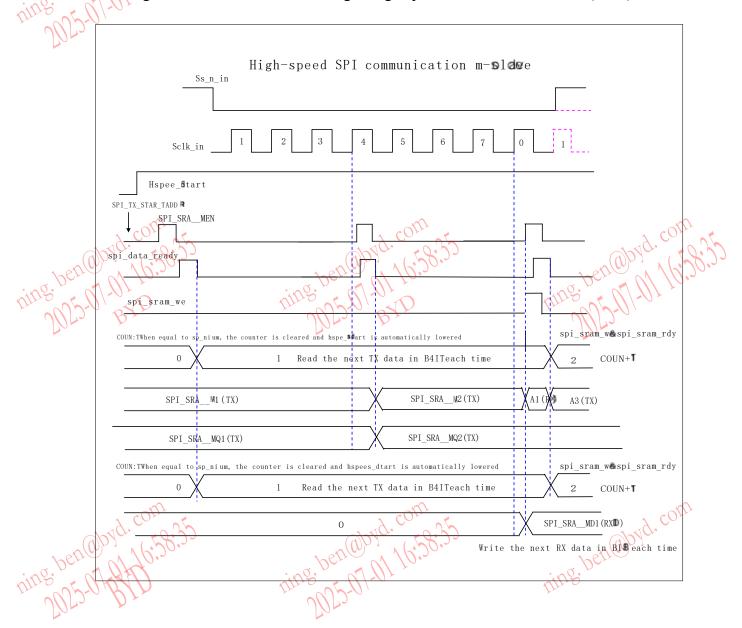
Schematic diagram of SPI continuous working in high-speed communication mode (host):



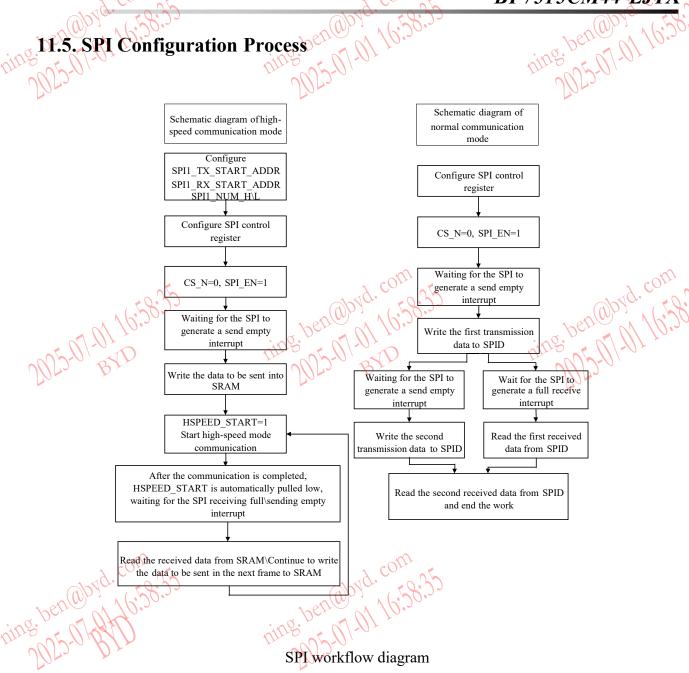
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Schematic diagram of SPI continuous working in high-speed communication mode (slave):



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### Note:

- Configure CPOL and CPHA when the chip selection is high, otherwise SCLK has glitches (master, slave)
- In high-speed mode, happened start will be automatically pulled low after the work is completed. At this time, the host can no longer send SCLK, otherwise an unstable state will occur.
- In slave mode, after the chip select is pulled low, SPI EN cannot be turned off. Otherwise, when the SPI EN is reopened, when the chip select becomes low again, the internally generated SCLK will have a glitch. That is, while SPI is selected, SPI EN cannot be turned off.
- In the slave mode, if the chip select is always 0, if you need to switch CPOL\CPHA\LSBFE midway, the slave can only switch after the master raises the chip select.
- In high-speed mode, if an odd number of data is sent in each frame, the chip select signal needs to be pulled up once between each frame.

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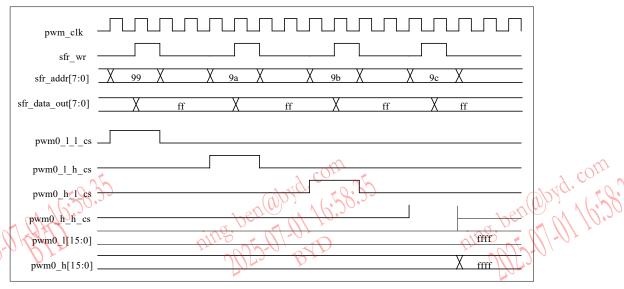


12. PWM



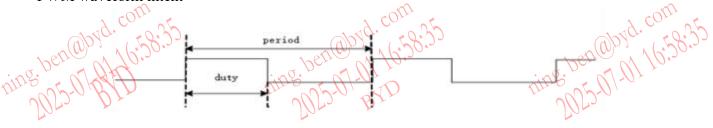
- 4 independent PWM modules;
- high-level control register and low-level control register: 16-bit register;
- Output period: Tpwm data = (PWM H + PWM L) \*Tpwm clk;
- Output duty cycle: Dpwm data = PWM H/ (PWM L + PWM H);
- PWM 0 shares period and duty cycle, each channel has independent polarity control;
- PWM 1 shares period and duty cycle, each channel has independent polarity control;
- PWM 2 and PWM 3 each support one output port and the polarity is not selectable
- PWM 0 and PWM 1 can be configured to output overflow interrupt respectively, PWM2 and PWM 3 do not support;
- Support common frequency: 38kHz (infrared application)

When the PWM 0 and PWM 1 count values are full, an overflow interrupt occurs, and the interrupt enable configuration is valid, the core enters the PWM interrupt.



The period and pulse width of the PWM pulse width modulation module can be configured through registers. When PWM\_H + PWM\_L = 0, the output is low, but the configuration of the register must be selected when the PWM output port is valid (active high) and high The high level control register and the low level control register must be configured in order from low to high, in order to ensure that the internal counter of the PWM module counts correctly and avoid generating wrong waveforms.

PWM waveform intent



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### 12.1. PWM Channel Configuration

The BF7515CM44-LJTX provide 4 independent 16bit PWM modules.

- PWM 0 supports 5 output ports (PWM0A, PWM0B, PWM0C, PWM0D, PWM0E);
- PWM 1 supports 5 output ports (PWM1A, PWM1B, PWM1C, PWM1D, PWM1E);
- PWM 2 supports 1 output ports (PWM 2);
  - PWM 3 supports 1 output ports (PWM 3);

PWM0 and PWM1 of the BF7515CM44-LJTX provide 8 output channels at most. When PWM0A and PWM1E are configured at the same time, PWM0A is valid and PWM1E is invalid; when PWM0B and PWM1D are configured at the same time, PWM0B is valid and PWM1D is invalid. See PWM port selection register (PWM\_IO\_SEL) and PWM port selection register 1 (PWM\_IO\_SEL1).

### 12.2. PWM Related Registers

UD B		<i>→</i>	SFR reg	gister		
Address	Name	RW	Reset	Description		
0x99	PWM0_L_L	RW	0000_0000Ь	PWM0 low level control register(low 8-bit)		
0x9A	PWM0_L_H	RW	0000_0000Ь	PWM0 low level control register (high 8-bit)		
0x9B	PWM0_H_L	RW	0000_0000Ь	PWM0 high level control register(low 8-bit)		
0x9C	PWM0_H_H	RW	0000_0000Ь	PWM0 high level control register (high 8-bit)		
0x9D	PWM1_L_L	RW	0000_0000Ь	PWM1 low level control register(low 8-bit)		
0x9E	PWM1_L_H	RW	0000_0000Ь	PWM1 low level control register (high 8-bit)		
0x9F	PWM1_H_L	RW	0000_0000Ь	PWM1 high level control register(low 8-bit)		
0xA1	PWM1_H_H	RW	0000_0000Ь	PWM1 high level control register (high 8-bit)		
0xA2	PWM2_L_L	RW	0000_0000Ь	PWM2 low level control register(low 8-bit)		
0xA3	PWM2_L_H	RW	0000_0000Ь	PWM2 low level control register (high 8-bit)		
0xA4	PWM2_H_L	RW	0000_0000Ь	PWM2 high level control register(low 8-bit)		
0xA5	PWM2_H_H	RW	0000_0000Ь	PWM2 high level control register (high 8-bit)		
0xA6	PWM3_L_L	RW	0000_0000Ь	PWM3 low level control register(low 8-bit)		
0xA7	PWM3_L_H	RW	0000_0000Ь	PWM3 low level control register (high 8-bit)		
0xA9	PWM3_H_L	RW	0000_0000Ь	PWM3 high level control register(low 8-bit)		
0xAA	PWM3_H_H	RW	0000_0000Ь	PWM3 high level control register (high 8-bit)		
0xAE	INT_PE_STA T	RW	0000_0000ь	Interrupt status register		
0xE1	IRCON2	RW	0000_0000b	Interrupt flag register 2		
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1		
0xE7	IEN2	RW	0000_0000b	Interrupt enable register 2		
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1		
0xF4	IPL2	RW	0000_0000b	Interrupt priority register2		

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0xF6	IPL1	RW	0000_00xxb	Interrupt priority register1
OUXFA	PWM_INT_C TRL	RW	xxxx_xx00b	PWM interrupt enable control register

### 12.2.1. PWM0 Level Control Register

PWM0\_L\_L (99H) PWM0 low level control register (low 8-bit)

<u> </u>	11) 1 11110	7 10 11 10 101	Common 10	515001 (10 11	0 010)			
Bit number	7	6	5	4	3	2	1	0
Symbol					_			
R/W				R/	W			
Reset value	0				)			-10-

PWM0 L H (9AH) PWM0 low level control register (high 8-bit)

			10 ( )		
Bit number	30.7	6	5 4 5 3	2	1,000
Symbol		•	25. De 1 01 10	***	15. pc. 12 11 In.
R/W		1	R/W	TI.	002-01
Reset value			0		Mile

PWM0 H L (9BH) PWM0 high level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol					_			
R/W				R/	W			
Reset value				(	)			

PWM0 H H (9CH) PWM0 high level control register (high 8-bit)

	Bit number	7	6	5	4	3	2	1	0
	Symbol O				y com	-			Y COLLY
	R/W			~(0	R/	W			Sold Con
5.	Reset value			va. perio	(	)	•	og. pen	11/10.

### 12.2.2. PWM1 Level Control Register

PWM1 L L (9DH) PWM1 low level control register (low 8-bit)

_	TWINI_E_E (SEII) TWINI IOW IOVER CONTROL (IOW CON)										
	Bit number	7	6	5	4	3	2	1	0		
	Symbol					_					
	R/W				R/	W					
	Reset value				(	0					

PWM1 L H (9EH) PWM1 low level control register (high 8-bit)

Bit number 7	6	5	4,000	3	2	1	000
Symbol		(a	phyg. co	5.3,5			org. co
DED R/W 16 DO		henle	R	W		hen (a	1/0:2
Reset value		126.	1/7//	)	n't'	v8 V	17/17

PWM1\_H\_L (9FH) PWM1 high level control register (low 8-bit)

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	$(0)$ $\beta$ $\beta$	20.5		(1)	JD 1 ( 1/2	10.5		$(\mathbf{q})$	17 CA			
<	Bit number	7	6	75en	1/4/0.	3	2	S PEUT	0/0/0.			
ح	Symbol		ning of 0/-01									
(	R/W		R/W									
	Reset value		0									
	PWM1_H_H (A	1H) PWM	11 high lev	el control 1	egister (hi	gh 8-bit)						
	Bit number	7	6	5	4	3	2	1	0			
	Symbol				PWM1_F	H_H [7:0]						
	R/W		R/W									
	Reset value				(	)						

# 12.2.3. PWM2 Level Control Register

PWM2 L L	A2H)	PWM2 low leve	el control register	(low 8-bit)

Bit number	7	6	: 2.5	4	3	2	1 0
Symbol			Jun of	PWM2_I	L_L [7:0]		THE ON SOUBLE
R/W				R/	W		Mar
Reset value				(	0		

### PWM2 L H (A3H) PWM2 low level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0	
Symbol		PWM2_L_H [7:0]							
R/W				R/	W				
Reset value				(	)				

### PWM2\_H\_L (A4H) PWM2 high level control register (low 8-bit)

Bit number 7	6	5	4000	2	1	Y O OUT
Symbol		~(C	PWM2_H_L [7:	0]		Dya C.
R/W		20. Perr	R/W	•	og. perio	W. 10.
Reset value	ζ.	111202-	0	71	11202-	1/-0,

PWM2\_H\_H (A5H) PWM2 high level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol		PWM2_H_H [7:0]						
R/W		R/W						
Reset value		0						

### 12.2.4. PWM3 Level Control Register

PWM3 L L (A6H) PWM3 low level control register (low 8-bit)

Bit number 7	6	5 4 2 3	2	1 0000
Symbol		PWM3_L_L [7:0]		pen (1) 16:31
R/W	ning	R/W	ni	vs. 2 W-111
Reset value	0	0		JO 13-0

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PWM3 L H (A7H) PWM3 low level control register (high 8-bit)

C	Bit number	7	6	3	3	2 1100 1 00
	Symbol			PWM3_L_H [7	7:0]	Mrs Br
	R/W			R/W		
	Reset value			0		

PWM3 H L (A9H) PWM3 high level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol		PWM3 H L [7:0]						
R/W		R/W						
Reset value				(	)			

PWM3 H H (AAH) PWM3 high level control register (high 8-bit)

	Bit number 7	6 5	3	2	1 000
	Symbol	7	PWM3_H_H[7:0]		Per (0) 1/1:3
ع	R/W	sing.	R/W	i	28. W.M. 10
(	Reset value	200	0	<b>V</b>	11, 3-0,

### 12.2.5. PWM0 and PWM1 Interrupt Register

INT\_PE\_STAT (AEH) Interrupt status register

Bit number	7	6	5	4
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2 2 com	1	0 y com
Symbol	NT_TIMER2_STAT	INT_PWM0_STAT	INT_LCD_STAT	INT LED STAT
R/W	R/W	R/W	R/W	O DET BANK JOIN
Reset value	0 111	205-00	0 1111	2017-10-11

Bit number	Bit symbol	Description
		PWM1 interrupt status flag, this bit is cleared by writing
7	7 INT_PWM1_STAT	0, and it can also be cleared by closing the PWM1 channel
		1: Interrupt is valid; 0: Interrupt is invalid
		PWM0 interrupt status flag, this bit is cleared by writing
2	2 INT_PWM0_STAT	0, and it can also be cleared by closing the PWM0
2,00		channel d com
Opla.	18:00	1: Interrupt is valid; 0: Interrupt is invalid

IRCON2 (E1H) Interrupt flag register 2

	4100112 (4111)	mreen apr	1145 1955	- \ )	_ / / / } _			()	- 111
0	Bit number	7	6	ings	4	3	2	me is	0
1	Symbol	IE15	IE14	TEXB. 3	IE12	IE11	IE10	JED	PE8

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(0)	7()00							. ( , ) (
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RWD.
Reset value	0	0	0	0	0	0	205	

Bit number	Bit symbol	Description
		Timer3/PWM1 interrupt flag
4	IE12	1: Timer3/PWM1 interrupt flag
		0: Clear Timer3/PWM1 interrupt flag

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	_	EX4	EX3	EX2	_	_
R/W	N/W	R/W	_	R/W	R/W	R/W	_	om
Reset value	.0.70	0	_	7710.	0.20	0	_	721g.

	Bit number	Bit symbol	Description in S.
1	152-0, BXD	,	WDT/Timer2/PWM0 interrupt enable
	7	EX7	1: WDT/Timer2/PWM0 interrupt enable;
			0: WDT/Timer2/PWM0 interrupt disable

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	EX15	EX14	EX13	EX12	EX11	EX10	EX9	EX8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description	14. COM
0001	3.33	Timer3/PWM1 interrupt enable	000
5 Derra 40 A	EX12	1: Timer3/PWM1 interrupt enable;	ina period W/M.
20201811		0: Timer3/PWM1 interrupt disable	Will Sold of Many

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	_	IE4	IE3	IE2	_	_
R/W	R/W	R/W	_	R/W	R/W	R/W	_	_
Reset value	0	0	_	0	0	0	_	_

Bit number	Bit symbol	Description	
7	IE7	WDT/Timer2/PWM0 interrupt flag  1: With interrupt flag; 0: Without interrupt flag	a com

IPL2 (F4H) Interrupt priority register2

1	Bit number	7	6	15th (0	140.3	3	2	PAULO	0/00.3
	Symbol	IPL2.7	IPL2.61	PPL2.5	IPL2.4	IPL2.3	IPL2.21	PPL2.	IPL2.0
7	R/W	R/W	R/W	RW	R/W	R/W	R/W	RW	R/W

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(11)6, '(20)		((1))~,	. ( . )	(100	
Reset value 0	0	2 pay	90	0	0

Bit number	Bit symbol	Description
		Timer3/PWM1 priority selection bit
4	IPL2.4	1: Timer3/PWM1 interrupt is high priority;
		0: Timer3/PWM1 interrupt is low priority

IPL1 (F6H) Interrupt priority register1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	_	IPL1.4	IPL1.3	IPL1.2	_	_
R/W	R/W	R/W	_	R/W	R/W	R/W	_	_
Reset value	0	0	-	0 0	0	0	-	-com

/ /// / /	Z . 10	
Bit number	Bit symbol	Description Description
2 4/1/1		WDT/Timer 2/PWM0 interrupt priority bit
7	IPL1.7	1: WDT/Timer 2/PWM0 interrupt is high priority;
		0: WDT/Timer 2/PWM0 interrupt is low priority

PWM INT CTRL (FAH) PWM interrupt enable control register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	_	_
R/W	_	_	_	_	_	_	R/W	R/W
Reset value	_	_	_	_	_	_	0	0

	Bit number	Bit symbol	Description
	11d.co		PWM1 counter overflow interrupt
	(0)0)		1: Interrupt enable; 0: Interrupt disable
NITE	0	<u></u>	PWM0 counter overflow interrupt
III	PID	`	1: Interrupt enable; 0: Interrupt disabled

# 12.3. Secondary Bus Register

	Secondary bus register									
Address	Name	RW	Reset	Description						
0x33	PWM_IO_SEL	RW	0000_0000Ь	PWM port selection register						
0x59	PWM_IO_SEL1	RW	xxxx_0000b	PWM port selection register 1						
0x60	PWM0_POLA_SEL	RW	xxx0_0000b	PWM0 polarity selection register						
0x61	PWM1_POLA_SEL	RW	xxx0_0000b	PWM1 polarity selection register						

### 12.3.1. PWM Port Selection Register

PWM\_IO\_SEL (33H) PWM port selection register

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	7()				1(),0		(11)	P. 1. 1.
Bit number	7	6	5en	14/0.	3	2	~ pro	110,000
Symbol	_	_ \dag{\alpha}	12.8. J.		_	- 17	U.S. 02-0	/-0,
R/W	R/W	R/W	R/W	R/W	R/W	R/W	RW	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description				
7 PWM_IO_SEL[7]		PWM3 selection enable				
		1: PWM3 function is selected;				
		0: PWM3 function is not selected				
		PWM2 selection enable				
6	PWM_IO_SEL[6]	1: PWM2 function is selected;				
		0: PWM2 function is not selected				
		PWM1C selection enable				
5	PWM_IO_SEL[5]	1: PWM1C function is selected;				
		0: PWM1C function is not selected				
		PWM1B selection enable				
4	PWM_IO_SEL[4]	1: PWM1B function is selected;				
		0: PWM1B function is not selected				
		PWM1A selection enable				
3	PWM_IO_SEL[3]	1: PWM1A function is selected;				
		0: PWM1A function is not selected				
		PWM0C selection enable				
2	PWM_IO_SEL[2]	1: PWM0C function is selected;				
		0: PWM0C function is not selected				
		PWM0B selection enable				
		1: PWM0B function is selected;				
1	PWM_IO_SEL[1]	PWM0B selection enable 1: PWM0B function is selected; 0: PWM0B function is not selected				
		When PWM0B and PWM1D are configured at the same				
		time, PWM0B is valid and PWM1D is invalid				
		PWM0A selection enable				
		1: PWM0A function is selected;				
0	PWM_IO_SEL[0]	0: PWM0A function is not selected				
		When PWM0A and PWM1E are configured at the same time, PWM0A is valid and PWM1E is invalid				

# 12.3.2. PWM Port Selection Register 1

PWM IO SEL1 (59H) PWM port selection register 1

Symbol	Bit number	7	6	25 1 14	3	2 1 0
	Symbol	_	- 112	JUJ 2-1, BAD	_	100 D-0 BID

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$(U)_{\Sigma}$ , $(V)_{\Sigma}$							. ( . )
PEN R/W	_	_	_	R/W	R/W	R/W	R/W
Reset value _	_	_	_	0	0	050	0

Bit number	Bit symbol	Description
		PWM1E selection enable 1: PWM1E function is selected;
3	PWM_IO_SEL[3]	0: PWM1E function is not selected
		When PWM1E and PWM0A are configured at the same time, PWM0A is valid and PWM1E is invalid
		PWM1D selection enable
	PWM_IO_SEL[2]	1: PWM1D function is selected;
2		0: PWM1D function is not selected
		When PWM1D and PWM0B are configured at the same time, PWM0B is valid and PWM1D is invalid
		PWM0E selection enable
1	PWM_IO_SEL[1]	1: PWM0E function is selected;
		0: PWM0E function is not selected
		PWM0D selection enable
0	PWM_IO_SEL[0]	1: PWM0D function is selected;
		0: PWM0D function is not selected

#### 12.3.3. PWM0 Polarity Selection Register

PWM0 POLA SEL (60H) PWM0 polarity selection register

Bit number 7	6	5	1014	8.33	2	1 (	bydo 19
Symbol	_	- pen	1 1p.	-	-	pend	1/0.3
R/W	_	ing of	R/W	R/W	R/W	R/W	R/W
Reset value _	_	2777	0	0	0	0	0

Bit number	Bit symbol	Description				
7~5		Reserved				
,		PWM0E output polarity selection				
4		1: Reverse output; 0: Normal output				
		PWM0D output polarity selection				
3		1: Reverse output;				
		0: Normal output				
_		PWM0C output polarity selection				
2		1: Reverse output; 0: Normal output				
Ova		PWM0B output polarity selection				
1970		1: Reverse output; 0: Normal output				

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(0)	70.3	
pence 1/0	,50	PWM0A output polarity selection
ning of Ord		1: Reverse output; 0: Normal output

#### 12.3.4. PWM1 Polarity Selection Register

PWM1 POLA SEL (61H) PWM1 polarity selection register

	((							
Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	_	_
R/W	_	_	_	R/W	R/W	R/W	R/W	R/W
Reset value	_	_	_	0	0	0	0	0

_ X	$\Omega$	- n	
Bit number	Bit symbol	Description	1 21 d. COL
7~5	56.33 <u></u>	Reserved	3000
2 00, (40)		PWM1E output polarity selection	ing ber of Million
1050	*	1: Reverse output; 0: Normal output	Jul 9-01-01
3		PWM1D output polarity selection	Mre
		1: Reverse output; 0: Normal output	
2		PWM1C output polarity selection	
		1: Reverse output; 0: Normal output	
1		PWM1B output polarity selection	
		1: Reverse output; 0: Normal output	
0		PWM1A output polarity selection	
		1: Reverse output; 0: Normal output	

BYD

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## 12.4. PWM Configuration Process



PWM Schematic diagram of configuration process

**Note:** frequency range: 184Hz ~ 120kHz recommended.

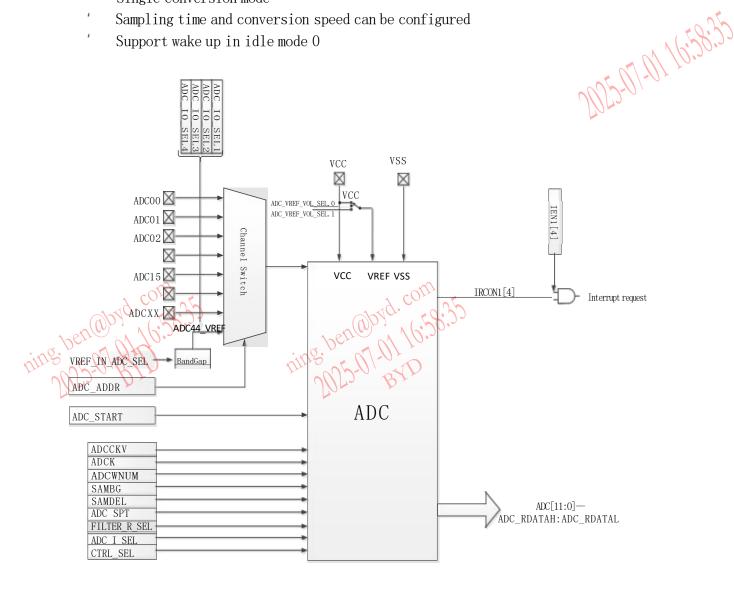
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#### BF7515CM44-LJT

ning ben abyd com

ning 105-07-01 16:5 The BF7515CM44-LJTX chip contains a single-ended, 12-bit linear successive approximation analog-to-digital converter (ADC), and the reference voltage of the ADC is connected to the VCC of the chip. ADC channels can input independent analog signals. The ADC c h an ne 1 e ach ti omn eaf, ter tha DC\_STAR module c onver ts 1 conversion is completed, the ADC result register is updated and an interrupt is generated. The BF7515CM44-LJTX chip has the following characteristics:

- 12-bit resolution linear and successive approximation to ADC
- Single conversion mode
- Sampling time and conversion speed can be configured
- Support wake up in idle mode 0



ADC structure block diagram

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#### 13.1. ADC Related Register

Ura B			SFR registe	er Marian
Address	Name	RW	Reset	Description
0xC1	ADC_SPT	RW	0000_0000b	ADC sampling time configure register
0xC3	ADC_SCAN_CFG	RW	x000_0000b	ADC scan configuration register
0xC4	ADCCKC	RW	0000_0000Ь	ADC clock and filter configuration register
0xC5	ADC_RDATAH	R	xxxx_0000b	ADC scan result register, high 4 bits
0xC6	ADC_RDATAL	R	0000_0000Ь	ADC scan result register, low 8 bits
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register1

ADC SFR register list

	MCr.	V/ / / / /	1 11	e si it issister						
5	m - 1		Seco	ndary bus reg	ister ing					
	Addr	Name	RW \	Reset	<b>Description</b> B					
	0x2A	ADC_IO_SEL0	RW	x000_0000b	ADC function selection register 0					
	0x2D	PD_ANA	RW	x111_xx11b	Analog ADC judgment register					
	0x32	ADC_CFG_SEL	RW	x000_0000b	ADC configuration register					
	0x42	ADC_CFG_SEL1	RW	xx00_0010b	ADC comparator offset cancellation selection register					
	0x53	ADC_IO_SEL1	RW	0000_0000Ь	ADC select enable register 1					
	0x54	ADC_IO_SEL2	RW	0000_0000Ь	ADC select enable register 2					
	0x55	ADC_IO_SEL3	RW	0000_0000Ь	ADC select enable register 3					
	0x56	ADC_IO_SEL4	RW	0000_0000Ь	ADC select enable register 4					
	0x57	ADC_IO_SEL5	RW	xxx0_0000b	ADC select enable register 5					
	ADC list of secondary bus registers  13.1.1. ADC Sampling Time Configuration Register									
	10.1.1.			izui autuli 110						

#### 13.1.1. ADC Sampling Time Configuration Register

ADC SPT (C1H) ADC sample time configuration register

		_ 1								
Bit number	7	6	5	4	3	2	1	0		
Symbol		ADC SPT[7:0]								
R/W		R/W								
Reset value				(	)					

Bit number Bit symbol	Description Off
Den (720 ) ADC_SPT[7:0]	ADC sampling time configuration register  Sampling time: t1= (ADC_SPT+1)*4* TADCK

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### 13.1.2. ADC Scan Configuration Register

7 0	05				20	<u> </u>	SF/313	CM44-LJ1X	7
13.1.2. ADC ADC SCAN			-00	5010	gister		7	025.07.01 16:5	3:
Bit number	7	6	5	4	3	2	1	0	
Symbol	_		ADC ADDR						
R/W	_		R/W						
Reset value	_			(	0			0	

Bit number	Bit symbol	Description
		ADC channel address selection register 000000: corresponding to ADC0; 000001: corresponding to ADC1;
6~1	ADC_ADDR	101010: corresponding to ADC42; 101011: corresponding to ADC43; 101100: corresponding to ADC44_VREF
		Other: Reserved
		ADC scan open register
		0: ADC module does not scan;
		1: ADC module starts to scan
		ADC_START is set from 0 to 1, ADC starts to scan, after
0	ADC_START	one scan, ADC_START hardware is automatically set to 0,
		corresponding to the ADC interrupt flag bit, the ADC
		interrupt flag bit needs to be cleared by software
		Note: ADC_START is not allowed to be configured during scanning

#### 13.1.3. ADC Clock and Filter Configuration Register

ADCCKC (C4H) ADC clock and filter configuration register

Bit number	7	6	5	4
Symbol	FILTER_SEL	SAMBG	SAN	MDEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	ADC	CKV	Λ AI	OCK ON
R/W	R/W	R/W	R/W	R/W
Reset value	0	1000	0	1000
		110 111 10		

Bit symbol Description Bit number

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$(0)$ $\beta$	20.2								_		
pence 1/1	FILTE	R SEL	1	U	ilter selecti						
205-01			0: No RC	C filter add	ed; 1: RC	filter adde	d.				
6	SAN	MBG		Sampling timing and comparison timing interval selection 0: interval of 0 Tadck; 1: interval of 1 Tadck							
			Sampling	g delay tim	e selection	L					
5~4	SAN	1DEL	00: 0*TA	лск; 01: 2	*Tadck:						
	3,54				10: 4*Tadck; 11: 8*Tadck						
3~2	ADC	CCKV	ADC comparator offset cancellation analog input clock								
3 2			00: 12M	Hz; 01: 8N	//Hz; 10: 4	MHz; 11:	2MHz				
			ADC clo	ck							
1~0	AΓ	OCK	00: 8MH	z; 01: 6M	Hz;						
			10: 4MH	z; 11: 3M	Hz			<b>≠</b> (	25		
								160	19:72		
13.1.4. ADC	Scan Re	sult Regi	ister				. 0	2 () In.			
	2011 11 112 8 Semi Itelani Itelani										
ADC RDATAF	H (C5H) A	DC scan r	esult regist	ter high 41	oits		, Mrs				
Bit number	7	6	5	4	3	2	1	0			

#### 13.1.4. ADC Scan Result Register

TIE G_TEETITITITITITITITITITITITITITITITITITI								
Bit number	7	6	5	4	3	2	1	0
Symbol	-	_	_	_		ADC_RD	ATAH [3:0	)]
R/W	_	_	_	_			R	
Reset value	_	_	_	_			0	

ADC RDATAL (C6H) ADC scan result register, low 8 bits

 DC ICDITITE	(0011) 111	o o beam re	56111 1051511	1,10 11 0 01				
Bit number	7	6	5	4	3	2	1	0
Symbol		ADC_RDATAL[7:0]						
R/W	11	of com						
Reset value	3		. (1	Joya	9.77		<u>_</u>	DAG. 150

Bit number	Bit symbol	Description the Description
3~0	ADC_RDATAH[3:0]	ADC scan result register
7~0	ADC_RDATAL[7:0]	ADC scan result register

#### 13.1.5. ADC Interrupt Register

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	_	EX4	EX3	EX2	_	_
R/W	N/W	R/W	_	R/W	N/W	R/W	_	- 00
Reset value	0.20	0	-	12/0.	0.20	0		27/g. 60
	70.0				27.2		((	

Bit number	Bit symbol	ing. M.J.	Description	sing. M. M.
4 9 1 9	EX4	ADC interrupt enable		1052-0, BAD

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1: ADC interrupt enable; 0: ADC interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	_	IE4	IE3	IE2	_	-
R/W	R/W	R/W	_	R/W	R/W	R/W	_	_
Reset value	0	0	_	0	0	0	-	-

Bit number	Bit symbol	Description
4	IE4	ADC interrupt flag
~~	$\mathcal{O}$	1: ADC interrupt flag is present;
-1-1/d. co,	0.35	0: ADC interrupt flag is cleared

IPL1 (F6H) Interrupt priority register1

Bit number	7	6	ng.5		3	2	ng. P	0
Symbol	IPL1.7	IPL1.6	5.00	IPL1.4	IPL1.3	IPL1.2	0000	NBID.
R/W	R/W	R/W		R/W	R/W	R/W		_
Reset value	0	0	_	0	0	0	_	_

Bit number	Bit symbol	Description
4	IPL1.4	ADC interrupt priority
		0: ADC is low priority;
		1: ADC is high priority

#### 13.2. ADC Secondary Bus Register

# 13.2.1. ADC Function Selection Register (16.58.3)

13.2. ADC Secondary Bus Register  13.2.1. ADC Function Selection Register										
ADC_IO_SEL0 (2AH) ADC function selection register 0										
Bit number	7	6	5	4	3	2	1	0		
Symbol	_			ADC	IO_SEL0	[6:0]				
R/W	_		R/W							
Reset value	_				0					

Bit number	Bit symbol	Description
6~0		Enable the ADC control function that disables analog input pins  1: Select ADC function;
		0: Not select ADC function
BID		0000001=ADC0; 0000010=ADC1; 0000100=ADC2; 0001000=ADC3; 0010000=ADC4; 0100000=ADC5;

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	1/10-		1.1		1(10-		( ) )	1,00		
pen W 10	,50		100000	0=ADC6			pente of 10.2			
ADC IO SEL1	DC IO SEL1 (53H) ADC select enable register 1							ning of O - VI		
Bit number	7	6	73/2	84	3	2	J. 177	80		
Symbol		ADC IO SEL1 [7:0]								
R/W		R/W								
Reset value				(	0					

Bit number	Bit sy	mbol			Descr	Description				
7~0	ADC_IO	D_SEL1 :0]	Enable the ADC control function that disables analog it pins  1: Select ADC function;  0: Not select ADC function  00000001=ADC7; 00000010=ADC8;  00000100=ADC9; 00001000=ADC10;  00010000=ADC11; 00100000=ADC12;  01000000=ADC13; 10000000=ADC14					og input		
ADC IO SEL2	(54H) AD	C select e	nable regis	ter 2						
Bit number	7	6	5	4	3	2	1	0		
Symbol		ADC_IO_SEL2 [7:0]								

Bit number	7	6	5	4	3	2	1	0	
Symbol		ADC_IO_SEL2 [7:0] R/W							
R/W									
Reset value		0							

	Bit number	Bit symbol	Description
3	ben abyd. co.	ADC_IO_SEL2 (7:0]	Enable the ADC control function that disables analog input pins  1; Select ADC function;  0: Not select ADC function  00000001=ADC15; 00000010=ADC16;  00000100=ADC17; 00001000=ADC18;  00010000=ADC19; 00100000=ADC20;  01000000=ADC21; 10000000=ADC22

ADC\_IO\_SEL3 (55H) ADC select enable register 3

Bit number	7	6	5	3	2	1	0	
Symbol	ADC_IO_SEL3[7:0]							
R/W	R/W							
Reset value	$r = \frac{1}{1} \cos \theta$							

Bit number	Bit symbol	Description	pen(a) 10:3
020,040	ADC_IO_SEL3	Enable the ADC control function that	disables analog input
1/2 /~00	[7:0]	pins	

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(1) (1) (1) (1) (1) (1) (1) (1) (1) (1)		
a pena 11/0/20	1: Select ADC function;	
305-01-0	0: Not select ADC function	
	00000001=ADC23; 00000010=ADC24;	
	00000100=ADC25; 00001000=ADC26;	
	00010000=ADC27; 00100000=ADC28;	
	01000000=ADC29; 10000000=ADC30	

ADC IO SEL4 (56H) ADC select enable register 4

Bit number	7	6	5	4	3	2	1	0		
Symbol		ADC_IO_SEL4 [7:0]								
R/W		R/W								
Reset value	)									

		. () • () )			U.
	Bit number	Bit symbol	262(0) 1 16:20	Description	5
200	025-07-01	<b>'</b>	Enable the ADC continuing pins  1: Select ADC function	rol function that disables analog input	
	7~0	ADC_IO_SEL4	0: Not select ADC fur	ection	
	/~0	[7:0]	00000001=ADC31;	00000010=ADC32;	
			00000100=ADC33;	00001000=ADC34;	
			00010000=ADC35;	00100000=ADC36;	
			01000000=ADC37;	10000000=ADC38	

ADC IO SEL5 (57H) ADC select enable register 5

	ADC 10 BEES (5/11) ADC Scient chaole register 5										
	Bit number	7	6	5	4	3	2	1	0		
	Symbol O	_	_	_	y con	ADC	_IO_SEL5	[4:0]	y com		
	R/W	_	_	- ~(0	plan		R/W	$\sim$ (0)	2.5		
5	Reset value	_		o perio			0	o perio	1/ 10.		

Bit number	Bit symbol	Description			
7~5		Reserved			
4~0	ADC_IO_SEL5 [4:0]	Enable the ADC control function that disables analog input pins  1: Select ADC function;  0: Not select ADC function  00001=ADC39; 00010=ADC40;  00100=ADC41; 01000=ADC42;  10000=ADC43;			



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## 13.2.2. Module Switch Control Register

PD ANA (2DH) Module switch control register

Bit number	7	6	5	4	3~1	0
Symbol	_	PD_LVDT	_	PD_XTAL_32K	ı	PD_ADC
R/W	_	R/W	_	R/W	-	R/W
Reset value	_	1	_	1	1	1

Bit number	Bit symbol	Description
		Analog ADC shutdown control register
0	PD_ADC	0: ADC module works normally;
		1: ADC module does not work

#### 13.2.3. ADC Configuration Register

ADC CFG SEL (32H) ADC configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	ADCWNUM ADC I SEL						I_SEL
R/W	_	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	_	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
6~2	ADCWNUM	Selection of distance conversion interval time after sampling: (3+ADCWNUM)*TADCK
1	ADC_I_SEL[1]	ADC select comparator bias current,  1: 4 μA;  0: 5 μA
0	ADC_I_SEL[0]	ADC select buffer bias current,  1: 4 μA;  0: 5 μA

#### 13.2.4. ADC Comparator Offset Cancellation Selection Register

ADC CFG SEL1 (42H) ADC comparator offset cancellation selection register

Bit number	7	6	5	4
Symbol	_	-	ADC_VREF_SEL	ADC_VREF_VOL_SEL
R/W	0.35	_	R/W	R/W
Reset value	26.3°	- 1.05	(0)	0,000
Bit number	3	:20.	1	ing. O M
Symbol	VREF_IN_	ADC_SEL	C BYD	TRL_SEL ON BY

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	1(10-			
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	1	0,0,0

Bit number	Bit symbol	Description			
	ADC VDEE CEL	ADC reference voltage selection:  0: Select VCC as the output signal;			
5	ADC_VREF_SEL	1: Select the voltage output by the ADC_VREF module as the reference voltage.			
4	ADC_VREF_VOL_SEL	ADC_VREF output mode selection: 0: 2V as ADC reference voltage; 1: 4V as ADC reference voltage. When ADC_VREF output mode is 2V/4V, it is recommended to select 3MHz for ADC frequency division clock			
3~2	VREF_IN_ADC_SEL	Voltage selection input to the internal ADC channel of the chip 00: 1.362V; 01: 2.253V; 10: 3.111V; 11: 4.082V;			
1~0	CTRL_SEL	ADC offset elimination timing selection, the default value is 10: 00/01: first offset elimination and then sampling; 10/11: offset elimination and sampling are performed at the same time, 10 first-stage comparator switches are turned off at the end; 11: all switches are turned off at the same time			

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#### 13.3. ADC Important Point

Timing requirements: (3+ADCWNUM) \*TADCK >4\*TADCK

ADCK: ADC clock 8 MHz/6 MHz/4 MHz/3MHz;

ADCCKV: ADC comparator offset cancellation analog input clock 12 MHz/8 MHz/4 MHz/2 MHz;

Voltage settling time after ADC input signal plus RC filter>= 2\*(ADC conversion time);

ADC conversion time:

formula	Description
$t_{ADC} = t_1 + t_2 + t_3 + 200 \text{ns}$	ADC detection time
$t_1 = 4*(ADC\_SPT+1) *TADCK$	ADC sampling time
t2=( ADCWNUM+3+SAMDEL)*TADCK	Distance conversion interval time after sampling
t <sub>3</sub> =( 2*1+12)*T <sub>ADCK</sub>	Sampling delay time

1. ADC\_SPT: ADC sampling time configuration register (ADC\_SPT=0~255). SAMDEL: Sampling delay time selection (SAMDEL=0: 0; 1: 2; 2: 4; 3: 8).

2. When selecting VCC as the ADC reference voltage, when the power supply voltage

fluctuates greatly or drops, the VCC voltage value can be inversely calculated by the formula ADCINNER\_Data/ VREF\_IN\_ADC\_SEL = 4096/VCC, and the Vin voltage value can be inversely calculated by the formula Vin Data/Vin=4096/VCC.

ADCINNER Data: ADC internal channel data;

Vin Data: ADC input channel data;

Vin: Input voltage;

VREF IN ADC SEL: Need to read the chip calibration value,

Vin = (Vin\_Data/ADCINNER\_Data)\*VREF\_IN\_ADC\_SEL, VREF\_IN\_ADC\_SEL needs to read the chip calibration value, first obtain the internal channel data, and then obtain the input voltage Vin\_Data data, and the interval between two data acquisitions should be as short as possible;

When ADC\_VREF\_VOL\_SEL 2V/4V reference voltage is selected, It is recommended to select 3MHz for ADC frequency division clock, The voltage value of Vin can be inversely calculated by the formula Vin Data/Vin=4096/ADC VREF VOL SEL.

Vin Data: ADC input channel data;

Vin: Input voltage (0~ADC VREF VOL SEL);

VREF IN ADC SEL: Need to read the chip calibration value,

Vin = (Vin\_Data/ADCINNER\_Data)\*VREF\_IN\_ADC\_SEL, ADC\_VREF\_VOL\_SEL needs to read the chip calibration value, Get the internal channel data first, then get the input voltage Vin\_Data data, The interval between two data acquisitions should be as short as possible;

3. ADC input interrupt conditions: The configuration sequence is ADC\_IO\_SEL enable->ADC interrupt enable->ADC\_ADDR(Address and ADC\_IO\_SEL must correspond)-> ADC\_START, Note on initial configuration timing during application. If there is an application where ADC and IO port functions are multiplexed, you need to pay attention to the switching timing, If ADC\_IO\_SEL is enabled or disabled or Address does not correspond to ADC\_IO\_SEL, ADC scanning cannot be turned on, and the configuration sequence must be

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followed: ADC\_IO\_SEL enable->ADC interrupt enable->ADC\_ADDR(Address and ADC\_IO\_SEL must correspond) >ADC\_START, to enable ADC scan

4. {SPROG\_ADDR\_H, SPROG\_ADDR\_L}= [0x41CA] ADC internal channel input voltage calibration value high eight bits,

{SPROG\_ADDR\_H, SPROG\_ADDR\_L}= [0x41CB] ADC internal channel input voltage calibration value low eight bits,

Read the 1.362V calibration value of the chip's information address ADC internal channel input voltage;

 $\{SPROG\_ADDR\_H, SPROG\_ADDR\_L\} = [0x41CC]$  ADC internal channel input voltage calibration value high eight bits,

{SPROG\_ADDR\_H, SPROG\_ADDR\_L}= [0x41CD] ADC internal channel input voltage calibration value low eight bits,

Read the chip information address ADC internal channel input voltage 2.253V calibration value;

{SPROG\_ADDR\_H, SPROG\_ADDR\_L}= [0x41CE] ADC internal channel input voltage calibration value high eight bits,

{SPROG\_ADDR\_H, SPROG\_ADDR\_L}= [0x41CF] ADC internal channel input voltage calibration value low eight bits,

Read the chip information address ADC internal channel input voltage 3.111V calibration value;

{SPROG\_ADDR\_H, SPROG\_ADDR\_L}= [0x41D0] ADC internal channel input voltage calibration value high eight bits,

{SPROG\_ADDR\_H, SPROG\_ADDR\_L}= [0x41D1] ADC internal channel input voltage calibration value low eight bits,

Read the chip information address ADC internal channel input voltage 4.082V calibration value;

{SPROG\_ADDR\_H, SPROG\_ADDR\_L}= [0x41D2] ADC\_VREF 2V voltage calibration value high eight bits,

{SPROG\_ADDR\_H, SPROG\_ADDR\_L}= [0x41D3] ADC\_VREF 2V voltage calibration value low eight bits,

Read the calibration value of the chip information address ADC Vref2V;

{SPROG\_ADDR\_H, SPROG\_ADDR\_L}= [0x41D4] ADC\_VREF 4V voltage calibration value high eight bits,

{SPROG\_ADDR\_H, SPROG\_ADDR\_L}= [0x41D5] ADC\_VREF4V voltage calibration value low eight bits,

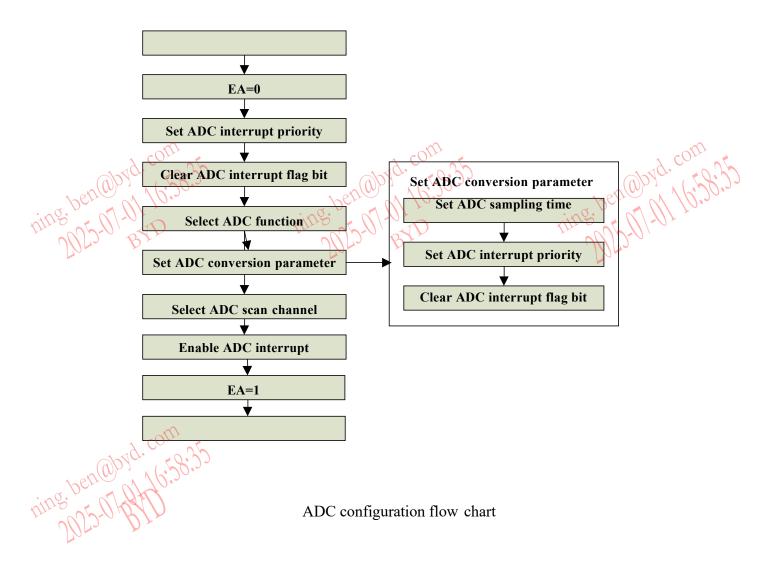
Refer to Chapter 3 to read Flash information steps.

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5. When the pin is configured as ADC function, the pin needs to be configured as 10 input mode, and other multiplexing functions are turned off, such as pull-up resistors, etc.

#### 13.4. ADC Configuration Process



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The BF7515CM44-LJTX series supports low voltage alarm function, which can effectively monitor the dynamic changes of voltage. Support 8 voltage levels, respectively:

2.7V/3.0V/3.3V/3.6V/3.8V/4.0V/4.2V/4.4V (preset point step-down interrupt, hysteresis 0.1V generates corresponding step-up interrupt). When the voltage monitoring is configured with the above threshold, the voltage drop to this threshold will trigger a low-voltage interrupt, and the system can handle the low-voltage interrupt appropriately according to application needs.

#### 14.1. LVDT Related Registers

	SFR register (3)							
A	ddress	Name	RW	Reset	Description (1)			
g. Ž	0xD5	INT_POBO_STAT	RW	xxxx_xx00b	LVDT Boost/Buck interrupt status register			
00	0xE1	IRCON2	RW	0000_0000ь	Interrupt flag register 2			
	0xE7	IEN2	RW	0000_0000b	Interrupt enable register 2			
	0xF4	IPL2	RW	0000_0000ь	Interrupt priority register2			

LVDT SFR register list

Secondary bus register							
Address	Name	RW	Reset	Description			
0x2C	SEL_LVDT_VTH	RW	xxxx_x000b	LVDT threshold selection register			
0x2D	PD_ANA	RW	x111_xx11b	Analog module switch register			
0x65 SEL_LVDT_DELAY RW xxxx_xx00b LVDT delay control register							
LVDT secondary bus register list							
1 1 16:20.2							
14.1.1. LVDT Boost/Buck Interrupt Status Register							
INIT DODO	STAT (D5H) I VDT Door	st/buole i	interrupt status r	agistar			

#### 14.1.1. LVDT Boost/Buck Interrupt Status Register

INT POBO STAT (D5H) LVDT Boost/buck interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	INT_PO_STAT	INT_BO_STAT
R/W	_	_	_	_	_	_	R/W	R/W
Reset value	_	_	_	_	_	_	0	0

	Bit number	Bit symbol	Description
	2 co	DIT DO STAT	LVDT boost interrupt status.
	OBJO.	INT_PO_STAT	1: Boost interrupt is valid; 0: Boost interrupt is invalid.
α .	belle		LVDT buck interrupt status.
9	08///	INT_BO_STAT	1. The buck interrupt is valid;
			0: The buck interrupt is invalid

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	7 60	705				20	BF/	313CM	44-LJ1X	<u> </u>
76	<b>14.1.2. Inter</b>	2025-	57.01 16:5	6.						
	Bit number	7	6	5	4	3	2	1	0	
	Symbol	IE15	IE14	IE13	IE12	IE11	IE10	IE9	IE8	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	Reset value	0	0	0	0	0	0	0	0	

Bit number	Bit symbol	Description
		LVDT interrupt flag
0	IE8	1: With LVDT interrupt flag
		0: Clear LVDT interrupt flag

#### 14.1.3. Interrupt Enable Register 2

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	EX15	EX14	EX13	EX12	EX11	EX10	EX9	EX8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description		
		LVDT interrupt enable		
0	EX8	1: LVDT interrupt enable;		
		0: LVDT interrupt disable		

#### 14.1.4. Interrupt Priority Register2

IPL2 (F4H) Interrupt priority register2

= == (1 :11) 111v111vp v p11011vj 10818v11=									
Bit number	7	6	5	4	3	2	1	0	
Symbol	IPL2.7	IPL2.6	IPL2.5	IPL2.4	IPL2.3	IPL2.2	IPL2.1	IPL2.0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	0	0	0	0	

Bit number	Bit symbol	Description
		LVDT priority selection bit.
0	IPL2.0	1: LVDT interrupt is high priority;
		0: LVDT interrupt is low priority

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#### 14.2. LVDT Secondary Bus Register

#### 14.2.1. LVDT Threshold Selection Register

SEL LVDT VTH (2CH) LVDT threshold selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	SE	L_LVDT_`	VTH
R/W	_	_	_	_	_	R/W	R/W	R/W
Reset value	_	_	_	_	_	0	0	0

	Bit number	Bit symbol	Description
4	ben Obyd. Co		LVDT threshold selection, the corresponding threshold is shown in the table "Threshold and Delay Selection"
ક		ζ.	000=2.7V; 001=3.0V; 010=3.8V;
	2~0	SEL_LVDT_VTH	010=3.8 V; 011=4.2 V; 100=3.3 V;
			101=3.6V;
			110=4.0V; 111=4.4V

#### 14.2.2. Module Switch Control Register

PD ANA (2DH) Module switch control register

	Juliodale Switt	ch common regi	Stor (			
Bit number	7	6 50	0.00 \$ 10:2	4	3~1	J. (0) / (1)
Symbol	-	PD_LVDT	$\mathcal{U}_{i,n}$	PD_XTAL_32K	ung.	PD_ADC
R/W	_	R/W	<u>-</u>	R/W	J//	R/W
Reset value	_	1	_	1	_	1

Bit number	Bit symbol	Description
		LVDT control register
6	PD_LVDT	1: Closed
		0: Open, closed by default

#### 14.2.3. LVDT Delay Control Register

SEL LVDT DELAY (65H) LVDT delay control register

ď,	Bit number	7	6.	2.3em	1/4/10.	3	2	og. Penic	1/0/0
	Symbol	-	<u>-</u>	71.60	N BAD	-	- <i>D</i>	2002	DY2
Ì	VII.			. 170				. 177	

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#### BF7515CM44-LJTX

	1110-							
OCO R/W	_	_	_	_	_	_	R/W	R/W
Reset value	_	_	_	_	-	_	050	0

Bit number	Bit symbol	Description
		Select signal, select LVDT power-down delay;
1~0	SEL_LVDT_DELAY	00: Delay time 1; 01: Delay time 2;
		10: Delay time 3; 11: Delay time 4

CEL LADT	CEL LUDT		LVDT		
SEL_LVDT_ VTH	SEL_LVDT   DELAY	Power down	Recovery	Hysteresis	Delay
VIII	_DELA I	threshold (V)	Recovery Hysteresis Delay		
abyd. ce	00	2.7 <u>aby</u> d.	2.8	124	7:9
Jen (0) 53 16:	01	2,70	2.8	125	14.9
000	10	in 82.7	2.8	125	29.1
1055-0	11	2.7	2.8	127	57.3
	00	3.0	3.1	117	8.7
001	01	3.0	3.1	117	16.5
001	10	3.0	3.1	118	32.3
	11	3.0	3.1	120	63.8
	00	3.8	3.9	123	10.2
010	01	3.8	3.9	123	19.6
010	10	3.8	3.9	124	38.5
	11	3.8	3.9	126	76.3
	00 01 10 11 00 01 10 11 00 01 11 00 01 11 00 01 11 00	4.2	4.3	124	10.8
011	01	4.2	4.3	125	20.7
011	10	4.2	4.3	126	40.8
Rin	11	4.2	4.3	128	80.8
	00	3.3	3.4	93	9.3
100	01	3.3	threshold (V)  2.7  2.8  124  7.9  2.7  2.8  125  2.9  2.7  2.8  127  2.8  127  2.7  2.8  127  2.7  2.8  127  2.7  3.0  3.1  117  3.0  3.1  117  16.1  3.0  3.1  118  32.2  3.0  3.1  110  3.8  3.9  123  10.2  3.8  3.9  124  38.2  3.8  3.9  124  38.2  3.8  3.9  125  10.2  4.2  4.3  126  4.2  4.3  126  4.2  4.3  126  4.2  4.3  126  4.2  4.3  127  3.8  3.9  127  3.8  3.9  128  80.8  3.9  129  120  121  121  120  120  121  120  123  120  123  124  125  126  127  127  128  129  129  120  120  121  120  121  120  122  123  124  125  126  126  127  127  127  128  128  128  128  128	17.7	
100	10	3.3	3.4	94	34.8
	11	3.3	3.4	95	68.7
	00	3.6	3.7	3.9     123     19.6       3.9     124     38.5       3.9     126     76.3       4.3     124     10.8       4.3     125     20.7       4.3     126     40.8       4.3     128     80.8       3.4     93     9.3       3.4     94     17.7       3.4     94     34.8       3.4     95     68.7       3.7     109     9.8       3.7     110     18.8       3.7     111     37       3.7     113     73.2       4.1     135     10.5	
101	01	3.6	3.7	110	18.8
101	10	3.6	3.7	111	37
	11	3.6	3.7	113	73.2
	00	4.0	4.1	135	10.5
110	01	4.0	4.1	136	20.1
110	10	4.0	4.1	137	39.7
	11	4.0	4.1	139	78.6

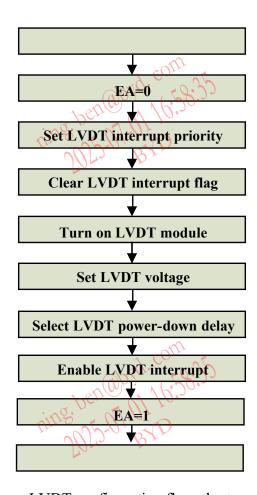
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Opia, Co	8:33				
pen 01 10	00	4.4	4.5	83	11.1
0501-0	01	4.4	4.5	83	21.3
111	10	4.4	4.5	84	41.9
	11	4.4	4.5	68	82.8

Threshold and delay selection

### 14.3. LVDT configuration process



LVDT configuration flow chart

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15. LED/LCD

The module can be configured with three drive modes: LED matrix drive mode, LED dot matrix drive mode, LCD drive mode. Through register configuration, only one mode of operation is supported at the same time.

All of the above driving methods, the total IO port switch is configurable, the scanning mode is configurable, the software controls the LED scanning to start, the interrupt mode scanning once interrupts and stops, and the cycle mode automatically starts the next frame scanning after one frame is scanned, without interruption If you want to stop, you need to turn off the scan enable by the software. When the scan enable is turned off, all states of the module are reset. Including LED controller and LCD controller.

#### 15.1. LED Dot Matrix Driver

Features of LED dot matrix drive mode:

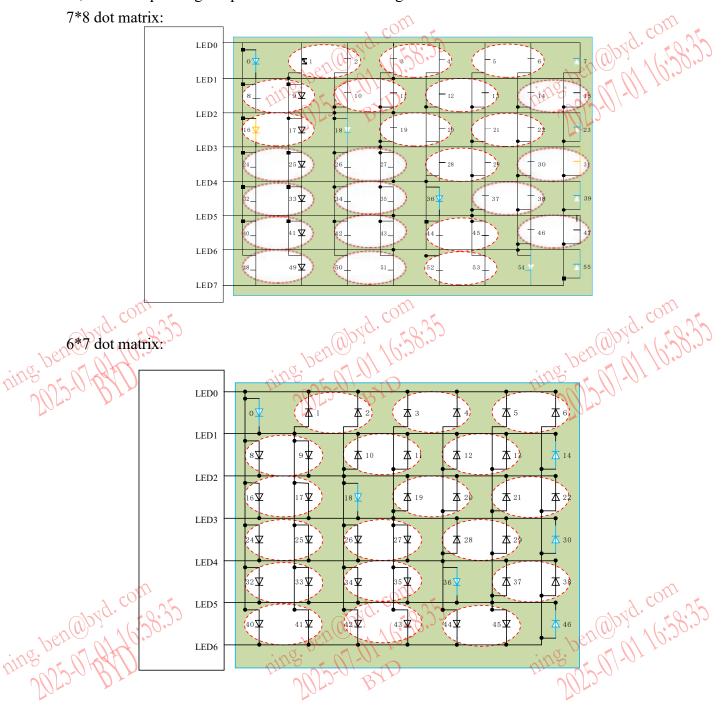
- Supports up to 56 lights LED drive, configurable to choose matrix 4\*5, 5\*6, 6\*7, 7\*8, of which matrix 4\*5 supports two IO enable;
- Dual lamps are turned on at the same time, the specific distribution is shown in the dot matrix description below;
- Single lamp on-time setting file: 8-bit register, configurable range is 16μs-4.096ms, step is 16μs;
- Each lamp driving time is individually selectable;
- IO ports have multiple multiplexing relationships. Each IO port needs to be configured through software to switch to LED port. According to the LED dot matrix mode selection, the LED function of LED0~LED7 corresponding to IO port will be automatically turned on. The starting port LED0 supports the selection of PB0~PB7. Other mouth sequence circulation;
- <sup>1</sup> 56 light dot matrix Address is unique, see the dot matrix description below, used to input switch light information;

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#### 15.1.1. DED Dot Matrix Description

16. The LED dot matrix is a universal 7\*8 dot matrix, and uses the dual lamp mode, that is, two lamps are lit at a time (common cathode). Corresponding to LED0~LED7 ports, up to 7x8=56 lamps can be configured to drive. The lamp address of the corresponding position is marked in the 7\*8 dot matrix in the figure below. The display configuration in the SRAM corresponds to the lighting condition of the corresponding address (1 means lighting, 0 means no light), the hardware code needs to analyze the light address and the current scan address to automatically complete the corresponding IO port output control. Configurable dot matrix 4\*5, 5\*6, 6\*7, 7\*8, different size dot matrix, the corresponding lamp address remains unchanged.

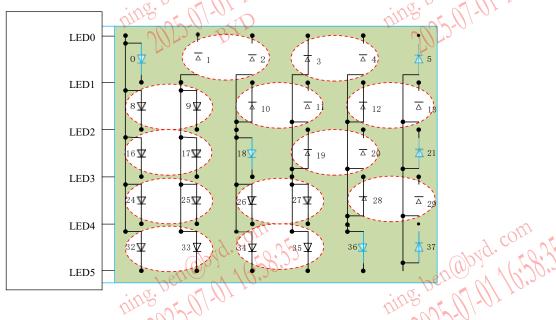


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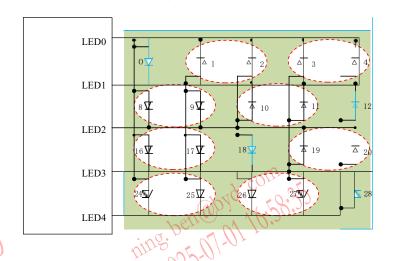
2025-07-07-16:58:35



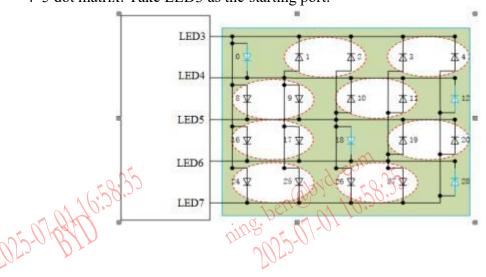
ning 5\*6 dot matrix:



4\*5 dot matrix: Take LED0 as the starting port:



4\*5 dot matrix: Take LED3 as the starting port:

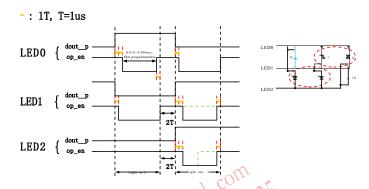


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Dot matrix scan timing example:

Take lighting 0, 1, 2 as an example, the detailed digital output interface control sequence is shown in the figure below:



Note:

LED scanning timing diagram

The starting port LED0 of the series can choose the specific position of the PAD, and DITA SELISI DI

DULY SELLZE 9.				
LED_IO_START	dot matrix	25 01 01 10.	order	105. pc. v. 1 1 10.
W2-0.81D	7*8 <sup>5</sup>	$PB 0 \rightarrow PB 1 \rightarrow PB 2$	$\rightarrow$ PB3	$\rightarrow$ PB4 $\rightarrow$ P B5 $\rightarrow$ P
000 PD0	6*7	$PB 0 \rightarrow PB 1 \rightarrow PB 2$	$\rightarrow$ PB3	$\rightarrow PB4 \rightarrow PB5 \rightarrow P$
000 PB0	5*6	$PB 0 \rightarrow PB 1 \rightarrow PB 2$	$\rightarrow$ PB3	$\rightarrow$ PB4 $\rightarrow$ P B5
	4*5	$PB 0 \rightarrow PB 1 \rightarrow PB 2$	$\rightarrow$ PB3	→PB4
	7*8	$PB 1 \rightarrow PB 2 \rightarrow PB 3$	$\rightarrow$ PB4	$\rightarrow PB5 \rightarrow PB6 \rightarrow P$
001 PD1	6*7	$PB 1 \rightarrow PB 2 \rightarrow PB 3$	$\rightarrow$ PB4	$\rightarrow PB5 \rightarrow PB6 \rightarrow P$
001 PB1	5*6	$PB 1 \rightarrow PB 2 \rightarrow PB 3$	→PB4	$\rightarrow$ PB5 $\rightarrow$ P B6
	4*5	$PB 1 \rightarrow PB 2 \rightarrow PB 3$	$\rightarrow$ PB4	→PB5
	7*8	$PB 2 \rightarrow PB 3 \rightarrow PB 4$	$\rightarrow$ PB5	$\rightarrow PB6 \rightarrow PB7 \rightarrow P$
010 PP2	6*7	$PB 2 \rightarrow PB 3 \rightarrow PB 4$	$\rightarrow$ PB5	$\rightarrow PB6 \rightarrow PB7 \rightarrow P$
010 PB2	5*6	$PB 2 \rightarrow PB 3 \rightarrow PB 4$	$\rightarrow$ PB5	$\rightarrow$ PB6 $\rightarrow$ PB7
	4*5	$PB 2 \rightarrow PB 3 \rightarrow PB 4$	$\rightarrow$ PB5	→PB6
(Va		and so on		

LED dot matrix drive LEDX arrangement order

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#### 15.1.2. Display Configuration Address

LED dot matrix drive mode corresponding to display configuration:

DX indicates whether the light is selected or not, 0: not bright, 1: bright;

Dx\_SEL indicates that the light is selected for the lighting cycle, 0: select the first segment of the

light cycle, 1: select the second segment of the light cycle.

Address	7	6	5	4	3	2	1	0
1000H	D7	D6	D5	D4	D3	D2	D1	D0
1001H	D15	D14	D13	D12	D11	D10	D9	D8
1002H	D23	D22	D21	D20	D19	D18	D17	D16
1003H	D31	D30	D29	D28	D27	D26	D25	D24
1004H	D39	D38	D37	D36	D35	D34	D33	D32
1005H	D47	D46	D45	D44	D43	D42	D41	D40
1006H	D55	D54	D53	D52	D51	D50	D49	D48
1007H	D7_SEL	D6_SEL	D5_SEL	D4_SEL	D3_SEL	D2_SEL	D1_SEL	D0_SEL
1008H	D15_SEL	D14_SEL	D13_SEL	D12_SEL	D11_SEL	D10_SEL	D9_SEL	D8_SEL
1009H	D23_SEL	D22_SEL	D21_SEL	D20_SEL	D19_SEL	D18_SEL	D17_SEL	D16_SEL
100AH	D31_SEL	D30_SEL	D29_SEL	D28_SEL	D27_SEL	D26_SEL	D25_SEL	D24_SEL
100BH	D39_SEL	D38_SEL	D37_SEL	D36_SEL	D35_SEL	D34_SEL	D33_SEL	D32_SEL
100CH	D47_SEL	D46_SEL	D45_SEL	D44_SEL	D43_SEL	D42_SEL	D41_SEL	D40_SEL
100DH	D55_SEL	D54_SEL	D53_SEL	D52_SEL	D51_SEL	D50_SEL	D49_SEL	D48_SEL

LED dot matrix drive mode corresponding display configuration table

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#### 15.1.3. LED Dot Matrix Register

J. B.		3	SFR register	7073 B
Address	Name	RW	Reset	Description
0xAE	INT_PE_STAT	RW	0000_0000Ь	Interrupt status register
0xAF	SCAN_START	RW	xxxx_xxx0b	LCD, LED scan on register
0xB1	DP_CON	RW	x000_0000b	LCD, LED control register
0xB2	DP_MODE	RW	0000_0000Ь	LCD, LED mode register
0xB3	SCAN_WIDTH	RW	0000_0000Ь	LED cycle configuration register
0xB4	LED2_WIDTH	RW	0000_0000ь	LED dot matrix drive mode cycle configuration register
0xE6	IENI N	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register1

	Secondary bus register									
Address	Name	RW	Reset	Description						
0x31	LED_DRIVE	RW	xxxx_0000b	LED port drive capability configuration register						
0x58	LED_IO_START	RW	xxxx_x000b	LED scan start selection register						

#### 15.1.3.1. LED Scan on Register

	SCAN START	Ur OZ	D, LED s	can on reg	isterd. cor	8:32		(1)	byd. com
Υ .	Bit number	7	6	5 pen	1/0	3	2	Device	0/0/0.
ع ح	Symbol	_	_ <	TINE OF	1/-0,	_	_ %	TUS OF	
(	R/W	_	_	J7772	ı	-	_	0/1/2	R/W
	Reset value	_	_	_	-	_	_	-	0

Bit number	Bit symbol	Description			
		LCD, LED scan on register			
0		1: Scan on; 0: Scan off			

#### 15.1.3.2. LED Control Register

DP CON (B1H) LCD, LED control register

R	2576011 (D444)	LVL	, LLD COII	10110519101	
	Da. 1170				
í L	Ditmumban	7	6	5. KAY   2\\\\ 2	1
7	Bit number	/	U	Jan 24   12   10   1	
4	~ (			1	
0			$\mathbf{IO}$ $\mathbf{ONI}$	DITY SEL DESEL	SCAN MODE COM MOD
1	Symbol		IO ON	DUNISEL DPSEL	SCAN MODE COM MOD
		_			

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1106, 12	100								
R/W	_	R/W		R/W		R/W	R/W	R/W	0
Reset value	_	0	0	0	0	0	0	0500	

Bit number	Bit symbol	Description
6	IO_ON	LCD/LED scanning corresponds to the total control bit of all IO ports 0: Close IO; 1: Open IO
5~3	DUTY_SEL	LED dot matrix drive mode dot matrix selection configuration register  Bit[1:0]: 00: 4x5 lattice; 01: 5x6 lattice;  10: 6x7 lattice; 11: 7x8 lattice  Bit [2]: 0: Take LED0 as the starting port  1: 4x5 dot matrix-LED3  (as the starting port to enable)
2	DPSEL	LCD, LED select control bit  0: Select LCD driver, LED driver is invalid  1: Select LED driver, LCD driver is invalid
1	SCAN_MODE	LCD, LED scan mode configuration  1: Cyclic scan mode;  0: Interrupt scan mode
0	COM_MOD	High-current IO port driver enable  1: COM port function is locked and works as a high-current IO port;  0: COM port function is not locked and can be configured as other functions;  When used as a high current sink IO port, by configuring the GPIO register to output the drive timing, the LED/LCD scan configuration is invalid

#### 15.1.3.3. LED Mode Register

DP\_MODE (B2H) LCD, LED mode register

DI_MODE (DE	ii) Leb, LLD i	11046 165	15001					
Bit number	mber 7 6 5		5	4	3 2		1	0
Symbol	LED_MOD	LCD_CKSEL		LCD_RSEL	LCD_FCSEL		LCD_RMOD	
R/W R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0 25 0	0	0	vd. 00.35	0	0	0	12.8

Bit number	Bit symbol	Description	ing. or of the
702-761	LED_MOD	LED drive mode selection register	Mrs ODD-U BYD

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1: Serial dot matrix scanning
0: Row and column matrix scan

#### 15.1.3.4. LED Period Configuration Register

SCAN WIDTH (B3H) LED period configuration register

Bit number	7	6	5	4	3	2.	1	0
Symbol	, 5 5 . 5							
R/W	R/W							
Reset value	0							

	Bit number	Bit symbol	Description
5	05-07-07		In the LED dot matrix drive mode, the corresponding single lamp lighting time configuration register-the first segment of the lamp
	7~0		cycle configuration: period=(scan_width+1)*16us, the support
			configuration range is 0.016~4.096ms; When on-time 1 <on-time 2,="" 2.<="" group="" is="" of="" on-time="" scan="" td="" the="" this="" time=""></on-time>

LED2 WIDTH (B4H) LED dot matrix drive mode cycle configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	_							
R/W	R/W							
Reset value		Q						

Bit number Bit symbol	Description
berroll	In the LED dot matrix drive mode, the corresponding single
2020 810	lamp lighting time configuration register-the second stage of
	lamp cycle configuration
7~0	Period = (led2_width+1)*16us
	Note: This register is only applicable to LED dot matrix
	drive mode: when the on time 1 is greater than the on time 2,
	the scan time of this group is on time 1.

#### 15.1.3.5. LED Interrupt Register

INT\_PE\_STAT (AEH) Interrupt status register

	Bit number	7	1-006, 16:20.	5	1004 165
Į,	Symbol	INT_PWM1_STA	AT UNT TIMERS STAT	INT08_STAT	INT_WDT_STAT
	R/W	R/W	N/R C	R/W	W/N C

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(0)	70.5	$(0)_{\Sigma}$ , $(2)_{\Sigma}$	<i>-</i>	$(U)_{\Sigma}$ , $(V)_{\Sigma}$
Reset value	0	pena di 10.2	0	pen on 10.3
Bit number	3 nit	2	1 hin	0,000
Symbol	INT_TIMER2_STAT	NT_PWM0_STAT	INT_LCD_STAT	INT_LED_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
0	INT_LED_STAT	LED interrupt status flag, write 0 to clear this bit, write SCAN_START operation can also be cleared 1: Interrupt is valid; 0: Interrupt is invalid

IEN1 (E6H) Interrupt enable register 1

Bit number	0.25	6	5	4.	3	2	1 _	200 C
Symbol	EX7	EX6	hen	EX4	EX3	EX2	hen(	00,1-10:0
R/W	R/W	R/W	126.	RW	R/W	R/W	128.	11/1/
Reset value	0	0	1055	0	0	0	JU 3.	7,

Bit number	Bit symbol	Description
		LED/LCD interrupt enable
6	EX6	1: LED/LCD interrupt enable;
		0: LED/LCD interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	_	IE4	IE3	IE2	_	- 🔊
R/W	R/W	R/W	_	RXW <sup>O</sup>	R/W	R/W	_	y com
Reset value	26.9	0	0	0,0	26:33	0	- 20	77.

Bit number	Bit symbol	Description Description
		LED/LCD interrupt flag
6	IE6	1: With LED/LCD interrupt flag
		0: Clear LED/LCD interrupt flag

IPL1 (F6H) Interrupt priority register1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	_	IPL1.4	IPL1.3	IPL1.2	_	_
R/W	R/W	R/W	_	R/W	R/W	R/W	_	_
Reset value	0	0	_	0	0	0	_	_

	1 10
Bit number Bit symbol	abyd. 28.3 Description abyd. 29
penta 170.30	LED/LCD interrupt priority bit
IPL1.6	1: LEDACO interrupt is high priority;
J ( ) 2 D 1 .	0: LED/LCD interrupt is low priority

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#### 15.1.4. Secondary Bus Register

#### 15.1.4.1. LED Port Drive Capability Configuration Register

LED DRIVE (31H) LED port drive capability configuration register

, _ , ,	222 21d (2 (0111) 222 poil will (0 tupuolill) collinguiumon regional							
Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_			_	
R/W	_	_	_	_	R/W	R/W	R/W	R/W
Reset value	_	_	_	_	0	0	0	0

Bit number	Bit symbol	Description					
3,00	<del></del>	For details, please refer to LED serial dot matrix drive current description					
15 1 4 2 LED	Coor Stout Sol	ing period in the					
15.1.4.2. LED Scan Start Selection Register							
LED TO START(58H) LED scan start selection register							

#### 15.1.4.2. LED Scan Start Selection Register

LED IO START(58H) LED scan start selection register

 EED 10 511 Met (5011) EED seam start selection register								
Bit number	7	6	5	4	3	2	1	0
Symbol	_	_	_	_	_	_	_	_
R/W	_	_	_	-	_	R/W	R/W	R/W
Reset value	_	_	_	_	_	0	0	0

Bit number	Bit symbol	Description
		LED port serial dot matrix start PAD selection (only for
		LED serial dot matrix scan, and DUTY_SEL[2] needs to be configured to 0)
OVa		000: PB0 port;
Pir		001: PB1 port;
		010: PB2 port;
2~0		011: PB3 port;
		100: PB4 port;
		101: PB5 port;
		110: PB6 port;
		111: PB7 port;
		See the table "LED dot matrix drive LEDX arrangement order"

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#### 15.1.5. LED Serial Dot Matrix Drive Current Description

7 502	05	BF/313CM44-LJ1X
1.5. LED Serial Dot Ma	trix Drive Current Description	2025-07-01 16:58
(Ta =, VC2C7= <b>T</b> V, LEI	D lamp voltage drop 1.8V~2.3V)	2022-01-01
LED_DRIVE	Ifp(mA)	
0	4	
1	10	
2	16	
3	20	
4	26	
5	31	
6	36	
7	41	
8	46	
9	51	
10	55	
11	60	
12	65	
13	69	
14	74	
15	78	

LED secondary bus drive current configuration register reference list

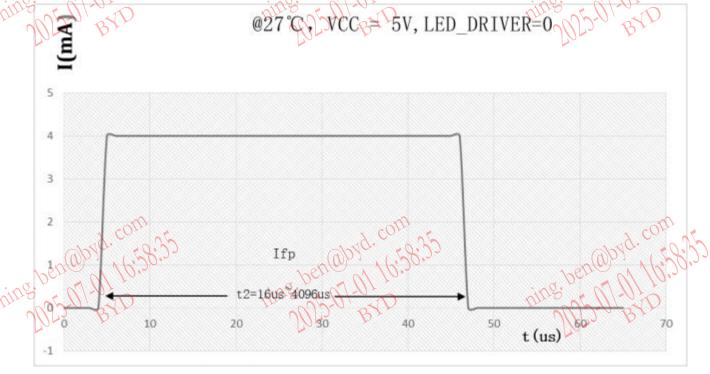
#### Note:

- LED drive current deviation range (±8%)@VCC=5V,Ta=(-40°C~105°C), the setting of LED DRIVE is recommended to be less than the nominal Ifp current of the LED lamp, and the LED lamp to be driven should be forward LED lights with the same voltage VF.
- 2. LED DRIVE:LED drive capability configuration register
- 3. Ifp: LED light conducts steady-state current.

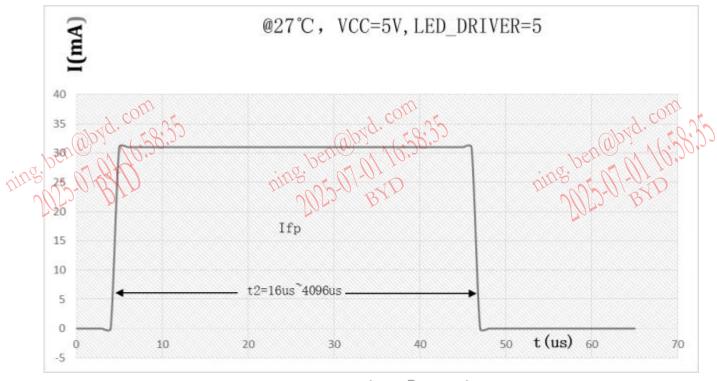
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#### LED serial dot matrix drive current-time diagram under several common configurations:



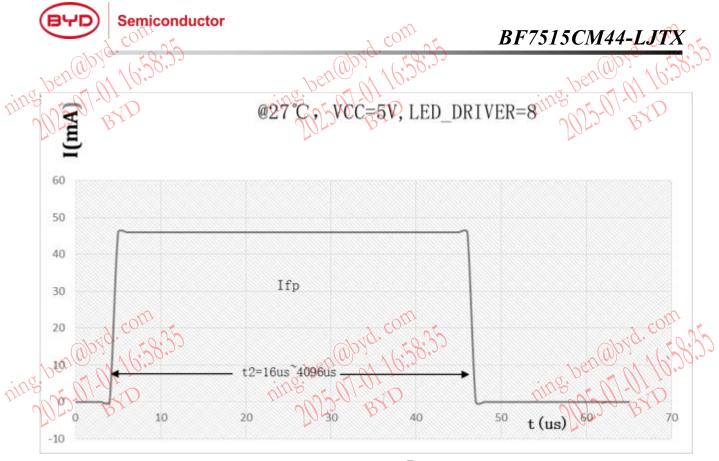
LED\_DRIVER VS Timeigure1



LED\_DRIVER VS Timigure2

BYD

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LED\_DRIVER VS Timigure3



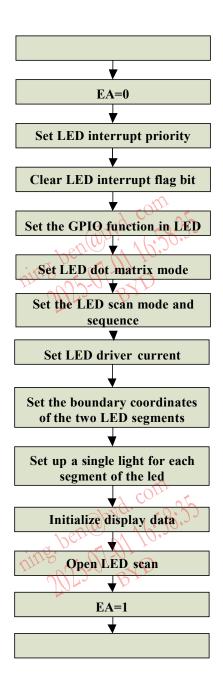
LED\_DRIVER VS Timigure4

BYD

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#### 15.1.6. LED Dot Matrix Configuration Process



LED dot matrix configuration flow chart

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#### 15.2. LED Matrix Drive

- Features of LED matrix drive mode: No. 11 16.5

  Support up to 8 COM x 8 SFC

  The SEG and C The SEG and COM scan period share the same register SCAN WIDTH, single SEG period=(scan width+1) \*16us, single COM period=(scan width+1) \*16us+8us;
- Single SEG conduction duty cycle:  $1/8 \sim 8/8$ , configured by the register DP CON[5:3];
- Support COM: 1 to 8, configured by the secondary bus register COM IO SEL;
- Support SEG: 1 to 8, configured by the secondary bus register SEG IO SEL configuration;
- Support LED row matrix 4\*4 mode, COM/SEG port by the register COM IO SEL control, in this mode PB[0:3] for COM0-3 port, PB[4:7] for SEG0-3 port, support COM 05-07-01 16:58 port forward and reverse configuration.

#### 15.2.1. LED Matrix Driver Description

In LED matrix mode, SEGL port/COML port are optional, IO is freely configured, and configured by the following secondary bus addressing mode. The number of COML ports scanned is completely controlled by the COML port selection configuration register (COM IO SEL), and the duty cycle of the single COML port lighting interval is selectable from 1/8 to 8/8.

COM IO SEL (23H) COM port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
R/W	N/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0.70	0	0	1000 c	0,7.0	0	0	70.0 × 0
75000 V 16:20.3			ben	00, 10:	20.5		ben (d)	2,16.3

10° 10°		
Bit number	Bit symbol	Description in S
1550 PIE		COML port selection configuration register, the
		corresponding bit is 1 to select COML port function
		1: Select COML port mode;
7~0		0: Select IO port mode
		Note: This register is valid when the LED matrix mode is
		selected, it is valid when the high current sink IO port drive is selected, and it is invalid in other cases

SEG IO SEL (24H) LED SEG0-7 port selection configuration register

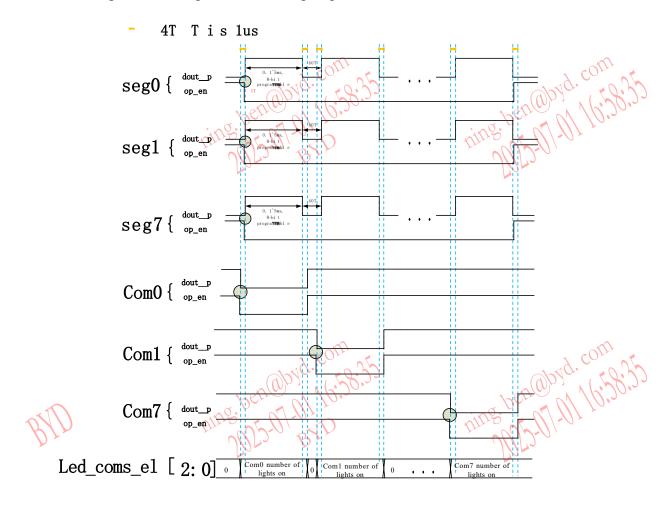
		<u> </u>						
Bit number	7	6	5	4 📈	3	2	1	0
Symbol	SEGL7	SEGL6	SEGL5	SEGL4	SEGL3	SEGL2	SEGL1	SEGL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0 .	2.9 Cr	0	0	0 .,	0. 9 Cr	0
DAI	Tire			77	100			

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Bit number Bit symbol	Description bent of 10.3
7~0	LED_SEG0-7 port select configuration register, corresponding to bit 1, SEGLx is segment
	1: select SEGMENT port mode; 0: select IO port mode

The SEG port output data corresponding to each COM port is stored in the SRAM to determine whether the light is on (1 means light, 0 means no light), the hardware code only needs to directly output data to the IO port according to the following sequence.



Timing diagram of LED matrix mode

BAD

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## 15.2.2. Display Configuration Address

LED matrix drive mode corresponding display configuration:

SEGx means to choose whether to light up, 0: no light, 1: light

Add	ress	7	6	5	4	3	2	1	0
1000H	COM0	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
1001H	COM1	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
1002H	COM2	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
1003H	COM3	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
1004H	COM4	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
1005H	COM5	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
1006H	COM6	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
1007H	COM7	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0

LED matrix drive mode corresponding display configuration table

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		COL		7 CC	BF/515CM44-LJ1X
	15 2 3 d	ED Matrix Driv	a Ragista	ben 0) 1/6	16:26
Z.		EB Matrix Bill	oth E		ping of Mal
7	Dr. B			SFR register	· Br
	Address	Name	RW	Reset	Description
	0xAE	INT_PE_STAT	RW	0000_0000Ь	Interrupt status register
	0xAF	SCAN_START	RW	xxxx_xxx0b	LCD, LED scan open register
	0xB1	DP_CON	RW	x000_0000b	LCD, LED control register
	0xB2	DP_MODE	RW	0000_0000b	LCD, LED mode register
	0xB3	SCAN_WIDTH	RW	0000_0000Ь	LED cycle configuration register
	0xB9	DP_CON1	RW	x000_0000b	LCD contrast Configuration Register
	0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
	0xF1	IRCONI	RW	0000_00xxb	Interrupt flag register 1
	0xF6	IPL1	RW	0000_00xxb	Interrupt priority register1
J.	0.10		ning		ping M. II.
	- 110-411'	4   1	( )	- 110 - 11	

Us. B	30	Sec	register		
Address	Name	RW	Reset	Description	
0x23	COM_IO_SEL RW		0000_0000Ь	COM selection configuration register	
0x24	SEG_IO_SEL	RW	0000_0000Ь	LED_SEG0-7 port selection configuration register	

### 15.2.3.1. LED Scan Open Register

SCAN START (AFH) LCD, LED scan open regist

		pan open i	75.50				
Bit number 7	6	5	4 co <sup>9</sup>	3	2	1	3 00000
Symbol	_	_ (	Opya.	8.5	_	- (	Jpha. 12
R/W	_	perin	2 17 10	_	_	perio	R/W
Reset value _	_ <	JINE OF	9/-0,	ı	_ %	TUS COL	

Bit number	Bit symbol	Description
		LCD, LED scan on register
0		1: Scan on; 0: Scan off

### 15.2.3.2. LED Control Register

DP CON (B1H) LCD, LED control register.

	DI COIT (DIII) LCI	, LLD Com		515001				
	Bit number 7	6	5	4 3	3	d. 2 3	1	0d. co.
	Symbol	IO_ON	DU	TY_SEL		DRSEL	SCAN_MODE	COM_MOD
g	R/W _	R/W	Oic	R/W		R/W	R/W	R/W
	Reset value _	0	0	00	)	0	0	0

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Bit number	Bit symbol	Description nine					
Mrs Br		LCD/LED scanning corresponds to the total control bit of all					
6	IO_ON	IO ports					
		0: Close IO; 1: Open IO					
		LED row and column drive mode single SEG port					
		conduction duty cycle configuration register:					
5~3	DUTY_SEL	0: 1/8 duty cycle; 1: 2/8 duty cycle; 2: 3/8 duty cycle; 3: 4/8 duty cycle; 4: 5/8 duty cycle; 5: 6/8 duty cycle;					
		6: 7/8 duty cycle; 7: 8/8 duty cycle					
		LCD, LED selection control bit					
2	DPSEL	0: Select LCD driver, LED driver is invalid					
		1: Select LED driver, LCD driver is invalid					
		LCD, LED scan mode configuration					
1	SCAN_MODE	1: Cycle scan mode					
		0: Interrupt scan mode					
		High current sink IO port drive enable					
		1: As a high current sink IO port;					
0	COM MOD	0: Can be configured for other functions;					
U		When used as a high current sink IO port, by configuring the					
		GPIO register to output the drive timing, the LED/LCD scan					
		configuration is invalid					

# 15.2.3.3. LED Mode Register

15.2.3.3, LED I	.50	mode reg	ben of	on 10:58:35		:179:	ben Ob	11/15.2	6.6
Bit number	7	6	15	B 4	3	2	113-11	80	
Symbol	LED_MOD	LCD_0	CKSEL	LCD_RSEL	LCD_	FCSEL	LCD_1	RMOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset value	0	0	0	0	0	0	0	0	

Bit number	Bit symbol	Description
		LED drive mode selection register
7	LED_MOD	1: Serial dot matrix scan
		0: Row and column matrix scan



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## 15.2.3.4. LED Cycle Configuration Register

	- 7 co	05				20	В	F/315CM	44 <b>-</b> LJT
15.2.3	0) 3.4. (LED)	Cycle Co	nfiguratio	n Registe	$r_{\sim}$	0:28:33			7 1/65
SCA	N WIDTE	H (B3H) L	ED cycle	configura	ion registe	er		2022-	7/20,
Bit	number	7	6	5	4	3	2	1	0
Sy	ymbol					_			
]	R/W					R/W			
Res	et value					0			

Bit number	Bit symbol	Description					
7~0		In the LED matrix drive mode, the corresponding single COM port scan time period = (scan_width+1)*16us, supports the configuration range 0.016~4.096ms					
45445 4 50		06:01/10/10 20					
15.2.3.5. LED Row and Column Matrix 4*4 Mode Register  DP. CON1 (B9H) LCD contrast configuration register							

#### 15.2.3.5. LED Row and Column Matrix 4\*4 Mode Register

DP CON1 (B9H) LCD contrast configuration register

21 cert (2)11) 2c2 tendust teningstation 108 lett									
Bit number	7	6	5	4					
Symbol	_	TRI_COM_INV	MATRIX_MOD	PD_LCD_POWER					
R/W	_	R/W	R/W	R/W					
Reset value	_	0	0	0					
Bit number	3	2	1	0					
Symbol		V	OL						
R/W <sub>2</sub>	R/W	R/W 1 CO	R/W	R/W 1 COM					
Reset value	0	Opia.	0	apilo, it					

Bit number	Bit symbol	Description with the contract of the contract				
7772 D.	TRI COM INIV	LED matrix 4*4 mode COM port reverse selection register				
6		in 4*4 mode,				
6	TRI_COM_INV	1: Output high when COM is selected;				
		0: Output low when COM is selected				
		LED matrix 4*4 mode selection register				
		1: Select 4*4 mode, LED0~LED3 correspond,				
5	MATRIX_MOD	COM0~COM3 port selection, LED4~LED7 correspond, SEG0~SEG3 port selection;				
		0: Not select 4*4 mode				



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## 15.2.3.6. Interrupt Status Register

M.	11F	PE	STAT	(AEH)	Interrupt	t status	register
----	-----	----	------	-------	-----------	----------	----------

2 0	in of		BF751	5CM44-LJTX			
15.2.3.6. Interrupt Status Register  INT_PE_STAT (AEH) Interrupt status register							
Bit number	7	6	5	4			
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT			
R/W	R/W	R/W	R/W	R/W			
Reset value	0	0	0	0			
Bit number	3	2	1	0			
Symbol	INT_TIMER2_STAT	INT_PWM0_STAT	INT_LCD_STAT	INT_LED_STAT			
R/W	R/W	R/W	R/W	R/W			
Reset value	0	0 000	0	0			

•	Bit number	Bit symbol	Description	,
500	125-01-01-10	INT_LCD_STAT	LCD interrupt status mark, this bit is cleared by writing 0, and it can also be cleared by writing SCAN_START 1: Interrupt is valid; 0: Interrupt is invalid	

### IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	_	EX4	EX3	EX2	_	_
R/W	R/W	R/W	_	R/W	R/W	R/W	_	_
Reset value	0	0	_	0	0	0	_	_

	Bit number	Bit symbol	Description	y com
	20)p/0.	8:33	LED/LCD interrupt enable	2000
0	pen 60/40	EX6	1: LED/LCD interrupt enable;	period W. 10.
DIVE	つらりはり		0: LED/LCD interrupt disable	Jille OF 11-01

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	_	IE4	IE3	IE2	_	_
R/W	R/W	R/W	_	R/W	R/W	R/W	_	_
Reset value	0	0	_	0	0	0	_	_

Bit number	Bit symbol	Description	
		LED/LCD interrupt flag	
6, 0	IE6	1: LED/LCD interrupt flag	1 com
abyd.	2.33	0: Clear LED/LCD interrupt flag	abyd. co
- LINP 1 ( s)	7()0-	- 11015	

IPL1 (F6H) Interrupt priority register1

- 3	4 A (1 04 1) 1416	mapt prior	ity registe	1 + 10° 01 1	10,		10°5	7/1/0,
5	Bit number	7	6	1085	3	2	ing 1	1-110
	Symbol	IPL1.7	IPL1.6	IPD1.	4 IPL1.3	IPL1.2	JU13-	BI

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(0)	7(100							21
R/W	R/W	R/W	_	R/W	R/W	R/W	- 01/10	,)
Reset value	0	0	_	0	0	0	2050	

Bit number	Bit symbol	Description
		LED/LCD interrupt priority bit
6	IPL1.6	1: LED/LCD interrupt is high priority;
		0: LED/LCD interrupt is low priority

## 15.2.4. Secondary Bus Register

## 15.2.4.1. COM Port Selection Configuration Register

COM IO SEL (23H) COML select configuration register

Bit number	7	6	Mrs 505	1 4	3	2		
Symbol	COML7	COML6	COML5	COML4	COML3	COML2	COML1	COML0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
		In LED matrix drive mode, 4*4 mode is not selected:
		COM port select configuration register, the corresponding bit is 1,
		COMLx is common
		1: Select the COM port function.
		0: Select the I/O port mode
7.0		In LED matrix drive mode, select 4*4 mode:
7~0		COML0~ COML3 is common, and COML4~ COML7 is segment
Ri		1: Select COM port function or SEG port function;
		0: Select the I/O port mode
		When the high current IO port drive is enabled:
		1: Select the high-current I/O port
		0: Select the I/O port mode

### 15.2.4.2. LED\_SEG0-7 Port Selection Configuration Register

SEG IO SEL (24H) LED SEG0-7 port selection configuration register

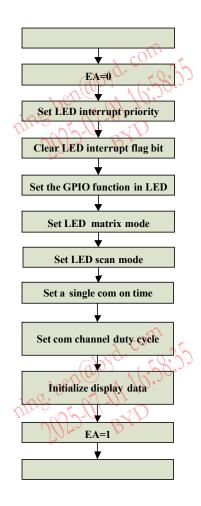
Bit number	(4.0)	6	5	15 y d4 Cor	5.7.3	2	1	1/2.0°0
Symbol	SEGL7	SEGL6	SEGL5	SEGL4	SEGL3	SEGL2	SEGLI	SEGLO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	JØJ. 2.	0	0	0	000	0

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		ing. All ing.
Bit number	Bit symbol	Description Description
7~0	-	LED_SEG0-7 port select configuration register, corresponding to bit 1, SEGLx is segment
, 0		1: select SEGMENT port mode; 0: select IO port mode

### 15.2.5. LED Matrix Configuration Process



LED matrix configuration flow chart

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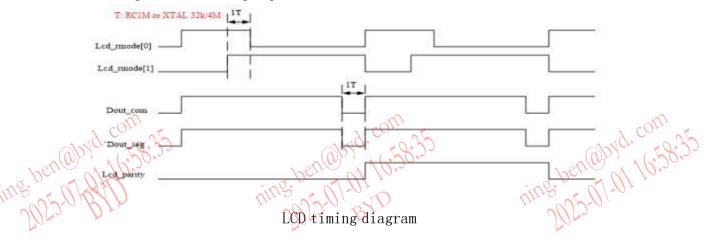
#### 15.3. LCD Driver

Features of LCD drive mode:

- Supports duty cycles, selected according to register DUTY\_SEL
- 4 COM x 28 SEG (1/4 duty cycle, 1/3 bias)
- 5 COM x 27 SEG (1/5 duty cycle, 1/3 bias)
- 6 COM x 26 SEG (1/6 duty cycle, 1/3 or 1/4 bias)
- 8 COM x 24 SEG (1/8 duty cycle, 1/4 bias)
- Support 2 drive modes: Traditional resistance mode (fast charging mode, slow charging mode), automatic switching mode between fast and slow charging.
- Support 3 kinds of bias resistance: 60k/225k/900k.
- Operating clocks: LIRC 32kHz, XTAL 32768Hz/4MHz, RC1MHz
  - Select RC1M, the lighting time of a single COM can be configured, the configuration range is 0.064~4.096ms, and the step is 64us;
  - Select LIRC 32KHz and XTAL 32768Hz, LCD conduction frequency is fixed at 64Hz (8COM configuration);
  - Select XTAL 4MHz, LCD conduction frequency is fixed at 7.8125kHz (8COM configuration)
- Support LCD contrast control, 0.531VDD~1.000VDD, 16-level contrast adjustment.
- The COM port is determined by the duty cycle configuration, and the SEG port is freely configured by the register.

#### 15.3.1. LCD Driver Description

In LCD mode, the number of COM ports scanned is completely controlled by the drive mode duty cycle configuration register DUTY\_SEL, and the SEG port selection is freely configured by LCD\_IO\_SEL\_1, LCD\_IO\_SEL\_2, LCD\_IO\_SEL\_3, LCD\_IO\_SEL\_4 registers, configured by the secondary bus addressing mode, LCD\_IO\_SEL\_4 also determines the sharing, When the COM port in the mode is used as SEG port, whether the corresponding COM port is selected. SRAM stores the corresponding SEG port output data of each COM port to determine whether to light up (1 means light, 0 means no light). The hardware code needs to directly output data to the IO port control circuit according to the following sequence.



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	(U)		(U)	
e	DUTY_SEL	duty cycle&& bias	COM*SEG	bento 11 15.30
	000/110/111	1/4 duty cycle, 1/3 bias	4 COM x 16/24 SEG COM 0-3, SEG 0-23	ning 2025-01-02
	001	1/8 duty cycle, 1/4 bias	8 COM x 16/24 SEG COM 0-7, SEG 0-23	
	010	1/4 duty cycle, 1/3 bias	4 COM x 20/28 SEG COM 0-3, SEG 0-23,	COM 4-7 shared as SEG 24-27
	011	1/5 duty cycle, 1/3 bias	5 COM x 19/27 SEG COM 0-4, SEG 0-23,	COM 5-7 shared as SEG 25-27
	100	1/6 duty cycle, 1/3bias	6 COM x 18/26 SEG COM 0-5, SEG 0-23,	COM 6-7 shared as SEG 26-27
	101	1/6 duty cycle, 1/4bias	6 COM x 18/26 SEG COM 0-5, SEG 0-23,	COM 6-7 shared as SEG 26-27
		LCD COM*SE	EG correspondence ta	ble
na	alog IO implement	s the following truth tab	ole:	10,50
ia	s voltage selection	LCD_BIAS_SEL	0: 1/3 bias voltage	e 1: 1/4 bias voltage;
				_

#### LCD COM\*SEG correspondence table

Odd and even frame selection LCD PARITY 0: odd frame 1: even frame;

Resistance string selection LCD\_RMODE 001: 20K 010: 75K 100: 300K;

Data selection DOUT PB (for example), compatible with the previous data line, the output function of the corresponding IO port is invalid (OP EN N=1);

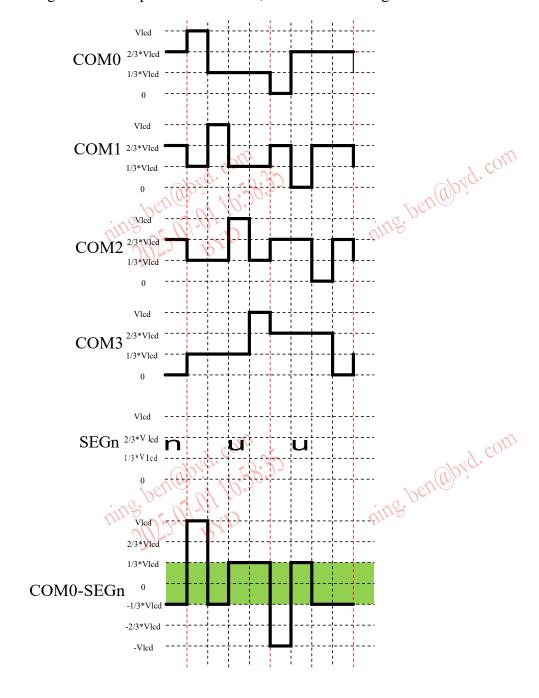
	COM truth table										
	LCD_BIAS_SEL	LCD_PARITY	DOUT_PB	Output voltage value							
	COLL	0	y com	1/3VLCD							
ning, ben abyd	0	0 0	1	VLCD							
per per	0	· valperr	0	2/3VLCD							
Ullie B	0	Ulling	1	VSS							
y	1	0	0	1/4VLCD							
	1	0	1	VLCD							
	1	1	0	3/4VLCD							
	1	1	1	VSS							
		SEG tr	uth table								
	LCD_BIAS_SEL	LCD_PARITY	DOUT_PB	Output voltage value							
	0	0	0	2/3VLCD							
	0	0	1	VSS							
	0	1	0	1/3VLCD							
	0	1	1	VLCD							
	1	0	0	2/4VLCD							
	1	0	1	VSS							
	1	1	0	2/4VLCD							

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**VLCD** 

1 CCD configure truth table

This realizes the bias voltage division sequence on the PAD, as shown in the figure below



LCD timing diagram (1/4 duty cycle, 1/3 bias)

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LCD timing diagram (1/8 duty cycle, 1/4 bias)

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# 15.3.2. Display Configuration Address

LCD drive mode corresponding display configuration:

SEGx means to choose whether to light up, 0: no light, 1: light;

Address	7	6	5	4	3	2	1	0	
	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0	
1000H	SEG0								
1001H	SEG1								
1002H	SEG2								
1003H	SEG3								
1004H	SEG4								
1005H	SEG5								
1006H	SEG6								
1007H	SEG7								
1008H	SEG8								
1009H	SEG9								
100AH	SEG10								
100BH	SEG11								
100CH	SEG12								
100DH	SEG13								
100EH	SEG14								
100FH	SEG15								
1010H	SEG16								
1011H	SEG17								
1012H	SEG18								
1013H	SEG19								
1014H	SEG20								
1015H	SEG21								
1016H	SEG22								
1017H	SEG23								
1018H	SEG24								
1019H			SEG25	SEG25	SEG25	SEG25	SEG25	SEG25	
101AH			SEG26	SEG26	SEG26	SEG26	SEG26	SEG26	
101BH					SEG27	SEG27	SEG27	SEG27	

LCD drive mode corresponding display configuration table

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### 15.3.3. LCD Register

	BYD	Semiconductor		2 CO	BF7515CM44-LJTX
15.3.3. LCD Register			ning	ben@bya 16	58.53 ping ben @ 10.58.53
	Mrs B	) <b>)</b>	0	SFR register	
	Address	Name	RW	Reset	Description
	0xAE	INT_PE_STAT	RW	0000_0000b	Interrupt status register
	0xAF	SCAN_START	RW	xxxx_xxx0b	LCD, LED scan open register
	0xB1	DP_CON	RW	x000_0000b	LCD, LED control register
	0xB2	DP_MODE	RW	0000_0000Ь	LCD, LED mode register
	0xB3	SCAN_WIDTH	RW	0000_0000Ь	LED cycle configuration register
	0xB9	DP_CON1	RW	x000_0000b	LCD contrast configuration register
	0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
	0xF1	IRCONI	RW	0000 00xxb	Interrupt flag register 1
	0xF6	INT DO	RW	0000_00xxb	Interrupt priority register1
5	1-17-1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	ning:	7-11-1	sing M. William
	U.D. B		Sec	ondary bus re	gister
	Address	Name	RW	Reset	Description

USS-A B	510	Seco	ndary bus regis	ster BY
Address	Name	Name RW Rese		Description
0x1F	LCD_IO_SEL_1	RW	0000_0000ь	LCD_SEG0-7 port selection configuration register
0x20	20 LCD_IO_SEL_2 R		0000_0000Ь	LCD_SEG8-15 port selection configuration register
0x21	LCD_IO_SEL_3	RW	0000_0000ь	LCD_SEG16-23 port selection configuration register
0x22	LCD_IO_SEL_4	RW	xxxx_0000b	LCD_SEG24-27 port selection configuration register
0x63	XTAL_CLK_SEL	RW	xxxx_xxx0b	Crystal frequency selection register
15.3.3.1. L	CD Scan Open Regi	2022-01-01 10.0		

#### 15.3.3.1. LCD Scan Open Register

SCAN\_START, (AFH) LCD, LED scan open register Bit number 5 3 0 Symbol R/W R/W Reset value 0

	Bit number	Bit symbol	Description	com
	pen @ 01 70:2	P.32	LCD, LED scan on register  1: Scan on; 0: Scan off	pen(a)pyd. 16:28
$\sigma$				

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	7 COD	1					٥٢	<b>BF7515</b>	CM44-LJTX	
	15332 depe	8;,)	ol Dogistor			(	16:28:3	, 3	0, 16:5	
DP CON (B1H) LCD, LED control register										
	Bit number	7	6	5	4	3	2	1	0	
	Symbol	_	IO_ON	DU	TY_S	SEL	DPSEL	SCAN_MODE	COM_MOD	
	R/W	_	R/W		R/W		R/W	R/W	R/W	
	Reset value	_	0	0	0	0	0	0	0	

Bit number	Bit symbol	Description
6	IO_ON	LCD/LED scanning corresponds to the total control bit of all IO ports 0: Close IO; 1: Open IO
5~3	DUTY_SEL	LCD drive mode duty cycle configuration register  000: 1/4 duty cycle, 1/3 bias (4 COM X 16/24 SEG)  COM port: COM0-3, SEG port: SEG0-23  001: 1/8 duty cycle, 1/4 bias (8 COM X 16/24SEG)  COM port: COM0-7, SEG port: SEG0-23  010: 1/4 duty cycle, 1/3 bias (4 COM X 20/28 SEG)  COM port: COM0-3,  SEG port: SEG0-23, COM4-7 shared as SEG24-27  011: 1/5 duty cycle, 1/3 bias (5 COM X 19/27 SEG)  COM port: COM0-4,  SEG port: SEG0-23, COM5-7 shared as SEG25-27  100: 1/6 duty cycle, 1/3 bias (6 COM X 18/26 SEG)  COM: COM0-5,  SEG: SEG0 -23, COM6-7 shared as SEG26-SEG27  101: 1/6 duty cycle, 1/4 bias (6 COM X 18/26 SEG)  COM port: COM0-5  SEG port: SEG0-23, COM6-7 shared as SEG26-SEG27  Others: 1/4 duty cycle, 1/3 bias (4 COM X 16/24 SEG)  COM: COM0-3, SEG: SEG0-23
2	DPSEL	LCD, LED selection control bit  0: Select LCD driver, LED driver is invalid  1: Select LED driver, LCD driver is invalid
1	SCAN_MODE	LCD, LED scan mode configuration  1: Cycle scan mode  0: Interrupt scan mode
0	COM_MOD	High current sink IO port drive enable  1: As a high current sink IO port;  0: Can be configured for other functions;

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When used as a high current sink IO port, by configuring the GPIO register to output the drive timing, the LED/LCD scan configuration is invalid

## 15.3.3.3. LCD Mode Register

DP MODE (B2H) LCD, LED mode register

DI_IVIODE (D2	(11) LCD, LLD	mode reg	13101					
Bit number	7	6	5	4	3	2	1	0
Symbol	LED_MOD	LCD_0	CKSEL	LCD_RSEL	LCD_I	FCSEL	LCD_RMOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	25 0	0	0	7,000	0	0	0	4. 60m

2 (0) , V (2,20.2		20.5	$\mathcal{L}(0)$ , $\mathcal{L}(0)$ , $\mathcal{L}(0)$ , $\mathcal{L}(0)$			
2	Bit number	Bit symbol	Description Description			
	MIS-UI BYD		LCD clock selection register			
	6~5	LCD CKSEL	10/11: Select RC1M			
	0~3	LCD_CRSLL	01: Select XTAL 32768Hz			
			00: Select LIRC			
			Charge time control bit			
	3~2	LCD_FCSEL	00: 1/8 LCD com period; 01: 1/16 LCD com period;			
			10: 1/32 LCD com period; 11: 1/64 LCD com period			
			LCD bias resistance selection control bit			
	4	LCD_RSEL	0: The sum of LCD bias resistance is 225k;			
			1: The sum of LCD bias resistance is 900k			
			Drive mode selection bit			
	$\sim$	\ \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	00: Traditional resistance mode (slow charging mode), the total			
	RVV		bias resistance is 225k/900k, when LCD_RSEL = 0, the total			
	D F		LCD bias resistance is 225K, when LCD_RSEL = 1, the total			
	1~0	LCD RMOD	LCD bias resistance is 900K			
	1~0	LCD_RWOD	01: Traditional resistance mode (fast charging mode), the total			
			bias resistance is 60k			
			10/11: Fast and slow charging automatic switching mode, the			
			total bias resistance is automatically switched between 60k and			
			225k/900k			

### 15.3.3.4. LCD Period Configuration Register

SCAN WIDTH (B3H) LED period configuration register

> C 1 11   11 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 (2311) 222	period cominguitation register	
Bit number	7	6 3 4 3	2 ning of 0
Symbol		Mrs. P.	

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OP! R/W	R/W	ı
Reset value	0	ı

Bit number	Bit symbol	Description
7~0		In LCD drive mode, the corresponding single COM port scan
		time:
		period=(scan_width+1)*64us, support the configuration range
		0.064~4.096ms, the upper two digits are reserved
		Note: In this mode, this register is only applicable to the LCD
		selection clock CLK_1M mode, the slowest LCD frame rate in
		other clock modes is 64Hz (8*24)

## 15.3.3.5. LCD Contrast Configuration Register

	other clock modes is 64Hz (8*24)								
15.3.3.5. LCD Contrast Configuration Register  DP_CON1 (B9H) LCD contrast configuration register									
Bit number	7	6	5	4					
Symbol	_	TRI_COM_INV	MATRIX_MOD	PD_LCD_POWER					
R/W	_	R/W	R/W	R/W					
Reset value	_	0	0	0					
Bit number	3	2	1	0					
Symbol	Symbol VOL								
R/W	R/W	R/W	R/W	R/W					
Reset value	0 0	0 200	0	0 d com					

	70	
Bit number	Bit symbol	Description Description
05-048	PD_LCD_POWER	LCD contrast control enable bit
M		0: Turn off LCD contrast control;
		1: Turn on LCD contrast control
3~0	VOL	LCD contrast control bit
		0000: VLCD = 0.53VDD; 0001: VLCD = 0.56VDD;
		0010: VLCD = 0.59VDD; 0011: VLCD = 0.63VDD;
		0100: VLCD = 0.66VDD; 0101: VLCD = 0.69VDD;
		0110: VLCD = 0.72VDD; 0111: VLCD = 0.75VDD;
		1000: VLCD = 0.78VDD; 1001: VLCD = 0.81VDD;
		1010: VLCD = 0.84VDD; 1011: VLCD = 0.88VDD;
		1100: VLCD = 0.91VDD; 1101: VLCD = 0.94VDD;
		1110: VLCD = 0.97VDD; 1111: VLCD = 1.00VDD

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7 00	05	0	KF/31	<u> </u>
8.0201-01	rupt Status Register  (AEH) Interrupt status	s register	73	2025-07-01 16:58
Bit number	7	6	5	4
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT_TIMER2_STAT	INT_PWM0_STAT	INT_LCD_STAT	INT_LED_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0 000	0	0

	Bit number	Bit symbol	Description Description
500	1	INT_LCD_STAT	LCD interrupt status mark, this bit is cleared by writing 0, and it can also be cleared by writing SCAN_START 1: Interrupt is valid; 0: Interrupt is invalid

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	_	EX4	EX3	EX2	_	_
R/W	R/W	R/W	_	R/W	R/W	R/W	_	_
Reset value	0	0	_	0	0	0	_	_

	Bit number	Bit symbol	Description	y com
	20)p/0.	8:33	LED/LCD interrupt enable	
۲.	pen 60/40	EX6	1: LED/LCD interrupt enable;	pen M. M.
ح	つらりはり		0: LED/LCD interrupt disable	ning of

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	_	IE4	IE3	IE2	_	_
R/W	R/W	R/W	_	R/W	R/W	R/W	_	_
Reset value	0	0	_	0	0	0	_	_

Bit number	Bit symbol	Description	
		LED/LCD interrupt flag	
6, 0	IE6	1: LED/LCD interrupt flag	1 com
abyd.	5.33	0: Clear LED/LCD interrupt flag	abyd. co
- LINP 1 ( o)	7()•-		

IPL1 (F6H) Interrupt priority register1

4 A (1 04 1) 1116	mapt prior	ity registe	1 1 10 b	7/10			10°	~/ / /	
Bit number	7	6	1085	4	3	2	ngi.	1/1/0	
Symbol	IPL1.7	IPL1.6	I	PD1.4	IPL1.3	IPL1.2	JU13.	BALL	

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	7()								Ų.
PW/	R/W	R/W	_	R/W	R/W	R/W	_	1/10.	
Reset value	0	0	_	0	0	0	-10-20-	_	

Bit number	Bit symbol	Description				
		LED/LCD interrupt priority bit				
6	IPL1.6	1: LED/LCD interrupt is high priority;				
		0: LED/LCD interrupt is low priority				

## 15.3.4. LCD Secondary Bus Register

## 15.3.4.1. LCD\_SEG Port Selection Configuration Register

LCD 10 SEL 1 (1FH) LCD SEG0-7 port selection configuration register

		. ((1111) 1	D DLG0	/ port soil	CHOIL COLL	Ediamon 1	ogistei		1 1 0 1
5	Bit number	7	- 6 .	or Belle	1/4/10.	3	2 .	o perio	U/0/0.
	Symbol	SEG7	SEG6 5	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0		LCD_SEG0-7 port selection configuration register. A Bit of 1 indicates that SEG port function is selected.  1: Select SEGMENT port mode;  0: Select IO port mode

LCD IO SEL 2 (20H) LCD SEG8-15 port selection configuration register

Bit number	8:37	6	5	byd4 5	8:33	2	1	oyd o co
Symbol	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8
R/W	R/W	R/W 🥎	R/W	R/W	R/W	R/W 🚫	R/W	R/W
Reset value	0	0	000	0	0	0	0/0/2	0

Bit number	Bit symbol	Description				
7~0		LCD_SEG8-15 port selection configuration register.  A Bit of 1 indicates that SEG port function is selected.  1: Select SEGMENT port mode;  0: Select IO port mode				

LCD IO SEL 3 (21H) LCD SEG16-23 port selection configuration register

Bit number	7	6	5	4.00	3	2	1	000
Symbol	SEG23	SEG22	SEG21	SEG20	SEG19	SEG18	SEG17	SEG16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	W. 6. 0 . V.	/_//0	0	0	0. 0. V	////0

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$(11)^{6}$	7()0-	
Bit number	Bit symbol	bent of long bent of long
705-01-01	5	LCD_SEG16-23 port selection configuration register.  A Bit of 1 indicates that SEG port function is selected.
7~0		1: Select SEGMENT port mode;
		0: Select IO port mode

LCD IO SEL 4 (22H) LCD SEG24-27 port selection configuration register

Bit number	7	6	6 5 4 3 2		1	0		
Symbol	_	_	_	_	SEG27/COM7	SEG26/COM6	SEG25/COM5	SEG24/COM4
R/W	_	_	_	_	R/W	R/W	R/W	R/W
Reset value	_			_	0	0	0	0

	-()/		
	Bit number	Bit symbol	Description
	Per (0) 1/2	20.2	LCD_SEG24-27 port selection configuration register,
Q	25 W-117		reserved in non-sharing mode, shared mode COM4~COM7
(	3~0		is LCD_SEG24-27
			1: Select SEG24~SEG27 port/COM3~COM7;
			0: Select IO port mode

### 15.3.4.2. Crystal Frequency Selection Register

XTAL CLK SEL (63H) Crystal frequency selection register

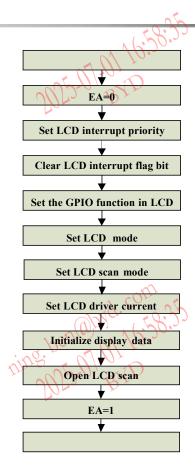
Bit number	7	6	5	4	3	2	1	0
Symbol	<u>-</u>	_	_	_	_	_	_	_
R/W	Ω	1	ı	1-com	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	_	_	R/W
Reset value	8:2	_	- (1	pya. C	8:25	_	- (6)	010.0 3
			7/10				7	

Bit number	Bit symbol	Descrip	tion ning
		Crystal frequency selection regis	ster
		1: Select 4MHz;	
		0: Select 32768Hz	

## 15.3.5. LCD Configuration Process



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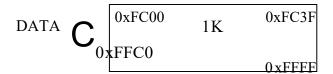
LCD configure process

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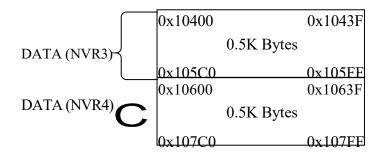
16. DATA Area

When EEP\_SELECT = 0, select address 0xFC00~0xFFFF as DATA area, one page. When using, it needs to perform page erasing, and then perform byte write operation, which can only be written once after erasing. The data area is erased and the data is 0xff.



 $\{SPROG\_ADDR\_H[1:0], SPROG\_ADDR\_L[7:0]\}$  The logical address  $(0\sim1023)$  corresponds to the physical address  $(0xFC00\sim0xFFFF)$ .

When EEP\_SELECT = 1, select NVR3 and NVR4 as the DATA area, each block of 512Bytes is a page, and the address is  $(0x10400\sim0x107FF)$ . When using, it needs to perform page erasing, and then perform byte write operation, which can only be written once after erasing.



#### NVR3:

{SPROG\_ADDR\_H[0], SPROG\_ADDR\_L}The logical address  $(0x4400+(0\sim511))$  corresponds to the physical address  $(0x10400\sim0x105FF)$ .

#### NVR4:

 $\{SPROG\_ADDR\_H[0], SPROG\_ADDR\_L\}$  The logical address  $(0x4600+(0\sim511))$  corresponds to the physical address  $(0x10600\sim0x107FF)$ .

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## 16.1. Page Erase Step

When EEP\_SELECT = 0, select the address (0xFC00~0xFFFF) as the DATA area, 1 page. When EEP\_SELECT = 1, select NVR3/4 as DATA area, NVR3 is 1 page, NVR4 is 1 page.

- 1. SPROG\_TIM[4:0] =  $0 \sim 9$  (suggest 5ms), byte write time is fixed at 23.5us, The main() program function is only configured once.
- 2. Close interrupt
- 3. EEP SELECT select;
- 4. Configure SPROG ADDR H, SPROG ADDR L, select to erase the page;
- 5. Configure SPROG CMD = 0x96;
- 6. Write 4 NOP instructions;
- 7. Start erasing, the CPU turns off the clock fsys, and turns on the clock fsys after erasing is completed;
- 8. Need to continue to erase data, jump to step 2;
- 9. Configure SPROG ADDR L=0x00, SPROG ADDR H=0x00, restore interrupt settings.

#### 16.2. Byte Write Step

When EEP\_SELECT = 0, select the address (0xFC00~0xFFFF) as the DATA area, 1 page. When EEP\_SELECT = 1, select NVR3/4 as DATA area, NVR3 is 1 page, NVR4 is 1 page.

- 1. SPROG\_TIM[4:0] =  $0\sim9$ (suggest 5ms), byte write time is fixed at 23.5us, The main() program function is only configured once;
- 2. Close interrupt;
- 3. EEP SELECT select;
- 4. Configure SPROG ADDR H, SPROG\_ADDR\_L, byte write address;
- 5. Configure SPROG DATA;
- 6. Configure SPROG CMD = 0x69;
- 7. Write 4 NOP instructions;
- 8. Start writing, the CPU turns off the clock fsys, and turns on the clock fsys after completion;
- 9. Need to continue to write data, jump to step 3;
- 10. Configure SPROG ADDR L=0x00, SPROG ADDR H=0x00, restore interrupt settings.

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### 16.3. Registers

Mrs B		)	SFR register	Mrs. Br.
Address	Name	RW	Reset	Description
0xCE	SPROG_ADDR_H	RW	0000_0000Ь	Address control register
0xCF	SPROG_ADDR_L	RW	0000_0000Ь	Address control register low 8 bits
0xD1	SPROG_DATA	RW	0000_0000Ь	Write data register
0xD2	SPROG_CMD	RW	0000_0000Ь	Command register
0xD3	SPROG_TIM	RW	1101_1101b	Erase time control register

· om	Secon	dary bus register	an a
Address	RW	Reset	<b>Description</b>
0x5B EEP SELECT	RW	xxxx xxx0b DA	TA area selection register

# 16.3.1. Address control register

SPROG ADDR H (CEH) Address control register

STREE TIBBR II (CEII) TRACTOSS CONGOTTOS SISCOT								
Bit number	7	6	5	4	3	2	1	0
Symbol		_						
R/W		R/W						
Reset value					0			

Bit number	Bit symbol	Description
2 co/		In non-Flash Boot upgrade mode:
alloyd.com		Bit[6:2]: DATA area (0xFC00~0xFFFF) selection enable
berre		00000: Select DATA area (0xFC00~0xFFFF), 1024Bytes
e BAN	ζ.	Other: invalid
y'		1. DATA area (0xFC00~0xFFFF):
		config {SPROG_ADDR_H[1:0], SPROG_ADDR_L[7:0]}
7~0		2. When SPROG_ADDR_H[2]=1, select NVR4:
		config {SPROG_ADDR_H[0], SPROG_ADDR_L[7:0]}
		3. When SPROG_ADDR_H[2]=0, select NVR3:
		config {SPROG_ADDR_H[0], SPROG_ADDR_L[7:0]}
		Note: In Flash_Boot upgrade mode,
		{ SPROG_ADDR_H, SPROG_ADDR_L} multiplexing all space addresses of CODE

## 16.3.2. Address control register low 8 bits

SPROG\_ADDR\_L(CFH) Address control register low 8 bits

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	1/10-				
Bit number	7	6	3	2	(10/0,5)
Symbol		7	SPROG_ADDR_L[7:0]	77	US. 02.01-01
R/W			R/W		JJ 7.2
Reset value			0		

Bit number	Bit symbol	Description
7~0	SPROG_ADDR_L[7:0]	The lower 8 bits of the address

## 16.3.3. Write Data Register

SPROG DATA(D1H) Write data register

	( <del>)</del>		<i>0</i>	~11}				~112
Bit number	27	6	5	1-1/24 <sup>COS</sup>	253	2	1	79.0
Symbol	26.33		1 00	000 16:54	5.55			62 16.2
R/W			ing. Do	R/V	V	Å	25. D	11/1/100
Reset value		Υ,	J.C. [10	0		1	000	BYD
Bit number	Bit syr	nbol		<u>*</u>	Descr	ription	Min	<b>y</b>
7~0			data to be	written				

# 16.3.4. Command Register

SPROG CMD(D2H) Command register

Bit number	7	6	5	4	3	2	1	0
Symbol			<u>-</u>					
R/W,	0	R W						1 com
Reset value	8:22	9phqq. (26:32)						pyo.

Bit number	Bit symbol	ning Description ning
7/172 1/2		Write 0x96: page erase
		Write 0x69: byte burn
		Write 0x88: read data indirectly;
		When continuously writing data 0x12, 0x34, 0x56, 0x78,
7.0		0x9A, enter the Flash Boot upgrade mode;
7~0		When continuously writing data 0xFE, 0xDC, 0xBA, 0x98,
		0x76, exit the Flash Boot upgrade mode
		When CFG_BOOT_SEL = 3 or the program is running in a
		non-BOOT space, the BOOT upgrade mode cannot be
		entered.

# 16.3.5. Erase Time Control Register

SPROG\_TIM(D3H) Erase time control register

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	(0)	7()00		( ( )		((), ~		((1)	P . ( )
<	Bit number	7	6	3 Sent	14/D.	3	2	2 PEVICE	0/0/0.2
7	Symbol	_	_ \$	1118V.		ı	- DJ	U.S. 02-0	/~/
(	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RW	R/W
	Reset value	1	1	0	1	1	1	0	1

Bit number	Bit symbol	Description
7~5	SPROG_TIM[7:5]	Byte write fixed time is 23.5us
		Erase time configuration SPROG_TIM[4:0]=0~31 When the selected address is 0xFC00~0xFFFF: When SPROG_TIM[4:0]=0~9,
4~0	SPROG_TIM[4:0]	Erase Time = 1.13 + SPROG_TIM[4:0] (ms); When SPROG_TIM[4:0]=10~31, Erase time = 9.13 (ms)
		When selecting NVR3/4 or BOOT upgrade mode: When SPROG_TIM[4:0]=0~9,
		Erase Time=0.57+0.5* SPROG_TIM[4:0] (ms);
		When SPROG_TIM[4:0]=10~31,
		Erase time=4.57(ms)

# 16.3.6. Secondary Bus Register

EEP SELECT (5BH) DATA area selection register

DEI SEEE	(,			5.000				
Bit number	7	6	5	4	3	2	1	0
Symbol o	V 25	-	-	1- CON	Ω <u> </u>	-		1-com
R/W	3:72	_	_ (	Johan C	8:23	_	- ((	R/W
Reset value		_	2 pen	7/0	_	_	" pend	0/0/0

Bit number	Bit symbol	Description						
0		1: Select NVR3 and NVR4 as DATA area						
		When SPROG_ADDR_H[2]=1, select NVR4; When SPROG_ADDR_H[2]=0, select NVR3						
		0: Select address (0xFC00~0xFFFF) as DATA area, 1 page						

BAM

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## 16.4. DATA Area Read

DATA area (0xFC00~0xFFFF) read: directly read the CODE absolute address (0xFC00+0~1023).

#### NVR3 and NVR4 read:

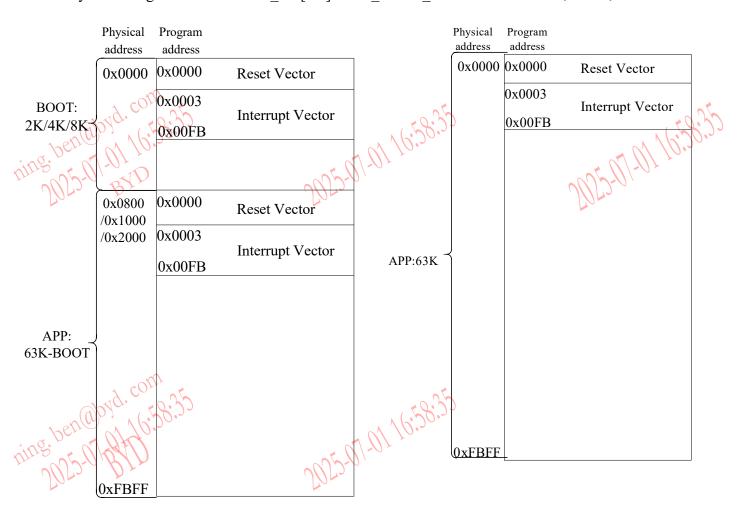
- 1. Turn off the interrupt;
- 2. Configure SPROG CMD = 0x88;
- 3. Configure SPROG\_ADDR\_H, SPROG\_ADDR\_L, the address to be read;
- 4. NVR3: {SPROG\_ADDR\_H, SPROG\_ADDR\_L} The logical address (0x4400+(0~511)) corresponds to the physical address (0x10400~0x105FF).
  - NVR4: {SPROG\_ADDR\_H, SPROG\_ADDR\_L} The logical address (0x4600+(0~511)) corresponds to the physical address (0x10600~0x107FF);
- 5. Read SPROG RDATA data;
- 6. Need to continue to read data, jump to step 2 and 3;
- 7. After reading SPROG RDATA data, configure SPROG CMD = 0x00;
- 8. Configure SPROG ADDR L=0x00, SPROG ADDR H=0x00; restore interrupt settings.

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# 17. IAP Operation

CFG\_11: [7:6] When CFG\_BOOT\_SEL is not equal to 3, Flash supports the IAP BOOT upgrade function, by sending IAP operation commands to realize the jump between the BOOT area and the APP area, BOOT comes with storage and write protection, and the size of the BOOT area is set by the configuration word CFG\_11:[7:6]- CFG\_BOOT\_SEL selection: 0: 2K, 1: 4K, 2: 8K.



Left: BOOT and APP partition map; Right: APP map, not-BOOT map

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# 17.1. Flash IAP Related Registers

Dry B		0	SFRregister	10123 B3	
Address	Name	RW	Reset	Description	
0xCE	SPROG_ADDR_H	RW	0000_0000Ь	Address control register	
0xCF	SPROG_ADDR_L	RW	0000_0000Ь	Address control register low 8 bits	
0xD1	SPROG_DATA	RW	0000_0000Ь	Write data register	
0xD2	0xD2 SPROG CMD RW		0000_0000Ь	Command register	
_			1101_1101b	Erase time control register	

	com	Seco	ndary bus regi	ster
Address	Name	RW	Reset	Description Description
0x5A	FLASH_BOOT_EN	R	xxxx_xxx0b	BOOT mode status selection register
0x5B	EEP_SELECT	RW	xxxx_xxx0b	DATA area selection register
0x6A	0x6A BOOT_CMD		0000_0000Ь	Program space jump instruction register
0x6B ROM_OFFSET_L		R	0000_0000ь	CODE area address offset,low 8bits
0x6C	ROM_OFFSET_H	R	0000_0000ь	CODE area address offset,high 8bits

## 17.1.1. Flash IAP Address Register

SPROG ADDR H (CEH) Address control register

Bit number	7	6	5	4	3	2	1	0	
Symbol CO				y col		y cour			
R/W			(RW)					Dolor 12	
Reset value		ben 1100				period 1100.			
		_	1115	11-0			11/25		

Bit number	Bit symbol	Description							
7~0		In Flash_Boot upgrade mode:							
		{SPROG_ADDR_H, SPROG_ADDR_L} are multiplexed into all Flash space addresses of 0x0000~0xFFFF.							

SPROG ADDR L(CFH) Address control register low 8 bits

Bit number	7	6	5	4	3	2	1	0			
Symbol		_									
R/W		R/W									
Reset value	20			1 000	Ó			1 com			

Bit number Bit symbol	ben Description	pen 01 /p.3
7~0	The lower 8 bits of the address	ning. of of J
A THE STATE OF THE		201175

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	- 1 co,	05				20	BF/S	)15CM4	4-LJTX
17.1.2. Write Data Register  SPROG_DATA(D1H)Write data register								2025-0	1.01.10.5
В	it number	7	6	5	4	3	2	1	0
	Symbol					_			
	R/W				R	/W			
R	eset value					0			
В	it number	Bit symbol Description							
	7~0	data to be written							

## 17.1.3. Command Register

SPROG CMD(D2H) Command register

2	Bit number	7	6	. 2.3	3	2	1 0 0
ر ر	Symbol			Miron Soll BAD		DILLO	15-UBYP
	R/W			R/W	7	, i	Mrs
	Reset value			0			

Bit number	Bit symbol	Description
7~0		When continuously writing data 0x12, 0x34, 0x56, 0x78, 0x9A, enter the Flash Boot upgrade mode; When continuously writing data 0xFE, 0xDC, 0xBA, 0x98, 0x76, exit the Flash Boot upgrade mode When CFG_BOOT_SEL = 3 or the program is running in a non-BOOT space, the BOOT upgrade mode cannot be entered.
	Time Control I	

# 17.1.4. Erase Time Control Register

SPROG TIM(D3H) Erase time control register

STITE STITE (SUIT) ENGINE VALUE VALU								
Bit number	7	6	5	4	3	2	1	0
Symbol	_	-	1		-	1	1	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	0	1	1	1	0	1

Bit num	iber	Bit symbol	Description
7~5	SF	PROG_TIM[7:5]	Byte write fixed time is 23.5us
Petiop;			Erase time configuration SPROG_TIM[4:0]=0-31
4~0	SF SF	PROG_TIM[4:0]	When the selected address is 0xFC00~0xFFFF:
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	210	<i>y</i>	When SPROG_TIM[4:0]=0~9,

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(1) (1) (1) (1) (1) (1) (1) (1) (1) (1)	
18 pena 01 10.30	Erase Time = 1.13 + SPROG_TIM[4:0] (ms); When SPROG_TIM[4:0]=10~31, Erase time = 9.13 (ms)
	When selecting NVR3/4 or BOOT upgrade mode: When SPROG_TIM[4:0]=0~9,
	Erase Time=0.57+0.5* SPROG_TIM[4:0] (ms);
	When SPROG_TIM[4:0]=10~31,
	Erase time=4.57(ms)

## 17.2. Secondary Bus Register

# 17.2.1. BOOT mode status register

ď	FLASH BOOT	EN (5	AH) BO	OT mode	status re	gister	2:22		ben @bya. 16:5
ning	Bit number	7	6	31/18	05401	3	2	1	nus of a line
(	Symbol	_	_	_	7772	<b>D</b> ,	_	_	FLASH_BOOT_EN
	R/W	_	_	_	_	_	_	_	R
	Reset value	_	_	_	_	_	_	_	0

Bit number	Bit symbol	Description
		1: Indicates that the Flash BOOT upgrade mode has been entered,
		0: indicates that the Flash BOOT upgrade mode has been exited.
0	FLASH_BOOT_EN	Note: In Flash BOOT upgrade mode, SPROG_ADDR_H, SPROG_ADDR_L, SPROG_DATA, SPROG_CMD,
BID		SPROG_TIM are reused as BOOT upgrade function.  {SPROG_ADDR_H, SPROG_ADDR_L} are multiplexed
		into all Flash space addresses from 0x0000 to 0xFFFF.

## 17.2.2. Program Space Jump Instruction Register

BOOT CMD (6AH) Program space jump instruction register

	boot cvib (orati) i togram space jump instruction register									
	Bit number	7	6	5	4	3	2	1	0	
	Symbol	_								
	R/W		R/W							
	Reset value	26			7 con	0			Y COIL	
(a)), (1:28:33				2007016:28:33				(1) (1) (1) (1) (1) (1) (1) (1) (1) (1)		

Bit number	Bit symbol	Description Description
05-0810	ų	Configure the program space jump instruction, write 5
/~0		groups of data (0xFF, 0x00, 0x88, 0x55, 0xAA)

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ning ben aby

continuously, jump into the main program space; write 5 groups of data (0x37, 0xC8, 0x42, 0x9A, 0x65), Jump into the Boot program space; the value read out is the byte written recently.

#### 17.2.3. CODE Area Address Offset

The read value is the actual total address offset.

ROM OFFSET L (6BH) CODE area address offset low 8bits

NOW OTTOET E (OBT) COBE area accress offsequent cons										
Bit number	7	6	5	4	3	2	1	0		
Symbol		·^						M		
R/W	25		R COR					y. Com		
Reset value	26:22	2000					6/2 / 1/2/			
PC - 110	•	per of for					VV 1110.			

Bit number	Bit symbol	Description	The apply of the state of the s				
7~0		CODE area address offset (low 8bits)					
DOM OFFGET HUGGIN CODE							

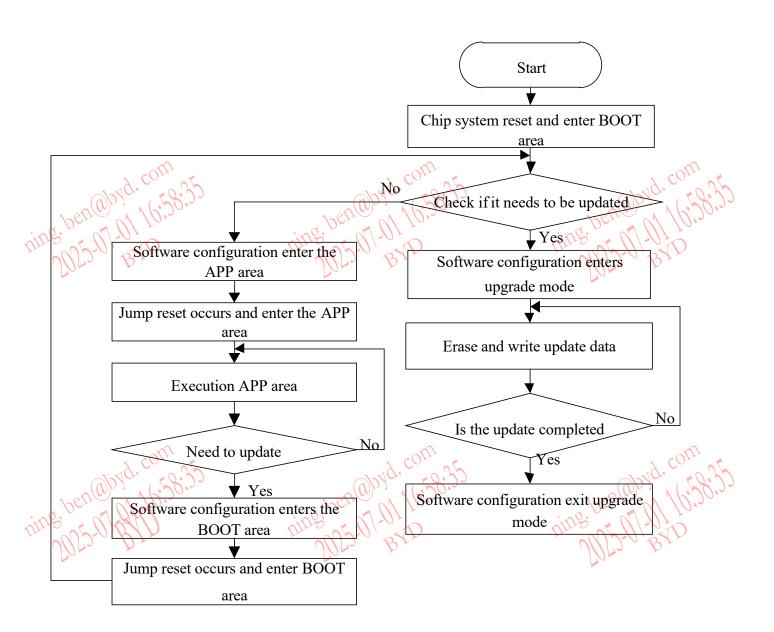
ROM_OFFSET_ H (6CH) CODE area address offset, high 8 bits								
Bit number	7	6	5	4	3	2	1	0
Symbol								
R/W		R						
Reset value				(	0			

	Bit number	Bit symbol	Description	
	7~0 <sub>2</sub> cos		CODE area address offset (high 8bits)	y cour
	2(0)p/g.		2019)(C	20p/g.
۲.	berne 10		. a perio	berne
2	RYD	\$	ins	ning.
	V F			

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# 17.3. Flash IAP Operating Procedures





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#### 17.3.1. Flash IAP Erase Step

#### In Flash BOOT upgrade mode:

- 1. SPROG\_TIM[4:0] =  $0 \sim 9$  (suggest 3ms), the byte write time is fixed at 23.5us, and it is configured only once in the main program main() function initialization;
- 2. Close interrupt;
- 3. Configure SPROG\_ADDR\_ L = 0x00;
- 4. Configure SPROG ADDR H([7:1]); select to erase the page;
- 5. Configure SPROG CMD = 0x96;
- 6. Write 4 NOP instructions;
- 7. Start erasing, the CPU turns off the clock fsys, and turns on the clock fsys after erasing is completed;
- 8. Need to continue erasing data, jump to step 2;
- 9. Configure SPROG ADDR L=0x00, SPROG ADDR H=0x00, restore interrupt settings.

#### 17.3.2. Flash IAP Byte Write Step

- 1. SPROG\_TIM[4:0] =  $0\sim9$  (suggest 3ms), the byte write time is fixed at 23.5us, and it is configured only once in the main program main() function initialization;
- 2. Close the interrupt;
- 3. Configure SPROG ADDR H, SPROG ADDR L, byte write address;
- 4. Configure SPROG DATA;
- 5. Configure SPROG CMD = 0x69;
- 6. Write 4 NOP instructions;
- 7. Start writing, the CPU turns off the clock fsys, and turns on the clock fsys after completion;
- 8. Need to continue writing data, jump to step 2; Configure SPROG\_ADDR\_L=0x00, SPROG\_ADDR\_H=0x00, restore interrupt settings;

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#### 17.3.3. Flash IAP Operation Instruction

Instruction	Instruction response status	Instruction data	
Enter upgrade mode instruction	FLASH_BOOT_EN = 1	0x12, 0x34, 0x56, 0x78, 0x9A	
Exit upgrade mode instruction	FLASH_BOOT_EN = 0	0xFE, 0xDC, 0xBA, 0x98, 0x76	
Enter the APP area instruction	ROM_OFFSETH/L	0xFF, 0x00, 0x88, 0x55, 0xAA	
Enter the BOOT area instruction	ROM_OFFSETH/L	0x37, 0xC8, 0x42, 0x9A, 0x65	

#### Instructions for operation:

- 1. Enter upgrade mode instruction: SPROG\_CMD sequential write: 0x12, 0x34, 0x56, 0x78, 0x9A;
- 2. Exit upgrade mode instruction: SPROG\_CMD sequential write: 0xFE, 0xDC, 0xBA, 0x98, 0x76;
- 3. Enter the APP area instruction: BOOT\_CMD sequential write: 0xFF, 0x00, 0x88, 0x55, 0xAA;
- 4. Enter the BOOT area instruction: BOOT\_CMD sequential write: 0x37, 0xC8, 0x42, 0x9A, 0x65;

#### Instructions response status:

FLASH BOOT EN = 1: Indicates that it has entered Flash BOOT upgrade mode,

FLASH\_BOOT\_EN = 0: Indicates that the Flash BOOT upgrade mode has been exited OM\_OFFSETH/L address offset status:

CFG BOOT SEL = 3, ROM OFFSETH/L = 0x0000// No BOOT upgrade function

CFG BOOT SEL != 3, If you are currently in the APP area:

CFG BOOT SEL = 0, ROM OFFSETH/L = 0x0800,

CFG BOOT SEL = 1, ROM OFFSETH/L = 0x1000,

CFG BOOT SEL = 2, ROM OFFSETH/L = 0x2000.

If you are currently in the boot area:

CFG BOOT SEL = 0, ROM OFFSETH/L = 0x0000.

Physical address of program execution = PC + ROM OFFSETH/L.

#### **Notes:**

- 1. When writing SPROG\_CMD, BOOT\_CMD instruction data, it must be written in order, otherwise it needs to be written again.
- 2. The working voltage of MCU is 2.7V~5.5V, and the MCU may work abnormally at 1.5V~2.7V, resulting in abnormal update and misoperation. Therefore, it is recommended not to perform IAP operation when the ADC or LVDT detection voltage is lower than 2.7V before IAP operation.
- 3. It is recommended to shield the interrupt during the update process to ensure that the IAP operation will not be affected by the interruption, and resume the interruption after the IAP operation is completed, and perform data verification after updating the data to ensure that the data is updated correctly.

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# 17.3.4. Address Correspondence In BOOT Upgrade Mode

Mary By	_	The office of the state of the	т.	The only By		
		rrespondence in BOOT upgrade mode				
SPROG_ADDR_H[7:1]	Block			corresponding range (HEX)		
4	4	00000800	>	000009FF		
5	5	00000A00	>	00000BFF		
6	6	00000C00	>	00000DFF		
7	7	00000E00	>	00000FFF		
8	8	00001000	>	000011FF		
9	9	00001200	>	000013FF		
10	10	00001400	>	000015FF		
11	11	00001600	>	000017FF		
12	12	00001800	>	000019FF		
13	13	00001A00	>	00001BFF		
14	14	00001C00	>	00001DFF		
15	15	00001E00	>	00001FFF		
16	16	00002000	>	000021FF		
17	17	00002200	>	000023FF		
18	18	00002400	>	000025FF		
19	19	00002600	>	000027FF		
20	20	00002800	>	000029FF		
21	21	00002A00	>	00002BFF		
22	22	00002C00	>	00002DFF		
23	23	00002E00	>	00002FFF		
24	24	00003000	>	000031FF		
25	25	00003200	>	000033FF		
26	26	00003400	>	000035FF		
27	27	00003600	>	000037FF		
28	28	00003800	>	000039FF		
29	29	00003A00	>	00003BFF		
30	30	00003C00	>	00003DFF		
31	31	00003E00	>	00003FFF		
32	32	00004000	>	000041FF		
33	33	00004200	>	000043FF		
34	34	00004400	>	000045FF		
35	35	00004600	>	000047FF		
36	36	00004800	>	000049FF		
37	37	00004A00	>	00004BFF		
	5,					

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(0), (0)				
Den (138)	38	00004C00	>	00004DFF
39	39	00004E00	>	00004FFF
40	40	00005000	>	000051FF
41	41	00005200	>	000053FF
42	42	00005400	>	000055FF
43	43	00005600	>	000057FF
44	44	00005800	>	000059FF
45	45	00005A00	>	00005BFF
46	46	00005C00	>	00005DFF
47	47	00005E00	>	00005FFF
48	48	00006000	>	000061FF
49	49	00006200	>	000063FF
50	50	00006400	>	000065FF
51	51	00006600	>	000067FF
52	52	00006800	>	000069FF
53	53	00006A00	>	00006BFF
54	54	00006C00	>	00006DFF
55	55	00006E00	>	00006FFF
56	56	00007000	>	000071FF
57	57	00007200	>	000073FF
58	58	00007400	>	000075FF
59	59	00007600	>	000077FF
60	60	00007800	>	000079FF
61	61	00007A00	>	00007BFF
62	62	00007C00	>	00007DFF
63	63	00007E00	>	00007FFF
64	64	0008000	>	000081FF
65	65	00008200	>	000083FF
66	66	00008400	>	000085FF
67	67	00008600	>	000087FF
68	68	0008800	>	000089FF
69	69	00008A00	>	00008BFF
70	70	00008C00	>	00008DFF
71	71	00008E00	>	00008FFF
72	72	00009000	>	000091FF
73	73	00009200	>	000093FF
74	74	00009400	>	000095FF
75	75	00009600	>	000097FF

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(0))				
berry 1763.3	76	00009800	>	000099FF
77	77	00009A00	>	00009BFF
78	78	00009C00	>	00009DFF
79	79	00009E00	>	00009FFF
80	80	0000A000	>	0000A1FF
81	81	0000A200	>	0000A3FF
82	82	0000A400	>	0000A5FF
83	83	0000A600	>	0000A7FF
84	84	0000A800	>	0000A9FF
85	85	0000AA00	>	0000ABFF
86	86	0000AC00	>	0000ADFF
87	87	0000AE00	>	0000AFFF
88	88	0000B000	>	0000B1FF
89	89	0000B200	>	0000B3FF
90	90	0000B400	>	0000B5FF
91	91	0000B600	>	0000B7FF
92	92	0000B800	>	0000B9FF
93	93	0000BA00	>	0000BBFF
94	94	0000BC00	>	0000BDFF
95	95	0000BE00	>	0000BFFF
96	96	0000C000	>	0000C1FF
97	97	0000C200	>	0000C3FF
98	98	0000C400	>	0000C5FF
99	99	0000C600	>	0000C7FF
100	100	0000C800	>	0000C9FF
101	101	0000CA00	>	0000CBFF
102	102	0000CC00	>	0000CDFF
103	103	0000CE00	>	0000CFFF
104	104	0000D000	>	0000D1FF
105	105	0000D200	>	0000D3FF
106	106	0000D400	>	0000D5FF
107	107	0000D600	>	0000D7FF
108	108	0000D800	>	0000D9FF
109	109	0000DA00	>	0000DBFF
110	110	0000DC00	>	0000DDFF
111	111	0000DE00	>	0000DFFF
112	112	0000E000	>	0000E1FF
113	113	0000E200	>	0000E3FF

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(0)				
hen 114	114	0000E400	>	0000E5FF
115	115	0000E600	>	0000E7FF
116	116	0000E800	>	0000E9FF
117	117	0000EA00	>	0000EBFF
118	118	0000EC00	>	0000EDFF
119	119	0000EE00	>	0000EFFF
120	120	0000F000	>	0000F1FF
121	121	0000F200	>	0000F3FF
122	122	0000F400	>	0000F5FF
123	123	0000F600	>	0000F7FF
124	124	0000F800	>	0000F9FF
125	125	0000FA00	>	0000FBFF

#### Notes:

- 1. Byte write physical address corresponding register: {SPROG\_ADDR\_H[7:0], SPROG\_ADDR\_L[7:0]};
- 2. 512 Bytes per Block;
- 3. When operating the 2K/4K/8K Block in the area where the BOOT is located, the BOOT is write-protected and the operation is invalid.
- 4. When the BOOT function is used, the absolute address of all CODE areas of the program needs to be subtracted from the offset address of ROM\_OFFSET\_H/L (PC ROM\_OFFSET), and then the absolute address of the CODE area is accessed.

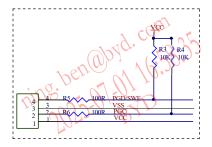
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18. Burning and Debugging

### 18.1. SWE Circuit Connection

Two-wire programming and single-wire debugging. When performing simulation debugging, you need to connect a SWE wire. In the SWE debugging mode, the IO function of the SWE port is blocked. It is recommended not to configure other functions of the SWE debugging IO port to avoid affecting the SWE debugging function.



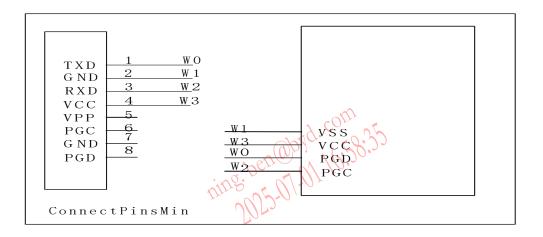
SWE circuit connection reference diagram

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# 18.2. Burning and Debugging Den Miles

Connect the chip PGC, PGD, VCC, VSS four lines. When entering the programming interface, select the chip of the corresponding model. Open the compiled HEX file, click on a built-in flash to wait for burning.



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19. CPU Instruction System. bendly 19.1 Instruction

### 19.1. Instruction Code

The BF7515CM44-LJTX instructions are divided into signal-byte instructions, double-byte instructions and three-byte instructions.

Signal-byte instructions: A signal-byte instruction consists of 8 bit binary code. There are only instruction opcodes in the instruction, no instruction operand or instruction operand is implied in the instruction opcode. There are 49 such instructions.

Double-byte instructions: Consists of two bytes, one for opcode and the other for the operand (or operand address), stored in order in program memory. There are 46 such instructions.

Three-byte instructions: Consists of one byte of instruction opcode and two bytes of operands (or operand address). There are 16 such instructions.

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# 19.2. Instruction Set

In order to describe the instructions conveniently, some symbols are used in the instructions. The meanings of these symbols are as follows:

Addr 11	Low 11 bit address
addr 16	16 bit address
direct	Direct addressing, 8 bit internal data and address(including SFR)
bit	Bit address
#data	8 bit immediate
#data16	16 bit immediate
rel	Signed 8 bit relative displacement
n	Number 0~7
Rn	R0~R7 working register of the current register bank
i	Number 0, 1
Ri	working register R0, R1
@	Register indirect addressing
<b>←</b>	Data transfer direction
	LOgic 'and,
	LOgic 'Or,
	LOgic 'xOr,
$\checkmark$	Have an effect on the flag
×	No effect on the flag

CPU instruction symbol table

Provides the assembly instructions used, the function of each instruction, the number of bytes occupied, the execution cycle of the instruction, and the effect on the corresponding flags:

8 bit data t	ransfer instructiio	on ing bering				*.00	18. pc. 1	Ul In.
102-0 B/D		MIND BYD	In	Impact on the fla			Number	Cycle
IMI	nemonic	Function	P	OV	AC	CY	of bytes	number
	Rn	A←(Rn)		×	×	×	1	1
MOVA	direct	A←(dir ec t)		×	×	×	2	1
MOV A	@Ri	A←((Ri) )		×	×	×	1	1
	#data	A←data		×	×	×	2	1
	A	Rn←(A)	×	×	×	×	1	1
MOV Rn	direct	Rn←(dir ec t)	×	×	×	×	2	2
	#data	Rn←data	×	×	×	×	2	1
MOV	A	dir ec t1←( A)	×	×	×	×	2	1
MOV	Rn	dir ec t1←( R n)	×	×	×	×	2	1
direct1	direct2	dir ec t1←( d ir	×	×	×	×	3	2
MOV \	@Ri	dir ec t←((Ri)	×	×	×	×	2	2
direct	#data	dir ec t←data	×	×	×	×	3	1

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pents M	<b>W</b> .3	(Ri) ←(A)	×	×	×	×	1	1
MOV	direct	$(Ri) \leftarrow (direc\ t$	×	×	×	×	2	2
@Ri	#data	(Ri) ←da ta	×	×	×	×	2	1

### 16 bit data transfer instruction

M	F4:	Im	pact o	n the	flag	Number	Cycle	
Mnemonic	Function	P	OV	AC	CY	of bytes	number	
MOV DPTR,#data16	DP TR←dat a16		×	×	×	3	1	

External data transfer and table lookup instructions

M		г .:	Im	pact o	n the	flag	Number	Cycle
Min	nemonic	Function	P	OV	AC	CY	ofbytes	number
MOVX (	@DPTR,A	(DP TR )←( A)	×	×	×	×	1	1
MOVC	@A+DPTR	$A \leftarrow ((A) + (D P TR)$	<b>\</b>	×	×	×	1	1 , 0
A,	@A+PC	$A \leftarrow ((A) + (P C))$	7	×	×	×	1	1 //:
MOVX A,	@DPTR	A←(DP T R)	~	×	×	×	4050	1

Notes: The number of cycles and the number of bytes of the MOVX instruction can be configured through registers CKCON<2:0>.

# Exchange class instruction

3.6		г .:	In	npact o	on the	flag	Number	Cycle
Mn	emonic	Function	P	OV	AC	CY	of bytes	number
	Rn	(Rn)←( A)		×	×	×	1	1
XCH A,	direct	(A)←( di rect )		×	×	×	2	2
XCH A,	@Ri	(A)←( (Ri )) ∧	×	×	×	×	1	2
XCHD A,	@Ri	(A)3~0~((Ri))3~0	V	×	×	×	1	2).
SWAP A	16:20.3	(A)7-4~(A)3-0	100	×	×	×	1,000	1 16.5
40.	70	110. 11.10					170.	1.1 100

## Arithmetic operation instruction

152-01P	emonic	DOD-O'BYD	Im	pact o	n the	flag	Number	Cycle
IVIII	lemonic	Function	P	OV	AC	CY	of bytes	number
	Rn	$A \leftarrow (A) + (Rn)$		$\checkmark$	$\checkmark$	$\checkmark$	1	1
	direct	$A \leftarrow (A) + (di re c)$		$\checkmark$	$\checkmark$	$\checkmark$	2	2
ADD A,	@Ri	$A \leftarrow (A) + ((R i))$		$\checkmark$	$\checkmark$	$\checkmark$	1	2
	#data	A←(A)+data		$\checkmark$	$\checkmark$	$\checkmark$	2	1
	Rn	$A \leftarrow (A) + (Rn) + ($		$\checkmark$	$\checkmark$	$\checkmark$	1	1
ADDC	direct	$A \leftarrow (A) + (di re c)$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	2	2
A,	@Ri	$A \leftarrow (A) + ((R i))$		$\checkmark$	$\checkmark$	$\checkmark$	1	2
,	#data	$A \leftarrow (A) + data + ($		$\checkmark$	$\checkmark$	$\checkmark$	2	1
	A	$A \leftarrow (A) + 1$		×	×	×	1	1
INC	Rn	$Rn \leftarrow (Rn)+1$	×	×	×	×	1	1
B	direct	dir ec t←( d ire	×	×	×	×	2	2

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	·   • · / / / ·							
pen of	@Ri	$(Ri) \leftarrow ((Ri)) +$	×	×	×	×	1	2
2501-0	DPTR	$DP TR \leftarrow ((D P TR)$	×	×	×	×	1	2
DA A		BCD code adjustment	$\checkmark$	×	$\checkmark$	$\checkmark$	1	1
	Rn	A←( A-( <b>R</b> n)-(C)	$\checkmark$	×	×	×	1	1
CLIDD A	direct	$A \leftarrow (A-(direct)-(C)$		$\checkmark$	$\checkmark$	$\checkmark$	2	2
SUBB A	@Ri	$(A) \leftarrow -((RAi))-(C)$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	1	2
	#data	$A \leftarrow (A-d) ta-(C)$		$\checkmark$	$\checkmark$	$\checkmark$	2	1
	A	A←( A-1)		×	×	×	1	1
DEC	Rn	$Rn \leftarrow (R-1n)$	×	×	×	×	1	1
DEC	direct	$dir ec t \leftarrow l(dire)$	×	×	×	×	2	2
	@Ri	$(Ri) \leftarrow (Ri)$	×	×	×	×	1	2
MUL AB		BA ←(A) *ft(erB), performing the multiplication operation, the lower byte is stored in A and the high byte is stored in B.	~	<b>√</b>	×	0	10250	1 16:3
DIV AB		$A \leftarrow (A)/(r^B m) aind B_r$		$\sqrt{}$	×	0	1	1

Notes: When the DA instruction is used, the adjustment rules are as follows: if the low 4 bits of accumulat or A are greater than 9 or AC = 1 are greater than 9 or CY = 1, then  $A \leftarrow A + 60H$ 

Logical op	eration instructio	n						
Mar		Engation of	In	npact o	on the	flag	Number	Cycle
lyin	nemonic	Function	P	OV	AC	CY	ofbytes	number
CLRA	16:58:33	A←00H	5	×	×	×	1 00	1
CPL A	4	$A \leftarrow (\overline{A})_{0}g$	$\checkmark$	×	×	×	a //	M/ 10.
USD-0.P	Rn	$A \leftarrow (A)(Rn)$	<b>√</b>	×	×	×	4002-0	1
ANILA	direct	$A \leftarrow (A)$ (direct)		×	×	×	2	2
ANL A,	@Ri	$A \leftarrow (A)((Ri))$	$\checkmark$	×	×	×	1	2
	#data	A←(A)data		×	×	×	2	1
ANL	A	dir ec t (dir(ecAt))	×	×	×	×	2	2
direct,	#data	dir ec t←(da¶aire	×	×	×	×	3	2
	Rn	$A \leftarrow (A)(Rn)$	~	×	×	×	1	1
ODIA	direct	$A \leftarrow (A)$ (direct)	~	×	×	×	2	2
ORL A,	@Ri	$A \leftarrow (A)((Ri))$		×	×	×	1	2
	#data	A←(A)data	$\checkmark$	×	×	×	2	1
ORL	A	dir ec t←(Ad) ire	×	×	×	×	2	2
direct,	#data	dir ec t←(dalaire	×	×	×	×	3	2
XRL A,	Rn	$A \leftarrow (A)(Rn)$		×	×	×	1	1

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(a) D/2	(6.58:33							
period W	direct	$A \leftarrow (A)$ (direct)		×	×	×	2	2
25-01-0	@Ri	$A \leftarrow (A)((Ri))$	$\sim$	×	×	×	1	2
	#data	A←(A)data		×	×	×	2	1
XRL	A	dir ec t←(Ad) ire	×	×	×	×	2	2
direct,	#data	dir ec t←(da⁴aire	×	×	×	×	3	2
Loop, shift	class instruction							
Mn	emonic	Function	In	npact o	on the	flag	Number	Cycle
1V111	lemonic	runction	P	OV	AC	CY	of bytes	number
RL A		The content in A is rotated left by one bit.	×	×	×	×	1	1
RLC A		A content with carry left shift one bit.	<b>√</b>	×	×	<b>√</b>	1	1
RR A		The content in A is rotated right by one bit.	×	×	×	×	1	1
RRC A		A content with carry right shift one bit.	<b>√</b>	×	×	<b>√</b>	1	1
Call, return	class instruction	1						
Mn	emonic	Function	In	npact o	on the	flag	Number	Cycle
1411		1 direction	P	OV	AC	CY	of bytes	number
		(PC)←( PC )+3,						
LCALL ad	dr16	(SP)←( PC ),	×	×	×	×	3	2
		(PC)←add r16						
		$(PC)\leftarrow (PC)+2,$						
ACALL ad	dr11	$(SP) \leftarrow (PC),$	×	×	×	×	2	2
DET		$(PC10\sim0)\leftarrow add$	.,	.,			1	2
RET		$(PC)\leftarrow ((SP))$	×	×	×	×	1	2
RETI		(PC)←( retu§nPfrom) interrupt	×	×	×	×	1	2
Transfer cla	ass instruction							
Mn	emonic	Function		ipact o			Number	Cycle
			P	OV	AC	CY	of bytes	number
	dr16	$PC \leftarrow add \ r \ 15 \sim 0$	×	×	×	×	3	2
	dr11	PC $10 \sim 0 \leftarrow a \ dd \ r1$	×	×	×	×	2	2
	el	$PC \leftarrow (PC) + r \ el$	×	×	×	×	2	2
JMP @	A+DPTR	$PC \leftarrow (A) + (DP TR)$	×	×	×	×	1	1
		$PC \leftarrow (P \ C, )+2$						
JZ rel		if(A)=0,	×	×	×	×	2	2
		$PC \leftarrow (PC) + r \ el$						
JNZ rel	<u> </u>	$PC \leftarrow (P \ C, )+2$ $if(A) \neq 0,$	×	×	×	×	2	2

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 $PC \leftarrow (PC) + r el$  $PC \leftarrow (P \ C, )+2$ JC if(CY)=1, rel 2 2 × X ×  $PC \leftarrow (PC) + r$  el  $PC \leftarrow (P C, )+2$ JNC if(CY)=0, 2 rel 2 × X ×  $PC \leftarrow (PC) + r \ el$  $PC \leftarrow (P C, )+3$ JBbit,rel if(bit)=1, × 3 2 X X  $PC \leftarrow (PC) + r el$  $PC \leftarrow (P \ C, )+3$ JNB bit,rel if(bit)=0, 3 2 X X X  $PC \leftarrow (PC) + r \ el$  $PC \leftarrow (P \ C, )+3$ JBC bit,rel if(bit)=1, then bit,  $\leftarrow 0$ 2 3 ×  $PC \leftarrow (PC) + r \ el$  $PC \leftarrow (P \ C, )+3$ if(A) \( \neq t \text{den} \) rect A, direct, rel 2 X × X 3 PC(PC)+rel  $if(A) < (direct), then CY \leftarrow 1$  $PC \leftarrow (P C, )+3$  $if(A) \neq data$ A,#data,rel then PC(PC)+rel 3 2 X X X if(A) < (data),thenCY  $\leftarrow 1$ **CJNE**  $PC \leftarrow (P \ C, )+3$  $if(Rn) \neq data$ Rn,#data,rel then 3 2 × X ×  $PC \leftarrow (PC) + r el$ if(Rn)<(data), then CY  $\leftarrow$ 1  $PC \leftarrow (P C, i)((Ri)3)$ ≠dat a @Ri,#data,rel 2 3 X X X Then PC  $\leftarrow$  (PC)+r if((Ri)) $\leq$ (data),then CY  $\leftarrow$ 1  $PC \leftarrow (PC) + 2, -lR, n$ Rn,rel if(Rn), the  $\neq 0$ 2 2 × X X  $PC \leftarrow (PC) + r el$ DJNZ  $PC \leftarrow (PC) + 3$ direct,rel (di rect -)1, $\leftarrow$ ( di × 3 2 X X X If  $(direct) \neq 0$ ,

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	~ ( ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~		<u> </u>	100				( <u>L</u> V)	1.70		
5	perio 1/0.3		Then $PC \leftarrow (PC) + r$					a perio	170.2		
(C)	Stack, empty operation class instruction						DIL	18 75-0			
( )	Mnemonic PUSH direct		Function	Impact on the f			flag	Number	Cycle		
			Tunction		OV	AC	CY	of bytes	number		
			$SP \leftarrow (SP) + 1, (SP) + 1$	×	×	×	×	2	2		
	POP direct		dir ec t←( S P1),	×	×	×	×	2	2		
	NOP		empty operation	×	×	×	×	1	1		
	Bit manipulation in	struction	1								
	Mnemonic		Function	Impact on the		flag Number		Cycle			
	IVITICITIONIC		Tunction	P	OV	AC	CY	ofbytes	number		
	MOV	C,bit	CY ←bit	×	×	×	$\sqrt{}$		2		
	IVIOV	bit,C	bit ←CY	×	×	×	×	2	2		
	CLR	C	CY ←0	×	×	×	<b>√</b>	1	1/20		
		bit	bit ←0	×	×	×	×	2	2		
	SETB	С	CY ←1	×	×	×	<b>√</b>	J///72.0	1		
		bit	bit ←1	×	×	×	×	2	2		
	CPL	С	$CY \leftarrow \overline{(Y)}$	×	×	×	<b>√</b>	1	1		
	CIL	bit	bit bi—t)(	×	×	×	×	2	2		
	ANL	C,bit	$C \leftarrow (C \text{ bit})$	×	×	×	<b>√</b>	2	2		
	ANL	C ,/bit	$C \leftarrow (C \mid bit)$	×	×	×	√	2	2		
	ORL	C,bit	$C \leftarrow (C \text{ bit})$	×	×	×	<b>√</b>	2	2		
	OKL	C,/bit	C←(C \bit)	×	×	×	<b>√</b>	2	2		
	Pseudo-instruction										
	Mnemonic	Instruction format			Function Description						
ORG tab:			ORG addr16		Define the first address of tab						
5	EQU	tab EQ	tab EQU data/tab			Assign values to labels					
0	DB	tab:	DB item or item tabel	De	Define a-byte or multi-byte						
	DW	tab: DW item or item tabel			16 bit word content used to define two or more cells in memory						
	DS	tab: DS expression			Specifies to leave several memory cells starting with the label						
BIT tab BIT			Assign a bit address to a label								
END is placed at the end of the assembly language program to tell the assembler that the source program ends here.					e						

CPU instruction set table



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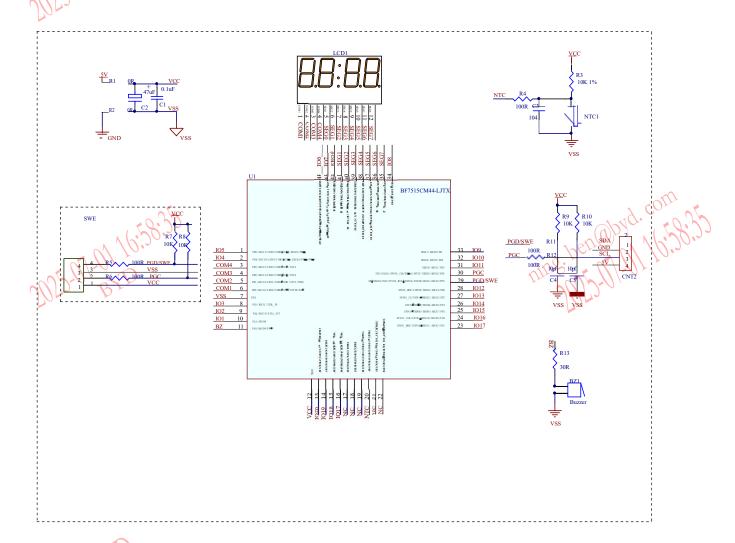
CPU related register		ď	ben Obya. 16	19:33 pen @pyle 10:28	
DIUS	SFR regis	ter	ning	75-10-20	ning of Old
C	Address	Name	RW	Reset	Description
	0x81	SP	RW	0x07	Stack pointer register
	0x82	DPL	RW	0x00	Data pointer register 0 low 8 bit
	0x83	DPH	RW	0x00	Data pointer register 0 high 8 bit
	0x87	PCON	RW	0x00	Idle mode 1 select register
	0xE0	ACC	RW	0x00	Accumulator
	0xF0	В	RW	0x00	B register

CPU SFR register list

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# 20. Reference Application Circuit



Note: the above reference schematic reference circuit is only for reference design.

- 1. SWE debugging peripheral circuit only SWE adjustment trial, if there is a pull-up resistor on the simulator or adapter board, there is no need to connect the SWE pull-up resistor.
- 2. Replace the  $0\Omega$  resistance of the power supply and ground in parallel with magnetic beads. The EMI test item (RE) can increase the test margin. The recommended parameter is  $600~\Omega@100 MHz$ .

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RARARARARA

122

30

30

m -

D

III 12

EI 

BASE METAL

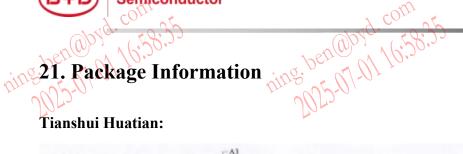
ning. ben abyd. com
2025-07-01 16:58:35

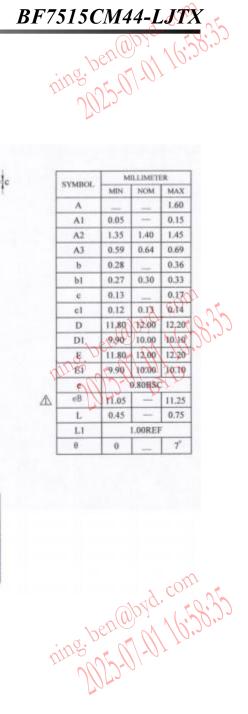
Ejector hole

WITH PLATING

SECTION B-B

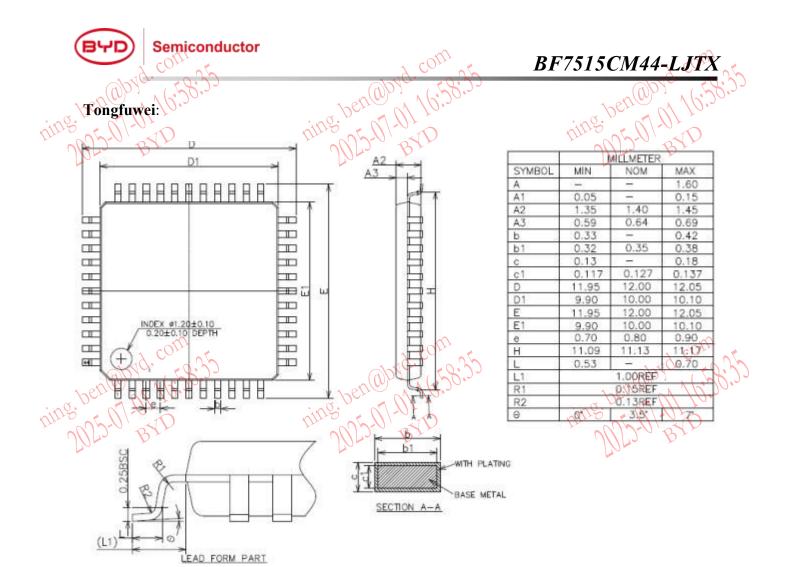
Front ejector hole . 1.2mm







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Bin

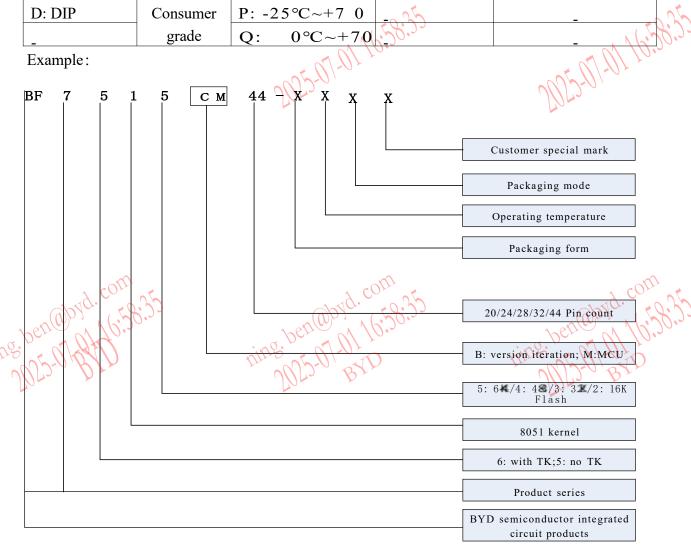
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# **Ordering Information**

'	Copy	of C	A C	oth of H	BF7515CM44-L <b>JT</b> X
20	Ordering Inf	ormation	ning. ben@bya. 1	) ?:28:33	ning ben @by BYD
Package Wor		Worl	k temperature Package style		Keep the follow-up
	S: SOP		A: -40°C~+ 15	B: tap	_
	A: SSOP	C 1	B: -40°C~+ 12	L: feed tube	_
	T: TSSOP	Car grade	C: -40°C~+ 10	T: tray	_
	M: MSSOP		D: -40°C~+ 85	_	_
	L: LQFP		K: -40°C~+ 85	_	_
	Q: QFN	Industrial grade	J: -40°C~+1 05	_	_
	B: BGA		L: -40°C~+1 2	_	_
	D: DIP	Consumer	P: -25°C~+7 0	-025	
	_	grade	Q: 0°C~+70	<i>:28:</i> 33	

Example:





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# **Revision Record**

Revision date	Revised content	Reviser	Remarks
2021-12-31	V1.0	JYY	V1.0
2022-01-19	<ol> <li>Update features</li> <li>Update memory description</li> <li>Update low power current</li> <li>Update clock block diagram</li> <li>Update header</li> </ol>	YNN	V1.1
2022-06-07	<ol> <li>Update the working mode</li> <li>Update the IO structure diagram</li> <li>Update the description of LCD COM*SEG correspondence table</li> <li>Update the LVDT configuration process</li> <li>Update the description of registers 0x58, 0x65, 0xB1</li> </ol>	YNN	V1.2
2022-10-25	<ol> <li>Add limit parameter description</li> <li>Delete the maximum and minimum values of high current in DC characteristics</li> <li>Update the description of "LED dot matrix drive LEDX arrangement order"</li> <li>Update the description of secondary bus register 0x23</li> <li>Add DATA area erase instructions</li> </ol>	YNN	V1.3

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