Built-in 12 Bit ADC/16 Bit PWM/Touch Key/64K FLASH 8-bit MCU

CA51F155 Series MCU

User Guide

REV1.0

Directory

1 Introduction

The CA51F155 series chip is an 8-bit microcontroller based on the 1T 8051 core, which not only retains the basic characteristics of traditional 8051 chips, but also runs 10 times faster than traditional 8051 chips in general, with superior performance. The chip is equipped with a 64KB Flash program memory, which can be programmed multiple times, and a 2KB SRAM to facilitate customer development of complex applications. It also integrates 46 channels of 12 Bit ADC, 46 channels of Touch Key (without external capacitors), 6 channels of 16 Bit PWM, maximum support for 8com x 32seg LCD/LED driver, I2C, UART, SPI, TMC, low voltage detection (LVD), 2 comparators and other functional modules. Support PWM, I2C, UART peripherals to be mapped to any pin, support 8 high current pins, software can achieve dual scan LED screen display function, and also support IDLE, STOP, and low-speed operation three power-saving modes to adapt to applications with different power consumption requirements. Its powerful functions and superior anti-interference performance make it widely applicable in household appliances.

2 Basic Features

- Core
  - CPU: 1T 8051, up to 10 times faster than traditional 8051
  - Compatible with 8051 instruction set, dual DPTR operation mode
- Memory
  - Flash: 64K bytes, supports multiple rewrites
  - Flash can be divided into program area and data area, the data area can be used to save data that needs to be saved after power down
  - RAM:256 bytes of internal RAM, 2K bytes of external RAM
- Operating Voltage
  - Operating voltage: 2.7V ~ 5.5V@Fosc=12MHz
2.2V ~ 5.5V@Fosc=6MHz
- Operating temperature
  - Operating temperature: -40℃~+85℃
- Clock System
  - External low-speed oscillator: 32.768KHz
  - Built in low-speed RC oscillator: 128KHz
  - Built in high-speed RC oscillator: 12MHz, accuracy of ± 2% @ 5V/25℃ (factory calibrated)
- Timer
  - Three 16-bit general-purpose timers: Timer 0, Timer 1, Timer 2
- General purpose input and output ports (GPIO)
  - Supports up to 46 GPIO ports (different models may vary)
  - Supports push-pull, open drain, pull-up (30K), pull-down (30K), and high resistance modes

- When pushing and pulling output, the maximum current of a single GPIO source can reach 15ma@5v The maximum current can reach 40ma@5v
- 8 high current GPIOs (P3.0~P3.7), with a maximum current of up to 90ma@5v , can be used for bright LED screen display

◆ TMC Functions

- The clock source of TMC timer can be selected as IRCL or XOSCL
- The smallest unit of interruption time, when selecting IRCL as the clock source, it is 512 IRCL clock cycles, and when selecting XOSCL as the clock source, it is 128 XOSCL clock cycles
- Configurable interrupt time from 1 to 256 minimum units of time

◆ Interrupt system

- 7 valid interrupt sources
- Two levels of interrupt priority, supporting nested interrupts
- 5 external interrupt sources INT0~INT4
- External interrupt triggering edge selection: INT0~1 (rising edge, falling edge), INT2~4 (rising edge, falling edge, double edge)
- Interrupt input pin selection: INT0 (P0.0), INT1 (P0.1), INT2 (P0.2), INT3 (P0.3), INT4. Any GPIO pin except for P0.0~P0.3 can be selected as the interrupt input pin

◆ Analog/Digital Converters (ADC/DAC)

- Support 46 channel 12 bit SAR ADCs (different models may vary)
- Supports two reference voltage sources: VDD and internal reference
- Selecting internal voltage as the reference, VDD voltage can be measured

◆ Touch Key

- Built in touch sensing controller
- Supports up to 46 touch channels (different models may have differences), without the need for external capacitors
- High anti-interference performance, in compliance with EMC standards
- Support touch interruption
- Support touch low-power mode

◆ PWM

- Supports 6 PWM outputs, each of which can be individually controlled, and the cycle and duty cycle can be freely configured within a 16 bit range
- Support complementary mode and dead zone mode, and support setting edge alignment and center alignment modes
- Support for direct output of internal clock function
- Support PWM interrupt function
- Each PWM output pin can be mapped to different GPIO pins

◆ LCD drive

- Maximum support 8com x 32seg、7com x 33seg、6com x 34seg、5com x 35seg、4com x 36seg

- Configurable duty cycle: 1/2, 1/3, 1/4, 1/5, 1/6, 1/7, 1/8 Duty
- Configurable bias voltage: 1/2, 1/3, 1/4 Bias
- Supports 8-level contrast adjustment
- Supports 8-level driving current (5uA, 40uA, 80uA, 130uA, 200uA, 320uA, 450uA, 600uA), and users can adjust according to different LCD screens

◆ LED drive
- Supports up to 8com x 32seg
- Supports 8-level brightness adjustment

◆ Analog comparator
- Built in 2 analog comparators

◆ Universal Serial Interface (UART0/UART1/UART2)
- Supports 3 full duplex serial ports
- Support 1-byte receive cache
- The TX/RX of UART0/UART1/UART2 can be mapped to different GPIO pins

◆ I^2C interface
- Built in 1 I2C interface, supporting master-slave mode, standard/fast/high-speed mode
- I2C pin SCL/SDA can be mapped to any GPIO pin

◆ SPI interface
- Built in 1 4-wire SPI interface, supporting master-slave mode

◆ Low voltage detection (LVD)
- The detection voltage can be set to 2.2V, 2.5V, 2.7V, 3.0V, 3.3V, 3.6V, 3.9V, and 4.2V.
- Low voltage reset or interrupt can be set

◆ Reset mode
- The chip supports multiple reset sources: power on/power off reset, soft reset, hard reset, watchdog reset, low voltage detection reset

◆ Watchdog
- 27 bit watchdog timer, 16 bit adjustment accuracy, configurable watchdog reset or interrupt

◆ Program download and simulation
- Support ISP and IAP
- Support online simulation function

◆ Low power consumption
- STOP mode, current<7uA
- IDLE mode, current<55uA
- Low speed operation mode, current<90uA

◆ Package Type : LQFP48/LQFP44/LQFP32/SOP28

3 Chip Model Function Introduction

Table 3-1 CA51F155 series specific model functional characteristics

Chip Model	Flash Capacity[BYTE]	SRam[BYTE]	Internal high-speed RC oscillator	Internal low-speed RC oscillator	external oscillator[32.768KHz]	Number of GPIO	Number of universal 16 bit timers	UART quantity	I²C	SPI	Number of 16 bit PWM channels	Touch key	Number of 12-bit ADC channels	LCD drive[com X seg]	LED drive [com X seg]	Analog Comparator	On-chip emulation functions	Operating Voltage [V]	Package form
CA51F155L0	64K	2K	√	√	√	30	3	3	1	1	6	30	30	8x17 7x18 6x19 5x20 4x21	8x17	2	√	2.2~5.5	LQFP32 (7x7mm)
CA51F155L1	64K	2K	√	√	√	42	3	3	1	1	6	42	42	8x28 7x29 6x30 5x31 4x32	8x28	2	√	2.2~5.5	LQFP44 (10x10mm)
CA51F155L2	64K	2K	√	√	√	46	3	3	1	1	6	46	46	8x32 7x33 6x34 5x35 4x36	8x32	2	√	2.2~5.5	LQFP48 (7x7mm)
CA51F155S6A	64K	2K	√	√	√	26	3	3	1	1	6	26	26	8x12 7x13 6x14 5x15 4x16	8x12	2	√	2.2~5.5	SOP28
CA51F155S6B	64K	2K	√	√	√	26	3	3	1	1	6	26	26	8x12 7x13 6x14 5x15 4x16	8x12	2	√	2.2~5.5	SOP28

4 System Block Diagram

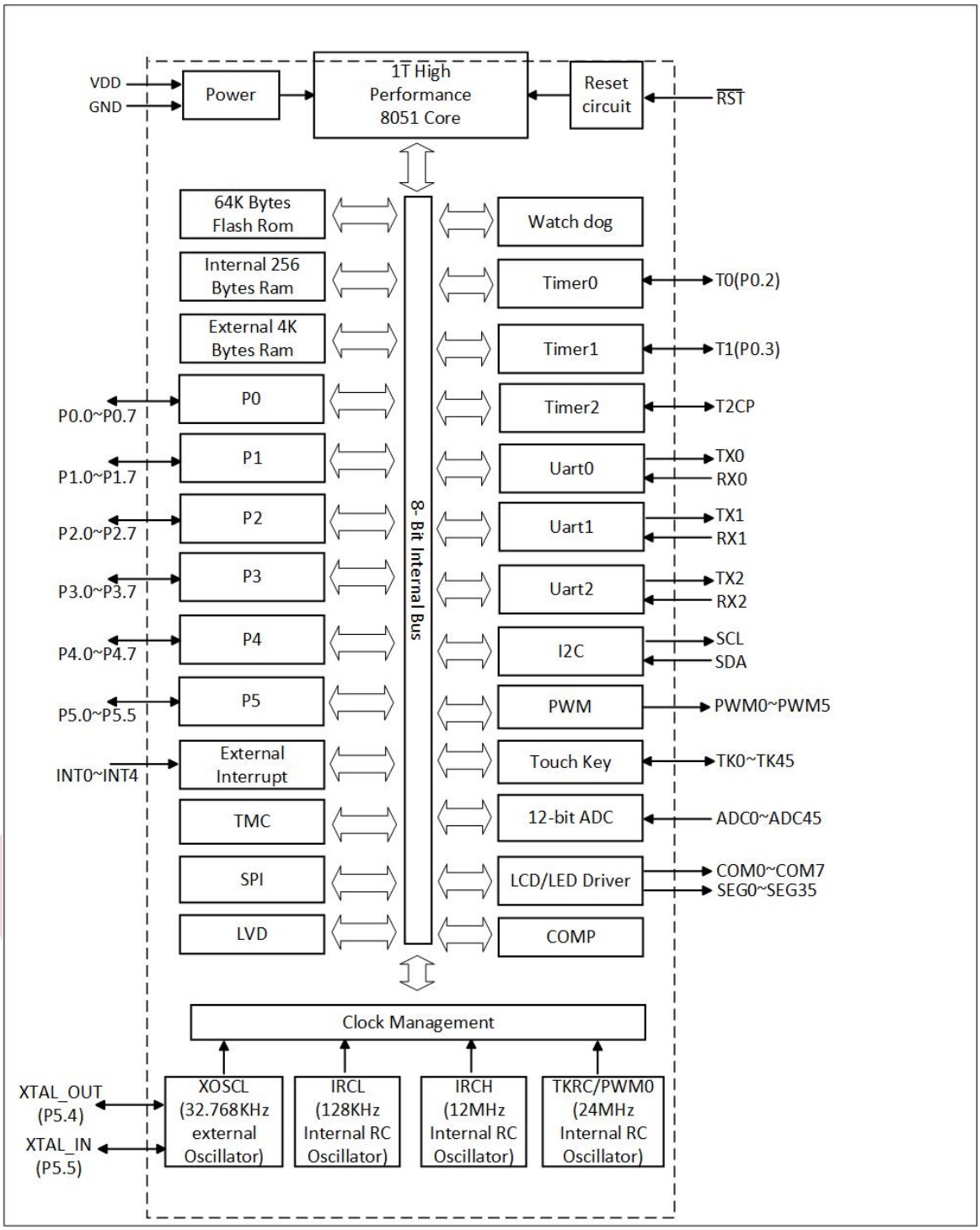


Figure 4-1 Chip Block Diagram

5 Pinout Packages and their Descriptions

5.1 Package Definition

Model：CA51F155L2

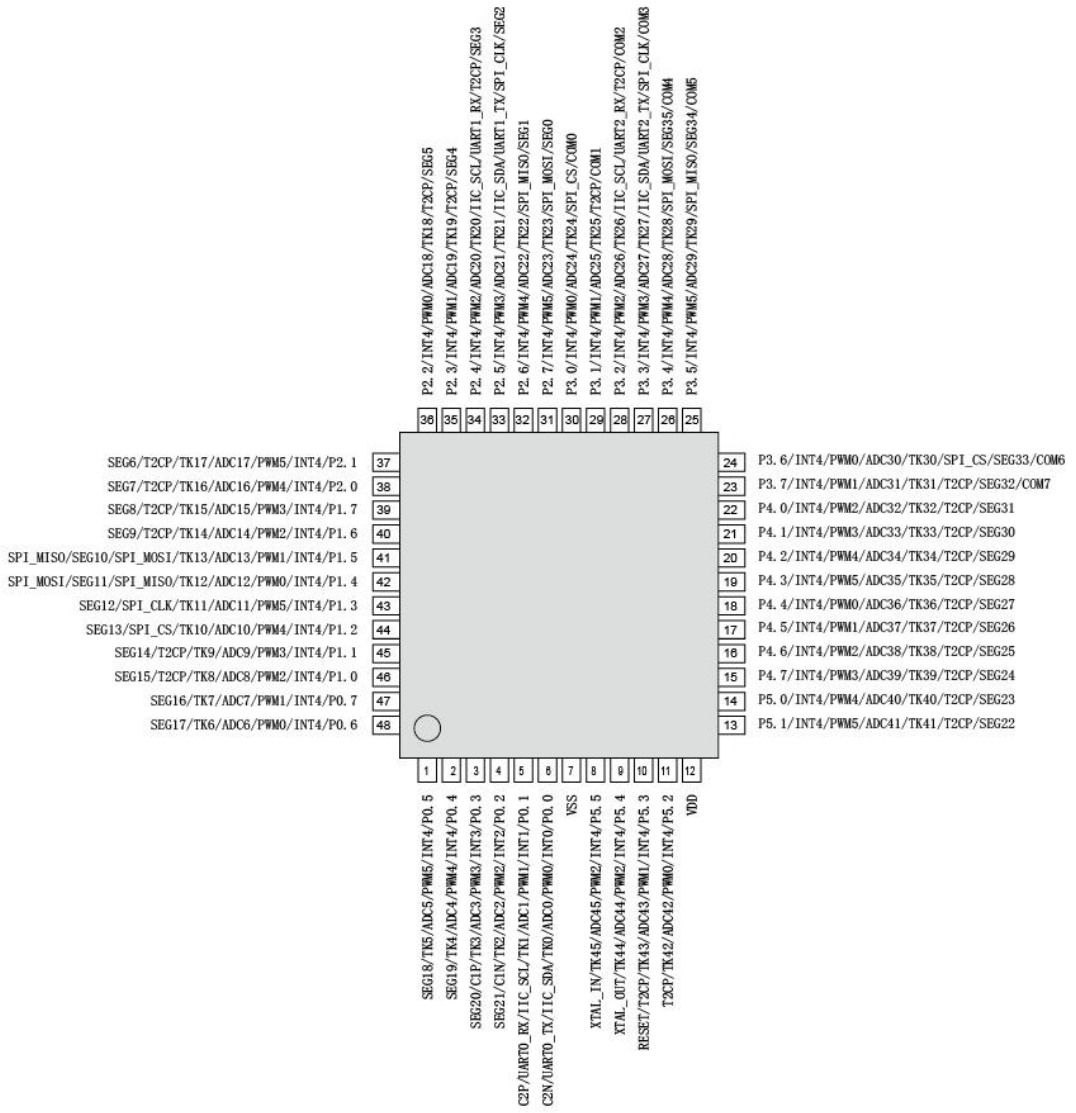


Figure 5-1-1 LQFP48 Package Diagram

Remarks:

(1) For the convenience of design applications, the RX/TX of UART0/UART1/UART2 can be mapped to different GPIO pins through settings, as described in the "15-2-9 Pin Reuse Function Mapping Table" for details.

(2) For the convenience of designing applications, the SCL/SDA of IIC can be mapped to any GPIO pin through settings, as described in the "15-2-9 Pin Multiplexing Function Mapping Table" for details. The simulation pins for downloading the CA51F155L2 program are P2.5 (IIC-SDA) and P2.4 (IIC-SCL)

Model：CA51F155L1

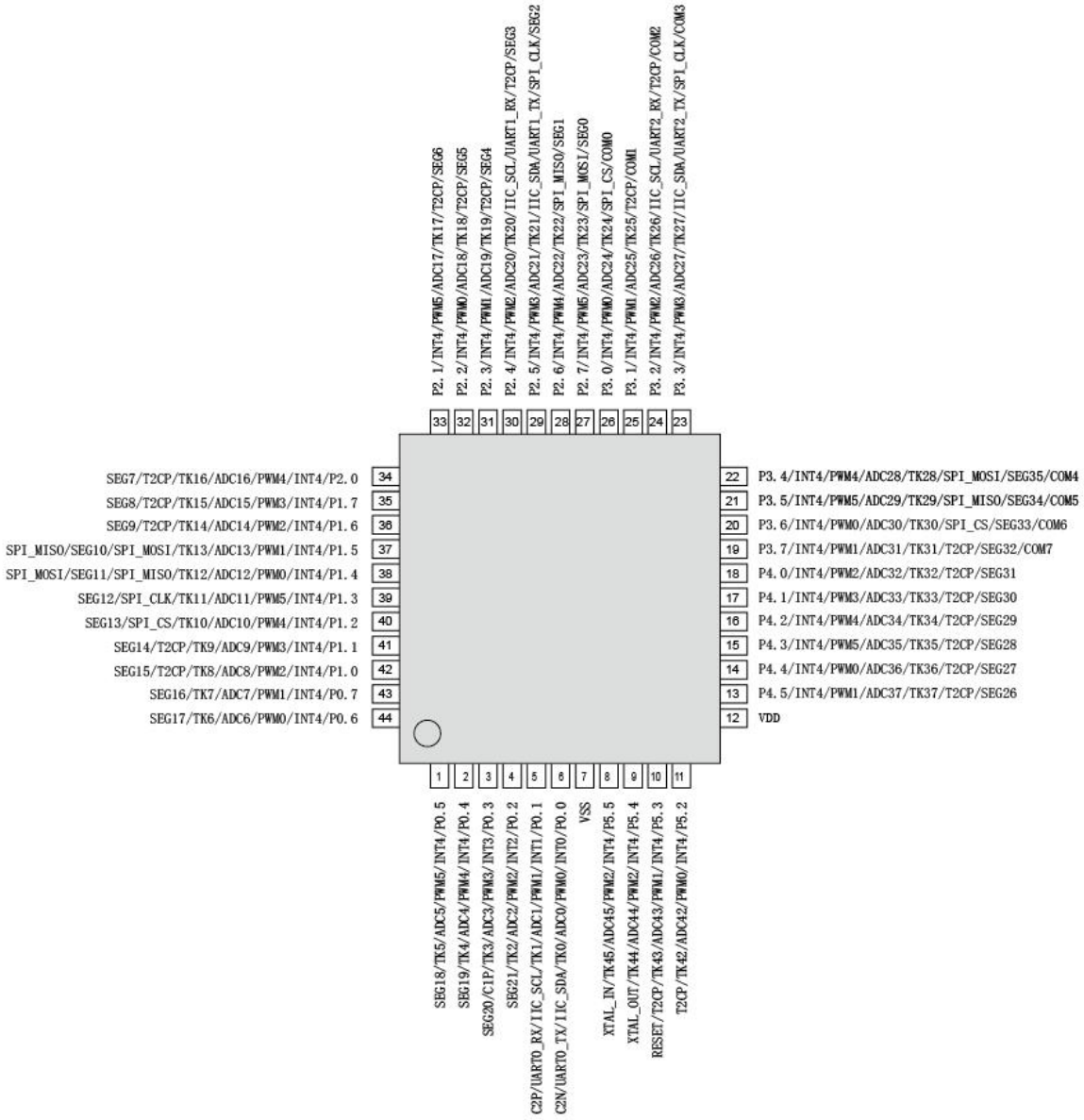


Figure 5-1-2 LQFP44 package diagram

Remarks:

(1) For the convenience of design applications, the RX/TX of UART0/UART1/UART2 can be mapped to different GPIO pins through settings, as described in the "15-2-9 Pin Reuse Function Mapping Table" for details.

(2) For the convenience of designing applications, the SCL/SDA of IIC can be mapped to any GPIO pin through settings, as described in the "15-2-9 Pin Multiplexing Function Mapping Table" for details. The simulation pins for downloading the CA51F155L1 program are P2.5 (IIC-SDA) and P2.4 (IIC-SCL)

Model：CA51F155L0

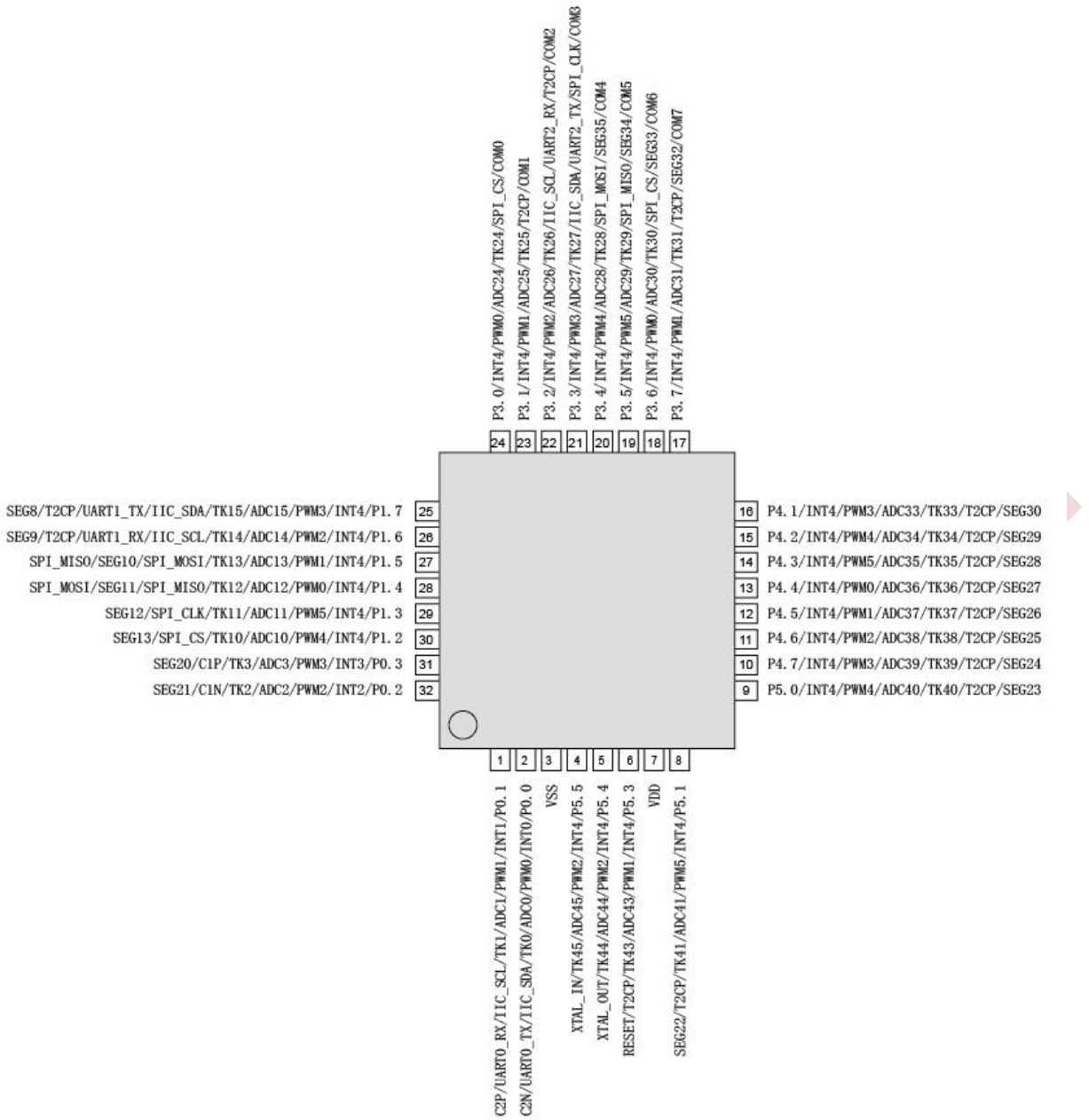


Figure 5-1-3 LQFP32 package diagram

Remarks:

(1) For the convenience of design applications, the RX/TX of UART0/UART1/UART2 can be mapped to different GPIO pins through settings, as described in the "15-2-9 Pin Reuse Function Mapping Table" for details.

(2) For the convenience of designing applications, the SCL/SDA of IIC can be mapped to any GPIO pin through settings, as described in the "15-2-9 Pin Multiplexing Function Mapping Table" for details. The simulation pins for downloading the CA51F155L0 program are P3.3 (IIC-SDA) and P3.2 (IIC-SCL)

Model：CA51F155S6A

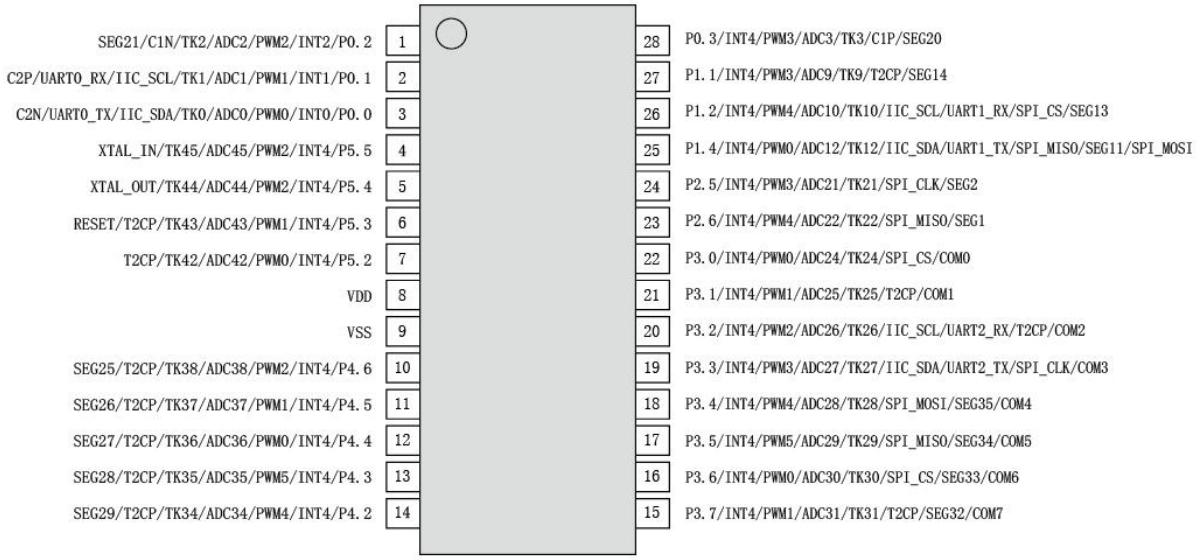


Figure 5-1-4 SOP28 package diagram

Model：CA51F155S6B

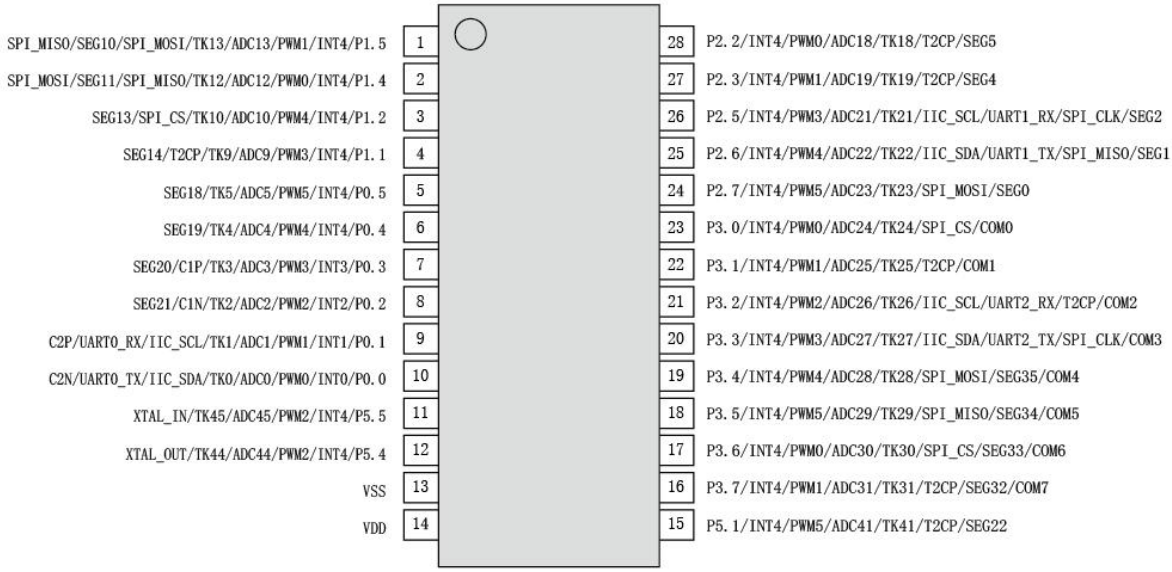


Figure 5-1-5 SOP28 package diagram

Remarks:

(1) For the convenience of design applications, the RX/TX of UART0/UART1/UART2 can be mapped to different GPIO pins through settings, as described in the "15-2-9 Pin Reuse Function Mapping Table" for details.

(2) For the convenience of designing applications, the SCL/SDA of IIC can be mapped to any GPIO pin through settings, as described in the "15-2-9 Pin Multiplexing Function Mapping Table" for details. The simulation pins for downloading the CA51F155S6A program are: P1.4 (IIC SDA), P1.2 (IIC SCL);

The simulation pins for downloading the CA51F155S6B program are P2.6 (IIC SDA) and P2.5 (IIC SCL);

5.2 Pin Description

Table 5-2-1 Pin Description

Pin Serial Number					Pin Name	Pin Function	Default Function
LQFP48	LQFP44	LQFP32	SOP28（A）	SOP28（B）			
1	1	-	-	5	P05/INT4/PWM5/ADC5/TK5/I2C_SDA/ I2C_SCL/UART0_RX/UART0_TX/SEG18	General purpose bi-directional I/O ports INT4 signal input PWM5 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART0 transfer port SEG output port	General purpose bi-directional I/O ports
2	2	-	-	6	P04/INT4/PWM4/ADC4/TK4/I2C_SDA/ I2C_SCL/UART0_RX/UART0_TX/SEG19	General purpose bi-directional I/O ports INT4 signal input PWM4 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART0 transfer port SEG output port	General purpose bi-directional I/O ports
3	3	31	28	7	P03/INT3/PWM3/ADC3/TK3/I2C_SDA/ I2C_SCL/UART0_RX/UART0_TX/C1P/SEG20	General purpose bi-directional I/O ports INT3 signal input PWM3 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART0 transfer port Positive input of comparator SEG output port	General purpose bi-directional I/O ports
4	4	32	1	8	P02/INT2/PWM2/ADC2/TK2/I2C_SDA/ I2C_SCL/UART0_RX/UART0_TX/C1N/SEG21	General purpose bi-directional I/O ports INT2 signal input PWM2 signal output ADC analog channel input Touch key analog channel	General purpose bi-directional I/O ports

						input I²C transfer port UART0 transfer port Negative input of comparator SEG output port	
5	5	1	2	9	P01/INT1/PWM1/ADC1/TK1/I2C_SDA/ I2C_SCL/UART0_RX/UART0_TX/C2P	General purpose bi-directional I/O ports INT1 signal input PWM1 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART0 transfer port Positive input of comparator	I²C transfer port
6	6	2	3	10	P00/INT0/PWM0/ADC0/TK0/I2C_SDA/ I2C_SCL/UART0_RX/UART0_TX/C2N	General purpose bi-directional I/O ports INT0 signal input PWM0 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART0 transfer port Negative input of comparator	I²C transfer port
7	7	3	9	13	VSS	Power ground pin	Power ground pin
8	8	4	4	11	P55/INT4/PWM2/ADC45/TK45/I2C_SDA/ I2C_SCL/UART0_RX/UART0_TX/XTAL_IN	General purpose bi-directional I/O ports INT4 signal input PWM2 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART0 transfer port External low-speed crystal oscillator input port	General purpose bi-directional I/O ports
9	9	5	5	12	P54/INT4/PWM2/ADC44/TK44/I2C_SDA/ I2C_SCL/UART0_RX/UART0_TX/XTAL_OUT	General purpose bi-directional I/O ports	General purpose bi-directional I/O

						INT4 signal input PWM2 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART0 transfer port External low-speed crystal oscillator output port	ports
10	10	6	6	-	P53/INT4/PWM1/ADC43/TK43/I2C_SDA/ I2C_SCL/UART0_RX/UART0_TX/T2CP/RESET	General purpose bi-directional I/O ports INT4 signal input PWM1 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART0 transfer port T2CP signal input Hardware reset pin	Hardware reset pin
11	11	-	7	-	P52/INT4/PWM0/ADC42/TK42/I2C_SDA/ I2C_SCL/UART0_RX/UART0_TX/T2CP	General purpose bi-directional I/O ports INT4 signal input PWM0 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART0 transfer port T2CP signal input	General purpose bi-directional I/O ports
12	12	7	8	14	VDD	Chip power supply pins	Chip power supply pins
13	-	8	-	15	P51/INT4/PWM5/ADC41/TK41/I2C_SDA/ I2C_SCL/UART0_RX/UART0_TX/T2CP/SEG22	General purpose bi-directional I/O ports INT4 signal input PWM5 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART0 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports

14	-	9	-	-	P50/INT4/PWM4/ADC40/TK40/I2C_SDA/ I2C_SCL/UART0_RX/UART0_TX/T2CP/SEG23	General purpose bi-directional I/O ports INT4 signal input PWM4 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART0 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports
15	-	10	-	-	P47/INT4/PWM3/ADC39/TK39/I2C_SDA/ I2C_SCL/UART0_RX/UART0_TX/T2CP/SEG24	General purpose bi-directional I/O ports INT4 signal input PWM3 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART0 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports
16	-	11	10	-	P46/INT4/PWM2/ADC38/TK38/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/T2CP/SEG25	General purpose bi-directional I/O ports INT4 signal input PWM2 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART2 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports
17	13	12	11	-	P45/INT4/PWM1/ADC37/TK37/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/T2CP/SEG26	General purpose bi-directional I/O ports INT4 signal input PWM1 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART2 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports

18	14	13	12	-	P44/INT4/PWM0/ADC36/TK36/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/T2CP/SEG27	General purpose bi-directional I/O ports INT4 signal input PWM0 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART2 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports
19	15	14	13	-	P43/INT4/PWM5/ADC35/TK35/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/T2CP/SEG28	General purpose bi-directional I/O ports INT4 signal input PWM5 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART2 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports
20	16	15	14	-	P42/INT4/PWM4/ADC34/TK34/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/T2CP/SEG29	General purpose bi-directional I/O ports INT4 signal input PWM4 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART2 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports
21	17	16	-	-	P41/INT4/PWM3/ADC33/TK33/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/T2CP/SEG30	General purpose bi-directional I/O ports INT4 signal input PWM3 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART2 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports

22	18	-	-	-	P40/INT4/PWM2/ADC32/TK32/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/T2CP/SEG31	General purpose bi-directional I/O ports INT4 signal input PWM2 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART2 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports
23	19	17	15	16	P37/INT4/PWM1/ADC31/TK31/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/T2CP/SEG32 /COM7	General purpose bi-directional I/O ports INT4 signal input PWM1 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART2 transfer port T2CP signal input SEG output port COM output port	General purpose bi-directional I/O ports
24	20	18	16	17	P36/INT4/PWM0/ADC30/TK30/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/SPI_CS/ SEG33/COM6	General purpose bi-directional I/O ports INT4 signal input PWM2 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART2 transfer port SPI_CS port SEG output port COM output port	General purpose bi-directional I/O ports
25	21	19	17	18	P35/INT4/PWM5/ADC29/TK29/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/SPI_MISO/ SEG34/COM5	General purpose bi-directional I/O ports INT4 signal input PWM5 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART2 transfer port	General purpose bi-directional I/O ports

						SPI_MISO port SEG output port COM output port	
26	22	20	18	19	P34/INT4/PWM4/ADC28/TK28/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/SPI_MOSI/ SEG35/COM4	General purpose bi-directional I/O ports INT4 signal input PWM4 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART2 data receiving port SPI_MOSI port SEG output port COM output port	General purpose bi-directional I/O ports
27	23	21	19	20	P33/INT4/PWM3/ADC27/TK27/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/SPI_CLK/ COM3	General purpose bi-directional I/O ports INT4 signal input PWM3 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART2 transfer port SPI_CLK port SEG output port COM output port	General purpose bi-directional I/O ports
28	24	22	20	21	P32/INT4/PWM2/ADC26/TK26/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/T2CP/COM2	General purpose bi-directional I/O ports INT4 signal input PWM2 signal output ADC analog channel input Touch key analog channel input I^2C transfer port UART2 transfer port T2CP signal input COM output port	General purpose bi-directional I/O ports
29	25	23	21	22	P31/INT4/PWM1/ADC25/TK25/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/T2CP/COM1	General purpose bi-directional I/O ports INT4 signal input PWM1 signal output ADC analog channel input Touch key analog channel	General purpose bi-directional I/O ports

						input I²C transfer port UART2 transfer port T2CP signal input COM output port	
30	26	24	22	23	P30/INT4/PWM0/ADC24/TK24/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/SPI_CS/ COM0	General purpose bi-directional I/O ports INT4 signal input PWM0 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART2 transfer port SPI_CS port COM output port	General purpose bi-directional I/O ports
31	27	-	-	24	P27/INT4/PWM5/ADC23/TK23/I2C_SDA/ I2C_SCL/UART1_RX/UART1_TX/SPI_MOSI/ SEG0	General purpose bi-directional I/O ports INT4 signal input PWM5 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART1 transfer port SPI_MOSI port SEG output port	General purpose bi-directional I/O ports
32	28	-	23	25	P26/INT4/PWM4/ADC22/TK22/I2C_SDA/ I2C_SCL/UART1_RX/UART1_TX/SPI_MISO/ SEG1	General purpose bi-directional I/O ports INT4 signal input PWM4 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART1 transfer port SPI_MISO port SEG output port	General purpose bi-directional I/O ports
33	29	-	24	26	P25/INT4/PWM3/ADC21/TK21/I2C_SDA/ I2C_SCL/UART1_RX/UART1_TX/SPI_CLK/ SEG2	General purpose bi-directional I/O ports INT4 signal input PWM3 signal output ADC analog channel input Touch key analog channel	General purpose bi-directional I/O ports

						input I²C transfer port UART1 transfer port SPI_CLK port SEG output port	
34	30	-	-	-	P24/INT4/PWM2/ADC20/TK20/I2C_SDA/ I2C_SCL/UART1_RX/UART1_TX/T2CP/SEG3	General purpose bi-directional I/O ports INT4 signal input PWM2 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART1 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports
35	31	-	-	27	P23/INT4/PWM1/ADC19/TK19/I2C_SDA/ I2C_SCL/UART1_RX/UART1_TX/T2CP/SEG4	General purpose bi-directional I/O ports INT4 signal input PWM1 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART1 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports
36	32	-	-	28	P22/INT4/PWM0/ADC18/TK18/I2C_SDA/ I2C_SCL/UART1_RX/UART1_TX/T2CP/SEG5	General purpose bi-directional I/O ports INT4 signal input PWM0 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART1 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports
37	33	-	-	-	P21/INT4/PWM5/ADC17/TK17/I2C_SDA/ I2C_SCL/UART1_RX/UART1_TX/T2CP/SEG6	General purpose bi-directional I/O ports INT4 signal input PWM5 signal output ADC analog channel input Touch key analog channel	General purpose bi-directional I/O ports

						input I²C transfer port UART1 transfer port T2CP signal input SEG output port	
38	34	-	-	-	P20/INT4/PWM4/ADC16/TK16/I2C_SDA/ I2C_SCL/UART1_RX/UART1_TX/T2CP/SEG7	General purpose bi-directional I/O ports INT4 signal input PWM4 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART1 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports
39	35	25	-	-	P17/INT4/PWM3/ADC15/TK15/I2C_SDA/ I2C_SCL/UART1_RX/UART1_TX/T2CP/SEG8	General purpose bi-directional I/O ports INT4 signal input PWM3 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART1 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports
40	36	26	-	-	P16/INT4/PWM2/ADC14/TK14/I2C_SDA/ I2C_SCL/UART1_RX/UART1_TX/T2CP/SEG9	General purpose bi-directional I/O ports INT4 signal input PWM2 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART1 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports
41	37	27	-	1	P15/INT4/PWM1/ADC13/TK13/I2C_SDA/ I2C_SCL/UART1_RX/UART1_TX/SPI_MOSI/ SEG10/SPI_MISO	General purpose bi-directional I/O ports INT4 signal input PWM1 signal output ADC analog channel input Touch key analog channel	General purpose bi-directional I/O ports

						input I²C transfer port UART1 transfer port SPI_MOSI/MISO port SEG output port	
42	38	28	25	2	P14/INT4/PWM0/ADC12/TK12/I2C_SDA/ I2C_SCL/UART1_RX/UART1_TX/SPI_MISO/ SEG11/SPI_MOSI	General purpose bi-directional I/O ports INT4 signal input PWM0 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART1 transfer port SPI_MOSI/MISO port SEG output port	General purpose bi-directional I/O ports
43	39	29	-	-	P13/INT4/PWM5/ADC11/TK11/I2C_SDA/ I2C_SCL/UART1_RX/UART1_TX/SPI_CLK/ SEG12	General purpose bi-directional I/O ports INT4 signal input PWM5 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART1 transfer port SPI_CLK port SEG output port	General purpose bi-directional I/O ports
44	40	30	26	3	P12/INT4/PWM4/ADC10/TK10/I2C_SDA/ I2C_SCL/UART1_RX/UART1_TX/SPI_CS/ SEG13	General purpose bi-directional I/O ports INT4 signal input PWM4 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART1 transfer port SPI_CS port SEG output port	General purpose bi-directional I/O ports
45	41	-	27	4	P11/INT4/PWM3/ADC9/TK9/I2C_SDA/ I2C_SCL/UART1_RX/UART1_TX/T2CP/SEG14	General purpose bi-directional I/O ports INT4 signal input PWM3 signal output ADC analog channel input Touch key analog channel	General purpose bi-directional I/O ports

						input I²C transfer port UART1 transfer port T2CP signal input SEG output port	
46	42	-	-	-	P10/INT4/PWM2/ADC8/TK8/I2C_SDA/ I2C_SCL/UART1_RX/UART1_TX/T2CP/SEG15	General purpose bi-directional I/O ports INT4 signal input PWM2 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART1 transfer port T2CP signal input SEG output port	General purpose bi-directional I/O ports
47	43	-	-	-	P07/INT4/PWM1/ADC7/TK7/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/COM7/SEG16	General purpose bi-directional I/O ports INT4 signal input PWM1 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART2 transfer port T2CP signal input COM output port SEG output port	General purpose bi-directional I/O ports
48	44	-	-	-	P06/INT4/PWM0/ADC6/TK6/I2C_SDA/ I2C_SCL/UART2_RX/UART2_TX/COM6/SEG17	General purpose bi-directional I/O ports INT4 signal input PWM0 signal output ADC analog channel input Touch key analog channel input I²C transfer port UART1 transfer port T2CP signal input COM output port SEG output port	General purpose bi-directional I/O ports

Note: The method for setting the signal pin multiplexing function is detailed in Table 15-2-9

6 Central Processing Unit (CPU)

6.1 CPU Introduction

The CA51F155 series chips use a single-cycle 8051 CPU, which is fully compatible with the original MCS-51 instruction set. the CPU uses a pipelined architecture, and typically, the single-cycle 8051 CPU runs 10 times faster than a standard 8051 processor.

The CPU has the following characteristics：

- 1T 8051 CPU
- Compatible with 8051 instruction set, see instruction set appendix
- Dual DPTR for fast data migration

6.2 Register Description

Program counter PC

The program counter PC register is 16 bits, which is a special register used to control the order of instruction execution, and it has no register address. After the microcontroller is powered on or reset, the PC value is 0 and the microcontroller starts executing the program from zero address.

Accumulator ACC

Accumulator ACC is a commonly used special register. The instruction system uses A as the accumulator helper, and it is often used to store the operands of arithmetic or logical operations and the results of the operations.

General purpose register B

The MUL AB instruction multiplies ACC with an 8-bit unsigned number in B. The low byte of the resulting 16-bit product is stored in A and the high byte is stored in B. The DIV AB instruction divides B by A. The integer quotient is stored in A and the remainder is stored in B. Register B can also be used as a general-purpose temporary storage register.

Stack pointer SP

The stack pointer SP is an 8-bit dedicated register. It indicates the location of the top of the stack in the internal RAM block. After system reset, SP initializes bit 07H, making the stack in fact start from cell 08H. Considering that cells 08H~1FH belong to working register group 1~3 respectively, if these areas are used in programming, it is better to change SP to 80H or larger.

Data pointer DPTR

The data pointers DPTR0/DPTR1 are two 16-bit dedicated registers, their high byte registers are represented by DP0H/DP1H and low byte registers are represented by DP0L/DP1L, which can be used optionally via DPS (PSW.1). each DPTR can be handled either as one 16-bit register or as two independent 8-bit registers DP0H/DP1H and DP0L/DP1L.

Status Register PSW

Status register PSW is the status register of the CPU. When the CPU does arithmetic operations or logical operations, the corresponding PSW status bits will change

Table 6-2-1 Accumulator ACC

E0H	7	6	5	4	3	2	1	0
ACC	ACC[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0

Table 6-2-2 General Register B

F0H	7	6	5	4	3	2	1	0
B	B[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0

Table 6-2-3 Stack Pointer SP

81H	7	6	5	4	3	2	1	0
SP	SP[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	1	1	1

Table 6-2-4 Data Pointer DP0L

82H	7	6	5	4	3	2	1	0
DP0L	DP0L[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0

Table 6-2-5 Data Pointer DP0H

83H	7	6	5	4	3	2	1	0
DP0H	DP0H[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0

Table 6-2-6 Data Pointer DP1L

84H	7	6	5	4	3	2	1	0
DP1L	DP1L[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0

Table 6-2-7 Data Pointer DP1H

85H	7	6	5	4	3	2	1	0
DP1H	DP1H[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0

Table 6-2-8 Status Register PSW

D0H	7	6	5	4	3	2	1	0
PSW	CY	AC	F0	RS[1:0]		OV	DPS	P
R/W	R/W	R/W	R/W	R/W		R/W	R	R
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	CY	Bit by bit flag 0：No rounding or borrowing occurs in arithmetic or logical operations 1：Arithmetic or logical operations with rounding or debit occurring
6	AC	Auxiliary feed flag bit 0：No auxiliary rounding or borrowing occurs in arithmetic or logical operations 1：Arithmetic or logical operations in which auxiliary rounding or borrowing occurs
5	F0	F0 flag bit User-defined flag bits
4~3	RS	R0~R7 register page selection bits 00：Page 0 (mapped to 00H-07H) 01：Page 1 (mapped to 08H-0FH) 10：Page 2 (mapped to 10H-17H) 11：Page 3 (mapped to 18H-1FH)
2	OV	Overflow flag bit 0：No overflow occurs 1：There is an overflow occurring
1	DPS	DPTR selection register, 0 to select DPTR0, 1 to select DPTR1
0	P	Parity check bits 0：The accumulator A value of 1 is an even number of bits 1：The number of bits with a totalizer A value of 1 is odd

Table 6-2-9 Register SPMAX

F3H	7	6	5	4	3	2	1	0
SPMAX	SPMAX[7:0]							
R/W	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~0	SPMAX	Register SPMAX is used to record the maximum value of SP, the user can check this register in the application to determine whether the stack is at risk of overflow

7 Memory Systems

7.1 Random data memory (RAM)

The CA51F155 series chips provide 256 bytes of internal RAM and 2K bytes of external RAM with the following memory address assignments：

- The low 128 bytes of internal RAM (address: 00H ~ 7FH) can be addressed directly or indirectly.
- The high 128 bytes of internal RAM (address: 80H ~ FFH) can only be indirectly addressed.
- External 2K bytes of external RAM (addresses: 0000H~07FFH) can be indirectly addressed through MOVX instructions.

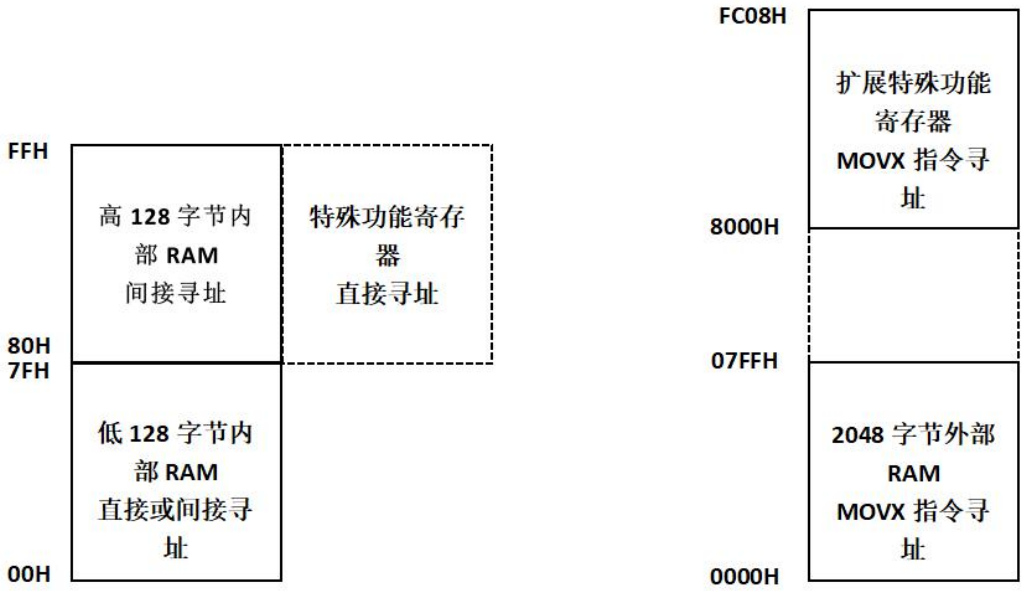


Figure 7-1-1 RAM Organizational Chart

7.2 Special Function Register (SFR)

CA51F155 series chips provide SFR distribution compatible with traditional 8051, SFR and high 128 bytes of internal RAM share the address 80H ~ FFH, can only be directly addressed, SFR mapping as shown in Table 7-2-1.

Table 7-2-1 Special Function Register (SFR) Mapping Table

	Bit-address able	Non-bit addressable						
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
F8H	TKST	TKCFG1	TKCFG2	TKCFG3	TKDL	TKDH	TKPULL	TKCFG4
F0H	B	CBYTE	TKPULLTRIM	SPMAX	TKIE	CMPCON	CMPOUT	-
E8H	LVDCON	LXCON	LXCFG	LXDAT	LXDIVL	LXDIVH	LXCAD	-
E0H	ACC	P4	P5	-	-	-	-	-
D8H	UDCKS0	S0RELL	S0RELH	-	-	-	-	-
D0H	PSW	EP0CON	EP1CON	EP2CON	EPIF	TMCON	TMSNU	I2CCKS
C8H	CKCON	CKDIV	IHCFG	TKCCFG	-	-	-	-
C0H	I2CCON	I2CADR	I2CADM	I2CCCR	I2CDAT	I2CSTA	I2CFLG	-
B8H	IP	S2CON	S2BUF	S2RELL	S2RELH	UDCKS2	-	-
B0H	P3	S1CON	S1BUF	S1RELL	S1RELH	UDCKS1	-	-
A8H	IE	SPCON	SPDAT	SPSTA	-	-	-	-
A0H	P2	WDFLG	WDVTHL	WDVTHH	T2CON	T2CRH	T2CRL	WDCON
98H	S0CON	S0BUF	PWMDUTH	PWMDUTL	PWMAIF	PWMBIF	PWMCIF	INDEX
90H	P1	PWMEN	PWMUPD	PWMCMAX	PWMCON	PWMCFG	PWMDIVL	PWMDIVH
88H	TCON	TMOD	TL0	TL1	TH0	TH1	IDLST	STPST
80H	P0	SP	DP0L	DP0H	DP1L	DP1H	PWCON	PCON

Due to the limited SFR address space, the CA51F155 series chips add extended special function registers to the external RAM address space, and the extended special function register mapping is shown in Figure 7-2-2.

Table 7-2-2 Extended Special Function Register Mapping Table

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
8000H	P00F	P01F	P02F	P03F	P04F	P05F	P06F	P07F
8008H	P10F	P11F	P12F	P13F	P14F	P15F	P16F	P17F
8010H	P20F	P21F	P22F	P23F	P24F	P25F	P26F	P27F
8018H	P30F	P31F	P32F	P33F	P34F	P35F	P36F	P37F
8040H	P40F	P41F	P42F	P43F	P44F	P45F	P46F	P47F
8048H	P50F	P51F	P52F	P53F	P54F	P55F	-	-
8050H	P40C	P41C	P42C	P43C	P44C	P45C	P46C	P47C
8058H	P50C	P51C	P52C	P53C	P54C	P55C	-	-
8060H	ADCON	ADCFGL	ADCDL	ADCDH	ADCALL	ADCALH	ADCKD	-
8120H	P00C	P01C	P02C	P03C	P04C	P05C	P06C	P07C
8128H	P10C	P11C	P12C	P13C	P14C	P15C	P16C	P17C

8130H	P20C	P21C	P22C	P23C	P24C	P25C	P26C	P27C
8138H	P30C	P31C	P32C	P33C	P34C	P35C	P36C	P37C
FC00H	MECON	FSCMD	FSDAT	LOCK	PADRD	PTSL	PTSH	-

7.3 Flash Memory

7.3.1 Function Introduction

Flash memory contains 64K bytes of Flash, which can be repeatedly erased. Flash memory is controlled by a specific set of registers, which users can use to perform operations such as read/write erasure and write protection. Can divide data storage areas arbitrarily, saving EEPROM.

7.3.2 Flash memory organization

- Flash consists of several pages, which are the smallest unit for erasing operations, with each page size of 128 bytes.
- Flash write operations are performed on a page by page basis and must be written to one page at a time (128 bytes). Single byte writing is not supported.
- Flash read operations do not need to be done on a page basis and can continuously read any number of bytes.
- Flash can be divided into program area and data area by function, with a division unit of 512 bytes. The program area is used to store the user's program, while the data area is used to store some data that needs to be saved after power failure.

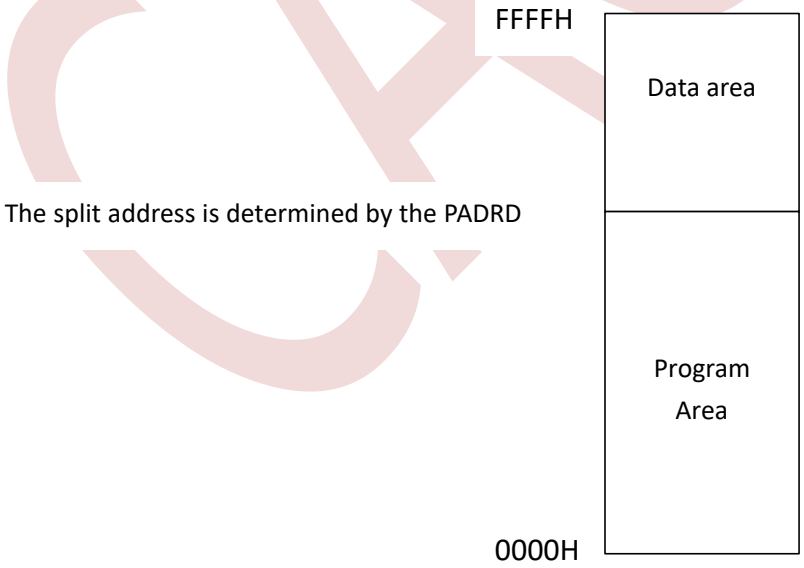


Figure 7-3-1 64KB Flash memory structure

7.3.3 Flash Register Description

Table 7-3-3-1 Register MECON

FC00H	7	6	5	4	3	2	1	0
MECON	-	DPSTB	-	-	-	-	-	BOOT
R/W	-	R/W	-	-	-	-	-	R/W
Initial Value	-	0	-	-	-	-	-	0

Bit Number	Bit Symbol	Description
7	-	-
6	DPSTB	IDLE/STOP mode Flash enter sleep mode control bit 0：IDLE/STOP mode, Flash is in normal operation mode 1：Flash enters sleep mode in IDLE/STOP mode Note: If DPSTB=1, when the chip enters IDLE/STOP mode, the Flash also enters sleep mode at the same time. The power consumption of the Flash in sleep mode is 50nA, and when the chip exits IDLE/STOP mode, the Flash also exits sleep mode at the same time.
5~1	-	-
0	BOOT	Set the program start space selection bit field after soft reset 0：Program runs from FLASH after soft reset 1：Program starts running from XRAM after soft reset

Table 7-3-3-2 Register FSCMD

FC01H	7	6	5	4	3	2	1	0
FSCMD	IFEN	-	-	-	CLRPL	CMD[2:0]		
R/W	R/W	-	-	-	0	R/W		
Initial Value	0	-	-	-	0	0	0	0

Bit Number	Bit Symbol	Description
7	IFEN	The information area access enable bit needs to be set to this position during access
6~4	-	-
3	CLRPL	Clear data from Flash latch
2~0	CMD	Command register 000: No operation 100: Flash sector erase 001: Read Flash data area 010: Write Flash data area 011: Erase one page of Flash data area 101: Read Flash Program Area 110: Writing Flash Program Area 111: Erase a page in the Flash program area

		Remark.： *1. The CMD is automatically cleared after the erase command is executed.* *2.The CMD remains unchanged after the read and write commands are written and then completed by reading and writing to FSDAT.*

Table 7-3-3-3 Register FSDAT

FC02H	7	6	5	4	3	2	1	0
FSDAT	FSDAT[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
Bit Number	Bit Symbol	Description						
7~0	FSDAT	Flash Data Register						

Table 7-3-3-4 Register LOCK

FC03H	7	6	5	4	3	2	1	0
LOCK								
R	-	REPE	-	-	FLKF	PLKF	DLKF	ILKF
W	LOCK[7:0]							
Initial Value	-	0	-	-	0	0	0	0
Bit Number	Bit Symbol	Description						
Write operation								
7~0	LOCK	28H：Unlocking of Flash programmable areas 29H：Unlocking the Flash program area 2AH：Unlocking the Flash data area AAH：Flash is locked, no write erase operation is possible						
Read operation								
7~4	-	-						
3	FLKF	Programmable zone unlock flag, 1 means unlocked						
2	PLKF	Program area unlock flag, 1 means unlocked						
1	DLKF	Data area unlock flag, 1 means unlocked						
0	-	-						

Table 7-3-3-5 Register PADRD

FC04H	7	6	5	4	3	2	1	0
PADRD	PADRD[7:0]							
R/W	R/W							
Initial Value	1	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	-	-
6~0	PADRD	Program area and data area division configuration register The program area and data area are divided in units of 512 bytes, and when PADRD>0 The address space of program area is: 0 ~ (PADRD×512 - 1), The address space of the data area is: (PADRD×512) ~ FFFFH. *Remark：* *1. When PADRD=0, the whole Flash space is data space.* *2. The maximum value of PADRD is 90H respectively, and the setting value of PADRD cannot exceed the maximum value.*

Table 7-3-3-6 Register PTS

FC05H	7	6	5	4	3	2	1	0
PTSL	PTS[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
FC06H	7	6	5	4	3	2	1	0
PTSH	-	-	PTS[13:8]					
R/W	-	-	R/W					
Initial Value	-	-	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
15~14	-	-
13~0	PTS	The target address pointer register, when writing FSDAT operations, the data will be written to the PTS [5:0] related flash latch for temporary storage, and PTS [5:0] corresponds to the lower 6 bits of the actual write operation; When sending a write command, it is necessary to set the relevant page address PTS [13:6]. It is best to reconfigure the PTS address during each read, write, and erase operation. For continuous read operations, only the first address of the continuous read operation can be set.

7.3.4 Flash Control Routines

◆ **Flash divides program area and data area**

For example, the 64K Flash space is divided into the last 512 bytes for data space and the rest for program space, and the program is as follows.

```
---------------------------------------------------------------------------------
PADRD = 127;        //Program area space address is: 0~0xFDFF,data area space address is: 0xFE00~0xFFFF


---------------------------------------------------------------------------------
```

Note: The physical address of the above set data area in FLASH is 0xFE00~0xFFFF, but the logical address is 0x0000~0x01FF, the logical address should be filled in when reading and writing data area.

◆ **Data space page erasure**

For example, to erase data space page n, the program is as follows:

```
---------------------------------------------------------------------------------
unsigned int address;
address = 0x80*n;
FSCMD = 0;                              // Set CMD to 0
LOCK = 0x2A;                            // Data space unlocking
FSCMD = 8;                              //Set erase latch
PTSH = (unsigned char)(address >>8);    //Fill in high-order address
PTSL = (unsigned char)(address);        //Fill in low order address
FSCMD = 3;                              //Set data area erase command
LOCK = 0xAA;                            // FLASH locking
---------------------------------------------------------------------------------
```

Note: Sector serial number n=0, 1, 2 .....

◆ **Writing data to the data space page**

For example, to write data 0xAA to a data space address of (0x80 * n), the program is as follows:

```
---------------------------------------------------------------------------------
unsigned char i;
unsigned int address;
address = 0x80*n;
FSCMD = 0;                              // Set CMD to 0
LOCK = 0x2A;                            // Data space unlocking
PTSH = 0;                               //Set the starting address of the page latch
PTSL = 0;                               //Set the starting address of the page latch
FSCMD = 8;                              //Set erase latch
for(i=0; i<128; i++)
{
    FSDAT = 0xAA;                       //Continuously write data for 1 page
}
PTSH = (unsigned char)(address >>8);    // Set the data first address 8 bits higher
PTSL = (unsigned char)(address);        // Set data first address low 8 bits
FSCMD = 2;                              // Set Write Command
LOCK = 0xAA;                            // FLASH locking
```

Note:

1．Page number n=0, 1, 2.

2．When writing data continuously, only the first address needs to be set. After each FSDAT write, the data pointer register PTS will automatically accumulate.

3．When reading and writing data areas, the set address is the logical address of the data area, not the physical address of FLASH, and the logical address starts from 0.

4．Data writing can only be done on a page by page basis, and 128 bytes must be written each time.

◆ **Data space readout data**

For example, reading Length bytes of data from the data space address n to DataBuf, the program is as follows:

```
unsigned int i,DataBuf[128];
FSCMD = 0;
PTSH = (unsigned char)(n>>8);          //Fill in high-order address
PTSL = (unsigned char)(n);             //Fill in low order address
FSCMD = 1;                             //Execute read operation
for(i = 0; i < Length; i++)
{
    DataBuf [i]= FSDAT;
}
FSCMD = 0;
LOCK = 0xAA;                           //FLASH locking
```

Note:

1．When continuously reading data, only the first address needs to be set. After each read of FSDAT, the data pointer register PTS will automatically accumulate.

2．When reading and writing data areas, the set address is the logical address of the data area, not the physical address of FLASH, and the logical address starts from 0.

3．Data reading does not need to be on a page basis and can read any number of bytes continuously.

◆ **Program space sector erase**

For example, to erase the program space sector n, the program is as follows:

```
unsigned int address;
address = 0x80*n;
FSCMD = 0;                             // Set CMD to 0
LOCK = 0x29;                           //Program space unlocking
FSCMD = 8;                             //Set erase latch
PTSH = (unsigned char)(address>>8);    //Set the high bit address of the sector
PTSL = (unsigned char)(address);       //Set the low bit address of the sector
FSCMD = 7;                             //Set erase command
LOCK = 0xAA;                           //FLASH locking
```

Note: Sector number n=0, 1, 2.

◆ **Writing data into program space**

For example, writing data 0xAA to program space address 0x80 * n, the program is as follows:

```
---------------------------------------------------------------------------------
unsigned char i;
unsigned int address;
address = 0x80*n;
FSCMD = 0;                          //Set CMD to 0
LOCK = 0x29;                        //Program space unlocking
PTSH = 0;                           //Set the starting address of the page latch
PTSL = 0;                           //Set the starting address of the page latch
FSCMD = 8;                          //Set erase latch
for(i=0; i<128; i++)
{
    FSDAT = 0xAA;                   //Continuously write 1 page of data
}
PTSH = (unsigned char)(address >>8); //Set the top 8 bits of the data header address
PTSL = (unsigned char)(address);    //Set the low 8 bits of the data header address
FSCMD = 6;                          //Set write command
LOCK = 0xAA;                        //FLASH locking
---------------------------------------------------------------------------------
```

Note:

1. Page number n=0, 1, 2.

2. When writing data continuously, only the first address needs to be set. After each FSDAT write, the data pointer register PTS will automatically accumulate.

3. Data writing can only be done on a page by page basis, and 128 bytes must be written each time.

◆ **Reading data from program space**

For example, reading Length bytes of data from program space address n to DataBuf, the program is as follows:

```
---------------------------------------------------------------------------------
unsigned char i，DataBuf [128];
FSCMD = 0;                          // Set CMD to 0
PTSH = (unsigned char)(n>>8);       // Set the top 8 bits of the data header address
PTSL = (unsigned char)(n);          // Set the low 8 bits of the data header address
FSCMD = 5;                          // Set read command
for(i=0; i<Length; i++)
{
    DataBuf [i] = FSDAT ;           //Continuously writing data
}
FSCMD = 0;
LOCK = 0xAA;                        // FLASH locking
---------------------------------------------------------------------------------
```

Note:

1. When continuously reading data, only the first address needs to be set. After each read of FSDAT, the data pointer register PTS will automatically accumulate.

2. Data reading does not need to be on a page basis and can read any number of bytes continuously.

7.4 External RAM mapped to program space

2K bytes of external RAM can be mapped to program space usage, with mapping addresses ranging from 0000H to 07FFH. Users can download programs to external RAM space and execute jump instructions directly to the mapped program area when the program is running. Similarly, the value of BOOT (see register MECON for details) can also be set to 1, and then a soft reset can be performed. After the reset, the program starts executing from the external RAM space (with mapped addresses ranging from 0000H to 07FFH). The mapping program area is particularly convenient for implementing IAP and other functions.

8 Interruption system

8.1 Function Introduction

CA51F155 series chip has an enhanced interrupt control system, there are 7 interrupt entry, each interrupt entry has a number of interrupt sources, each interrupt source has two levels of interrupt priority. Each interrupt source has its own interrupt vector, priority setting bit, interrupt enable bit, and interrupt flag, and after responding to the interrupt, the CPU will enter the interrupt service program corresponding to the interrupt and return to the pre-interrupt state after receiving the RETI instruction. If more than one valid interrupt generates interrupt requests at the same time, the CPU will respond in order according to the set interrupt priority; if the priority is the same, it will respond in order according to their natural priority (interrupt entry address from lowest to highest).

8.2 Interrupt logic

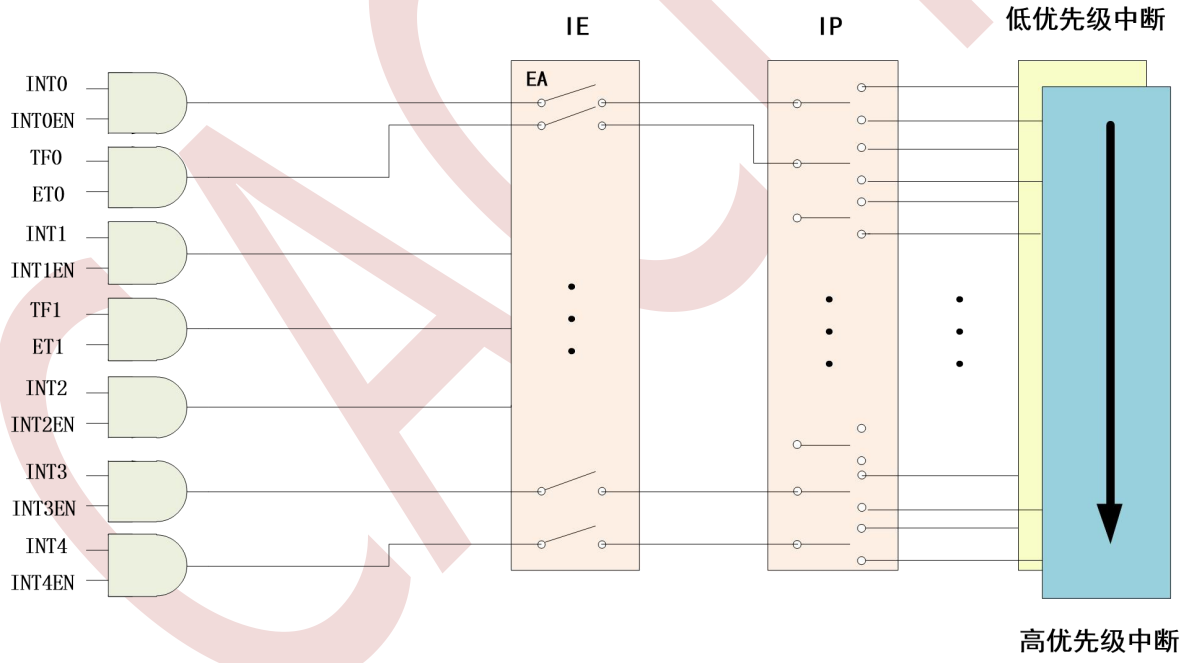


Table 8-2-1 Interrupt Logic Diagram

8.3 Interrupt vector table

Table 8-3-1 Interrupt vector table

Interruptions	Interrupt source	vector	Default Priority
INT0	INT0	03H	0
TF0	Timer 0	0BH	1
INT1	INT1	13H	2
TF1	Timer 1	1BH	3
INT2	External interrupt 2/UART0/ADC interrupt/PWM interrupt/SPI interrupt	23H	4
INT3	External interrupt 3/UART1/Timer 2/Touch interrupt/TMC interrupt	2BH	5
INT4	External interrupt 4/UART2/WDT interrupt/I2C interrupt/LVD interrupt	33H	6

8.4 Interrupt control register

Table 8-4-1 Register IE

A8H	7	6	5	4	3	2	1	0
IE	EA	INT4EN	INT3EN	INT2EN	ET1	EX1	ET0	EX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	EA	Global interrupt enable control bit 0：Shutdown 1：open
6	INT4EN	Interrupt 4 enable control bit (used for external interrupt 4/UART2/WDT interrupt/I2C interrupt/LVD interrupt) 0: Close 1: Open
5	INT3EN	Interrupt 3 enable control bit (used for external interrupt 3/UART1/Timer 2/Touch interrupt/TMC interrupt) 0: Close 1: Open
4	INT2EN	Interrupt 2 enable control bit (used for external interrupt 2/UART0/ADC interrupt/PWM interrupt/SPI interrupt) 0: Close 1: Open

3	ET1	Timer 1 interrupt enable control bit 0: Close 1: Open
2	EX1	Interrupt 1 enable control bit (for external interrupt 1) 0: Close 1: Open
1	ET0	Timer 0 interrupt enable control bit 0: Close 1: Open
0	EX0	Interrupt 0 enable control bit (for external interrupt 0) 0: Close 1: Open

Note: The enable control bit of IE corresponds to the interrupt vector, and the interrupt switches of each interrupt source must also be turned on separately. For example, to enable the interrupt of external interrupt 2, in addition to setting INT2EN to 1, EPIE0 (enable bit of external interrupt 2) should also be set to 1.

Table 8-4-2 Register IP

B8H	7	6	5	4	3	2	1	0
IP	-	PX4	PX3	PX2	PT1	PX1	PT0	PX0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	-	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	-	-
6	PX4	Interrupt INT4 priority control bit 0: Low priority 1: High priority
5	PX3	Interrupt INT3 priority control bit 0: Low priority 1: High priority
4	PX2	Interrupt INT2 priority control bit 0: Low priority 1: High priority
3	PT1	Timer 1 priority control bit 0: Low priority 1: High priority
2	PX1	External interrupt 1 priority control bit 0: Low priority 1: High priority

1	PT0	Timer 0 priority control bit 0: Low priority 1: High priority
0	PX0	External interrupt 0 priority control bit 0: Low priority 1: High priority

8.5 External Interrupt

8.5.1 External Interrupt Introduction

In addition to the standard 8051's INT0 and INT1, the system also extends three interrupt entry points INT2 to INT4 as external interrupts. Each external interrupt can be used to wake up in STOP mode. EPIF is an external interrupt status register from INT2 to INT4. The configuration registers corresponding to INT2~INT4 are EP0CON~EP2CON.

Interrupt input pin selection: INT0 (P0.0), INT1 (P0.1), INT2 (P0.2), INT3 (P0.3), INT4 can select any other I/O pin except for P0.0~P0.3 as the interrupt trigger source input pin. INT0~INT1 can choose to trigger interrupts along the rising or falling edge, while INT2~INT4 can choose to trigger interrupts along the rising, falling, or double edges.

Note:

1. INT0 and INT1 can be triggered by either the rising or falling edge, with the selection bits IT0 and IT1 respectively. Please refer to the description of register TCON for details.

8.5.2 External Interrupt Register

Table 8-5-2-1 Register EPIF

D4H	7	6	5	4	3	2	1	0
EPIF	-	-	-	-	-	EPIF2	EPIF1	EPIF0
R/W	-	-	-	-	-	R/W	R/W	R/W
Initial Value	-	-	-	-	-	0	0	0

Bit Number	Bit Symbol	Description
7~3	-	-
2	EPIF2	External interrupt 4 interrupt flag bit, write 1 to reset to zero
1	EPIF1	External interrupt 3 interrupt flag bit, write 1 to reset to zero
0	EPIF0	External interrupt 2 interrupt flag, write 1 to reset to zero

Table 8-5-2-2 Register EPCON

D1H	7	6	5	4	3	2	1	0
EP0CON	EPIE0	EPPL0		-	-	-	-	-
R/W	R/W	R/W	RW	-	-	-	-	-
Initial Value	0	0	0	-	-	-	-	-

D2H	7	6	5	4	3	2	1	0
EP1CON	EPIE1	EPPL1		-	-	-	-	EPPS2[5]
R/W	R/W	R/W	R/W	-	-	-	-	R/W
Initial Value	0	0	0	-	-	-	-	0

D3H	7	6	5	4	3	2	1	0
EP2CON	EPIE2	EPPL2		EPPS2[4~0]				
R/W	R/W	R/W	R/W	R/W				
Initial Value	0	0	0	0	0	0	0	0

Note: "n" in the table below represents 0/1/2

Bit Number	Bit Symbol	Description
7	EPIEn	External interrupt enable bit 0: Close 1: Open *Note: n=0/1/2 corresponds to external interrupts 2/3/4, respectively.*
6~5	EPPLn	External interrupt trigger edge selection bit 00: Rising edge 01: Descending edge 1x: Double edge *Note: n=0/1/2 corresponds to external interrupts 2/3/4, respectively.* *X=0/1*
EP1CON[0] EP2CON[4~0]	EPPS2[5~0]	External interrupt 4 selection interrupt input port 6'h00~6'h07: P1.0~P1.7 6'h08~6'h0F: P2.0~P2.7 6'h10~6'h17: P3.0~P3.7 6'h18~6'h1F: P4.0~P4.7 6'h20~6'h25: P5.0~P5.5 6'h26~6'h28: P0.4~P0.6 Other: P0.7 *Note: EPPS2 [5] is placed in EP1CON [0]*

8.5.3 External Interrupt Control Routines

◆ **External interrupt 0 control routine**

For example, to enable external interrupt 0, the procedure is as follows:

```
---------------------------------------------------------------------------------
void INT0_init(void)
{
    P00F = 1;       //The interrupt pin for external interrupt 0 is P0.0, set P0.0 as the input function
    EX0 = 1;        //INT0 interrupt enable
    IE0 = 1;        //External interrupt 0 enable
    IT0 = 1;        //Set to falling edge interrupt
    EA = 1;         //Total interrupt enable
}

void INT0_ISR (void) interrupt 0
{
    //External interrupt 0 interrupt service program
}
---------------------------------------------------------------------------------
```

◆ **External interrupt 4 control routine**

Taking external interrupt 4 as an example, set P3.3 as the input pin for external interrupt 4 and enable external interrupt 4. The program is as follows:

```
---------------------------------------------------------------------------------
#define EPIE(n)             (n<<7)
#define EPPL(n)             (n<<5)
#define EPPSEL_L(n)         ((n&0x1F)<<0)
#define EPPSEL_H(n)         (n>>5)
#define P33_INDEX           19

void INT4_init(void)
{
    P33F = 1;                                   //Set P3.3 as input pin
    /* Enable external interrupt and select falling edge trigger, set P33 as INT4 interrupt pin */
    EP1CON |= EPPSEL_H(P33_INDEX);              // EPPS2 [5] placed on EP1CON [0]
    EP2CON = EPIE(1) | EPPL(1) | EPPSEL_L(P33_INDEX);
    INT4EN = 1;                                 // INT4 interrupt enable
    EA = 1;                                     // Total interrupt enable
}
void INT4_ISR (void) interrupt 6
{
    if(EPIF & 0x04)                             // Determine external interrupt 4 interrupt flag
    {
```

```
        EPIF = 0x04;                        // Interrupt flag write 1 clear 0
        // External Interrupt 4 Interrupt Service Program
        ......
    }
}
```

---

9 Clock System

9.1 Introduction of clock system

The CA51F155 family of chips supports the following clock sources in total：

- Built-in 12MHz RC oscillator
- Built-in 128KHz RC oscillator
- Built-in 24MHz RC oscillator
- Support external 32.768KHz crystal oscillator

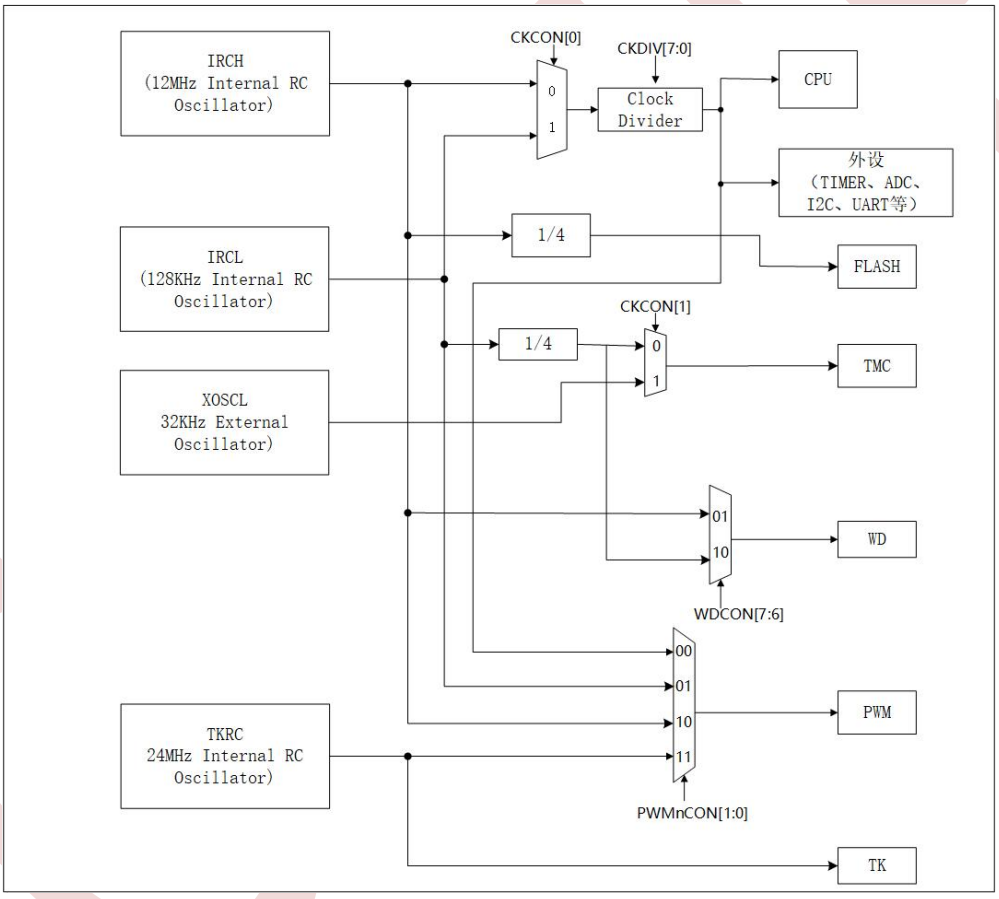


Figure 9-1-1 Clock source diagram

Users can control the clock sources independently. They can disable or enable any of the clock sources in order to manage the power consumption flexibly.

All the clock sources can be set as system alarm clock and assigned to various peripherals as their clock sources. For more information you may refer to the Peripherals part.

9.1.1 Clock-specific Name Definition

Symbol	Description
IRCH	Built-in 12MHz RC oscillator
IRCL	Built-in 128KHz RC oscillator
TKRC	Built-in 24MHz RC oscillator
XOSCL	External 32.768MHz crystal oscillator

9.1.2 12 MHz Internal RC Oscillator(IRCH)

IRCH is the default system clock after the chip is powered on, and can be turned on or off by the IHCKE bit of register CKCON.The chip is shipped from IRCH frequency correction for 12MHz@5V/25° C with a clock accuracy of ±2%.

9.1.2 24 MHz Internal RC Oscillator(TKRC)

TKRC can be turned on or off through the TKCKE bit of register CKCON, serving as a dedicated clock for touch modules.

9.1.3 Built-in 128 KHz RC Oscillator (IRCL)

IRCL can be turned on or off by the ILCKE bit in register CKCON. IRCL is set to the system clock to achieve low system power consumption.

9.1.4 External 32.768KHz Crystal Resonator (XOSCL)

XOSCL is mainly used as a clock source for TMC, used for real-time timing, to achieve the clock function of the product. XOSCL is opened or closed through the XLCKE bit of register CKCON. It should be noted that XOSCL has a relatively long oscillation time, which takes about 1 second to reach stability. When applying, it is necessary to wait for the XOSCL clock to stabilize before it can be used.

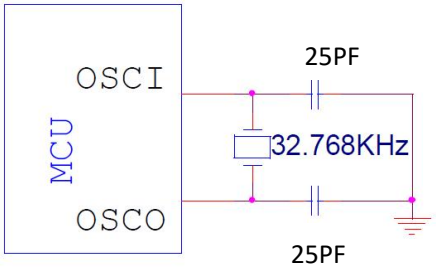


Figure 9-1-4-1 Typical circuit diagram of XOSCL

Important Reminder:

1. *During hardware design, the load capacitor of the crystal oscillator must be connected to the chip ground, and the compensation capacitor of the crystal oscillator should be as close as possible to the VSS pin of the chip.*

32.768KHz quartz crystal oscillator requires the use of crystal oscillator specifications with a diameter of 3mm x 8mm.

2. *The above circuit and component parameters are for reference only. The parameters may need to be modified when using crystal oscillators from different manufacturers in the circuit.*

9.2 Clock Control Register Description

Table 9-2-1 Register IHCFG

CAH	7	6	5	4	3	2	1	0
IHCFG	IHCFG[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
Bit Number	Bit Symbol	Description						
7~0	IHCFG	IRCH frequency adjustment register						

Table 9-2-2 Register TKCCFG

CBH	7	6	5	4	3	2	1	0
TKCCFG	TKCCFG [7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
Bit Number	Bit Symbol	Description						
7~0	TKCCFG	TKRC frequency adjustment register						

9.3 System Clock

The system clock control is completed by registers CKCON and CKDIV. Through these register groups, it is possible to separately set the switches of each clock source, switch the system clock, and perform frequency division operations.

There are two clock options for the system clock: IRCH and IRCL. After power on, the default system clock is IRCH, and the CKDIV value is 1, which means that the system clock defaults to the binary frequency of IRCH when powered on. If the CPU needs to run at a higher frequency, the software can set the CKDIV to 0.

9.3.1 System clock structure diagram

The system clock structure diagram is shown in Figure 9-3-1.

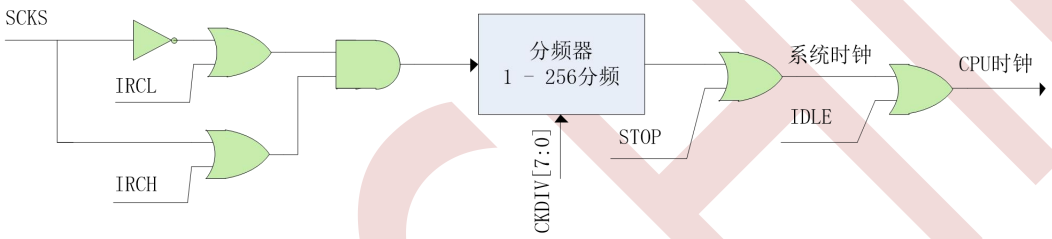


Figure 9-3-1 System clock structure diagram

9.3.2 System Clock Control Register Description

Table 9-3-2-1 Register CKCON

C8H	7	6	5	4	3	2	1	0
CKCON	IHCKE	ILCKE	TKCKE	XLCKE	-	-	TMCS	SCKS
R/W	R/W	R/W	R/W	R/W	-	-	R/W	R/W
Initial Value	0	0	0	0	-	-	0	0

Bit Number	Bit Symbol	Description
7	IHCKE	IRCH enable control bit 0：Shutdown 1：Open Note: When this bit is 1, the clock module is turned on, but when this bit is 0, if the system or other modules choose the clock source, the clock will still be turned on.
6	ILCKE	IRCL enable control bit 0：Shutdown 1：Open Note:

		When this bit is 1, the clock module is turned on, but when this bit is 0, if the system or other modules choose the clock source, the clock will still be turned on.
5	TKCKE	TK clock enable control bit 0：Shutdown 1：Open
4	XLCKE	XOSCL clock enable control bit 0：XOSCL clock off 1：XOSCL clock on
3~2	-	-
1	TMCS	TMC counting clock selection 0：Select IRCL 1：Select XOSCL
0	SCKS	System clock selection bit 0：Select IRCH 1：Select IRCL

Table 9-3-2-2 Register CKDIV

C9H	7	6	5	4	3	2	1	0
CKDIV	CKDIV[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	1
Bit Number	Bit Symbol	Description						
7~0	CKDIV	System clock frequency division： 00H：No division 01H：frequency divided by 2 02H：frequency divided by 3 03H：frequency divided by 4 …… FFH：frequency divided by 256						

Note: After powering on, the system clock defaults to 2 divisions. If you need to modify it to a 12MHz clock, you need to set CKDIV to 8'h00;

9.3.3 System clock control methods and routines

◆ **Set the system clock to IRCH**

To set IRCH as the system clock. The program is as follows:

```
---------------------------------------------------------------------------------------
#define IHCKE               (1<<7)
#define CKSEL_IRCH          0
void Sys_Clk_Set_IRCH(void)
{
    CKCON |= IHCKE;                         // enable IRCH
    CKCON = (CKCON&0xFE) | CKSEL_IRCH;      // set IRCH as system clock
}
---------------------------------------------------------------------------------------
```

◆ **Set IRCL as the system clock**

To set IRCL as the system clock. The program is as follows:

```
---------------------------------------------------------------------------------------
#define ILCKE               (1<<6)
#define CKSEL_IRCL          1
void Sys_Clk_Set_IRCL(void)
{
    CKCON |= ILCKE;                         // Turn on the IRCL clock
    Delay_ms(1);                            // Delay 1ms after enabling IRCL and wait for IRCL to stabilize
    CKCON = (CKCON&0xFE) | CKSEL_IRCL;      // Set the system clock to IRCL
}
---------------------------------------------------------------------------------------
```

10 Power supply and reset system

10.1 Power supply system

Connect a 2.2V-5.5V power supply between the VDD and VSS pins of the CA51F155 series chip, which can directly supply power to the internal digital and analog systems of the chip. It should be noted that under different power supply voltage conditions, the maximum frequency and power consumption supported by the chip for operation are not the same. Please refer to the Electrical Characteristics section for details.

Figure 10-1-1 shows a typical circuit diagram of the chip power supply.

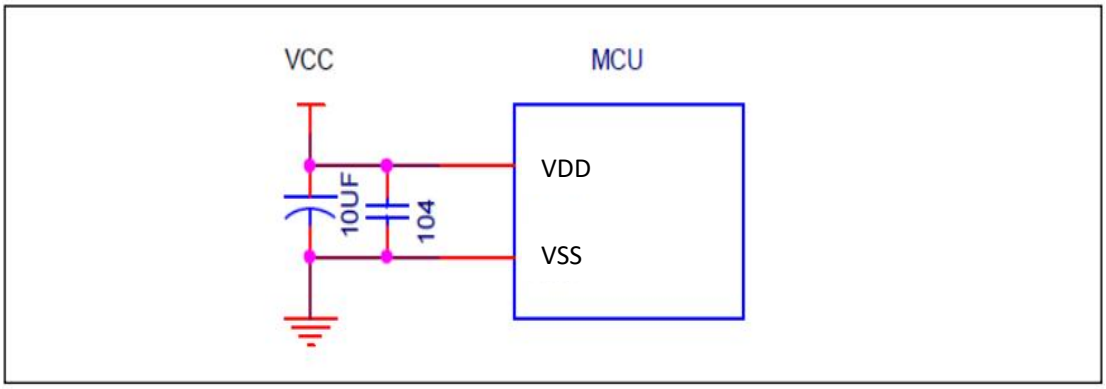


Figure 10-1-1 Typical circuit diagram of chip power supply

Important Reminder:

1. *In the above circuits, the filtering capacitors 10uF and 104 are standard configurations for chip power supply circuits and cannot be omitted. This capacitor must be close to the chip power supply Place your feet, otherwise it may cause abnormal chip operation.*
2. *The above circuit and component parameters are for reference only, and may need to be modified according to the peripheral working environment and different voltage power supply parameters*

10.1.2 Internal reference voltage control register

Table 10-1-2-1 Register PWCON

86H	7	6	5	4	3	2	1	0
PWCON	FLEVEL[3:0]				VREFS	-	-	-
R/W	R/W				R/W	-	-	-
Initial Value	1	0	0	0	0	-	-	-

Bit Number	Bit Symbol	Description
7~4	FLEVEL	Internal reference voltage (Bandgap) output adjustment bit field 0000：0.825V 0001：0.850V 0010：0.875V 0011：0.900V 0100：0.925V 0101：0.950V 0110：0.975V 0111：1.000V 1000：1.025V 1001：1.050V 1010：1.075V 1011：1.100V 1100：1.125V 1101：1.150V 1110：1.175V 1111：1.200V *Note: This reference voltage has been calibrated at the factory with an accuracy of ± 50mV. The calibration value is automatically loaded when powered on and cannot be changed by the user.*
3	VREFS	Drive selection for reference voltage: 0:0.8uA driving capability, default 1: Operational amplifier drive
2~0	-	-

10.2 Reset system

The CA51F155 series chips have multiple internal and external reset sources, as shown in Figure 10-2-1.

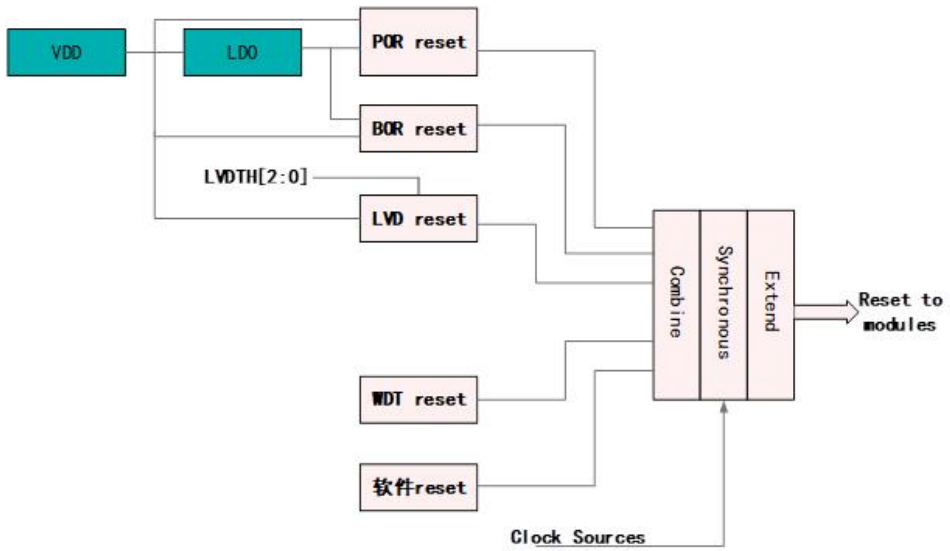
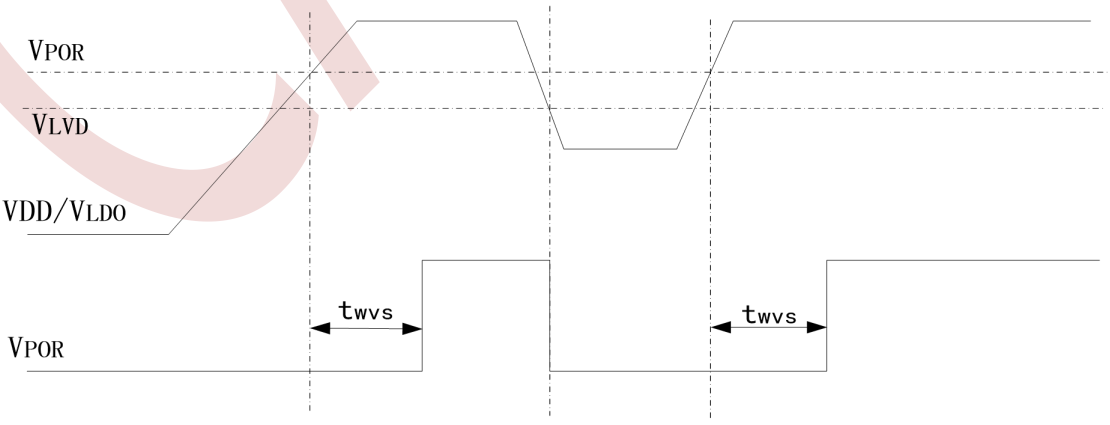


图 10-2-1 Reset system architecture diagram

- **Power-On Reset (POR)**

The system shows a gradually increasing curve when powered on, and it takes some time to reach the normal working voltage. Power on reset is based on the power supply voltage VDD. When the voltage is below the detection threshold, the power on reset signal is effective.

The power-on reset circuit ensures that the chip is in a reset state during the power-up process and that the chip can start operating from a known stable state after power-up. The power-on reset signal is also spread by the chip's internal counter to ensure that the various internal analog modules can enter a stable operating state after power-on.



twvs：等待电压稳定时间

Figure 10-2-2 Power-on reset circuit example and power-on process

- **Power-Off Reset (BOR)**

By using power-off reset, a warning signal for power drop (such as interference or load changes) can be provided to the chip. Once the power supply voltage VDD drops to a certain threshold, the chip should be reset in a timely manner to avoid abnormal system operation or program execution errors.

- **Low voltage reset**

Low voltage detection (LVD) allows continuous monitoring of the supply voltage VDD in various operating modes. a reset signal can be generated when VDD falls below the domain voltage set by LVD for more than 20us (provided that LVD is set to reset mode).

- **Watchdog Reset**

The watchdog timer is responsible for monitoring the execution of instructions by the processor and, with the proper configuration, can generate a reset signal if the watchdog timer is not refreshed within a specific time period. After a power-on reset, the watchdog timer is off and then configured to be on when the user needs it.

- **Soft Reset**

The chip can perform a soft reset under program control. By writing 1 to the SWRST bit in the PCON register, the CPU can issue a reset command.

Power-on and power-down reset will reset all circuits, LVD and WDT reset cannot reset their own circuits, but can reset other circuits (e.g. after WDT reset is generated, WDT module circuits are not reset, WDT registers remain in the state before reset, but circuits outside WDT have been reset). neither LVD/WDT nor soft reset can reset memory control circuits Neither LVD/WDT nor soft reset can reset the memory control circuit. After a soft reset, the program will start running from the location pointed by the BOOT configuration. After all resets are generated, the PC will point to address 0.

11 Power Management

The CA51F155 series chips have three different low-power modes: IDLE mode, STOP mode, and low-speed operation mode. system power consumption is less than 55uA in IDLE mode, less than 7uA in STOP mode, and less than 90uA in low-speed operation.

11.1 IDLE mode

In IDLE mode, the CPU will stop working. Before entering IDLE mode, all other clock sources except the master clock can be selected to be turned off as needed to save power. Likewise, before entering IDLE mode, certain peripherals of the chip can be set to be switched on and off as needed. The open peripherals can still work normally in IDLE state.

Before setting into IDLE mode, you need to check the registers IDLST (IDLSTH and IDLSTL), if all the bits are 0, the CPU will enter IDLE mode normally after setting into IDLE mode. If the bits of IDLST are not all 0, even if there is an operation to set into IDLE mode, the CPU will not enter IDLE mode, but continue to stay in normal operation mode. In this case, the user needs to finish the interrupt processing of the corresponding bit of IDLST before resetting the action to enter IDLE mode.

All reset events and any interrupt events will wake up the chip. After the interrupt wakes up the CPU, the chip will first restore the clock, then respond to the interrupt and enter the service program of the interrupt. After exiting the interrupt service program, the chip will execute the instruction following the reset IDLE instruction. When exiting the IDLE mode, the IDLE bit will be automatically cleared to zero.

Note that two nop instructions need to follow immediately after the reset IDLE instruction to prevent program errors.

11.2 STOP mode

STOP mode is a deeper low-power mode than IDLE. STOP mode stops all clocks (including the master clock) and clock generation circuits. If the WDT and TMC are on, the clock modules they use will be in operation and the WDT and TMC can be selectively turned off to save power.

Similar to IDLE mode, before entering STOP mode, you need to check the STPST (STPSTH and STPSTL) registers, if there are bits set to 1, you need to handle them first to ensure that you can enter STOP mode smoothly.

STOP mode can be woken up by external interrupt, LVD interrupt or reset, TMC interrupt, WDT interrupt or reset, clock monitor interrupt and touch interrupt. If it is wake-up by interrupt, then after waking up the MCU, the chip will first restore the clock, then respond to the interrupt and enter the service program of the interrupt. After exiting the interrupt service program, the chip will execute the instruction after the set STOP instruction. When exiting STOP mode, the STOP bit will be automatically cleared to zero.

For better wake-up of the chip, it is recommended to switch the system clock to the internal clock before entering STOP mode, because the external clock needs more time to wait for stability when waking up.

When entering STOP mode, the last clock edge will turn off the system clock, and then the chip enters

STOP mode completely. It should be noted that the instruction to set STOP needs to be followed immediately by three nop instructions to prevent program errors.

11.3 Low-speed operation mode

Since the power consumption of the chip is directly related to the operating speed, switching the master clock to run at a low clock speed can also significantly reduce power consumption. The current when the system is set to IRCL (frequency of 128KHz) is less than 90uA.

11.4 Low Power Related Register Description

Table 11-4-1 Register PCON

87H	7	6	5	4	3	2	1	0
PCON	-	-	SWRST	-	-	TSMODE	STOP	IDLE
R/W	-	-	W	-	-	R	W	W
Initial Value	-	-	0	-	-	0	0	0

Bit Number	Bit Symbol	Description
7	-	-
6	-	-
5	SWRST	Soft reset control bit, 1 valid Set SWRST=1 to generate a soft reset, and clear 0 automatically after the reset is generated.
4~3	-	-
2	TSMODE	Online emulation mode flag bit, 1 means the chip is working in online emulation mode
1	STOP	STOP mode control bit, 1 valid When STOP=1 and STPST is 0, the chip enters STOP mode and automatically clears 0 after exiting STOP mode
0	IDLE	IDLE mode control bit, 1 valid When setting IDLE=1 and IDLST is 0, the chip enters IDLE mode and automatically clears 0 after exiting IDLE mode

Table 11-4-2 Registers IDLST

8EH	7	6	5	4	3	2	1	0
IDLST	-	IDLSTL[6:0]						
R/W	-	R						
Initial Value	-	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description

7	-	-
6	I2CINT/WDIF/LVDINT/UART2/EPIF[2]	When in IDLE mode, the interrupt status of external interrupt 4/UART2/WDT/I2C/WDT/LVD
5	TKINT/TMINT/TIMER2/EPIF[1]	When in IDLE mode, external interrupt 3/UART1/timer 2/touch interrupt/TMC interrupt status
4	UART1/ADC/PWM/SPI/EPIF[0]	When in IDLE mode, the interrupt status of external interrupt 2/UART0/ADC interrupt/PWM interrupt/SPI interrupt
3	TF1	When in IDLE mode, the interrupt state of timer 1
2	PIF[1]	When in IDLE mode, the interrupt status of external interrupt 1
1	TF0	When in IDLE mode, the interrupt state of timer 0
0	PIF[0]	When in IDLE mode, the interrupt state of external interrupt 0

Table 11-4-3 Registers STPST

8FH	7	6	5	4	3	2	1	0
STPST	-	STPSTL [6:0]						
R/W	-	R						
Initial Value	-	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	-	-
6	WDTWKF/LVDWKF/I2CWKF	When in STOP mode, the interrupt status of WDT/LVD/I2C
5	TKWKF/TMWKF	When in STOP mode, touch the interrupt status of the button/TMC
4	EPWKF[2]	When in STOP mode, the interrupt status of external interrupt 4
3	EPWKF[1]	When in STOP mode, the interrupt status of external interrupt 3
2	EPWKF[0]	When in STOP mode, the interrupt status of external interrupt 2
1	PWKF[1]	When in STOP mode, the interrupt status of external interrupt 1
0	PWKF[0]	When in STOP mode, the interrupt state of external interrupt 0

11.5 Low power mode control routines

◆ **STOP Mode Routine**

The STOP mode procedure is as follows.

```
---------------------------------------------------------------------------------------
#define IHCKE           (1<<7)
#define ILCKE           (1<<6)
#define CKSEL_IRCH      0
#define CKSEL_IRCL      1

void Stop(void)
{
    bit IE_EA;
    unsigned char ck_bak;
    I2CCON = 0;             // Turn off the I2C function, because I2C is enabled by default, if I2C is not turned off
                            // will not be able to turn off the IRCH clock
    MECON |= (1<<6);        // Set FLASH into deep sleep state
    ck_bak = CKCON & 0xFE;              // Backup clock status
    CKCON = 0;                          //Turn off all clocks
    IE_EA = EA;                         //Save global interrupt enable bit status
    EA = 0;
    PCON = (PCON&0x04)|0x02;            //Enter STOP mode
    _nop_();                            //Three nop instructions need to be followed immediately after the
                            //STOP instruction to prevent program errors.
    _nop_();
    _nop_();
    EA = IE_EA;                         //Restore the original global interrupt switch state
    Sys_Clk_Set_IRCH();
    CKCON |= ck_bak;                    //Restore the closed clock
}
```

Test conditions:

All clocks are turned off, all output pins are unloaded, all digital input pins are not floating, all peripherals are turned off, Flash enters deep sleep mode, and CPU enters STOP mode.

```
---------------------------------------------------------------------------------------
```

◆ **IDLE Mode Routine**

The IDLE mode procedure is as follows.

```
---------------------------------------------------------------------------------------
#define IHCKE           (1<<7)
#define ILCKE           (1<<6)
#define CKSEL_IRCH      0
#define CKSEL_IRCL      1
```

```
void Idle(void)
{
    unsigned char ck_bak;
    I2CCON = 0;          // Disable I2C module, because I2C is enabled by default, if I2C is not disabled, IRCH
                         //      clock will not be disabled
    ck_bak = CKCON & 0xFE;                  // Backup clock status
    CKCON = (CKCON&0x41) | ILCKE;           // Enable IRCL clock and turn off other clocks
    Delay_ms(1);                            // Enable IRCL and delay for 1ms, wait for IRCL to stabilize
    CKCON = (CKCON&0xFE) | CKSEL_IRCL; // System clock switched to IRCL
    MECON |= (1<<6);                        // Set FLASH to enter deep sleep mode
    while(IDLST&0x7F);                      // If there is an interrupt that is not responding, wait for the interrupt to be
                                            // responded to
    PCON = (PCON&0x04)|0x01;                // Enter IDLE mode
    _nop_();
    _nop_();
    Sys_Clk_Set_IRCH();
    CKCON |= ck_bak;                        // Restore the closed clock
}
```

Note:

Since the master clock is still open after entering IDLE, if the master clock is a high-speed clock before entering IDLE, the power consumption will still be very large after entering IDLE mode, so you need to switch the master clock to a low-speed clock before entering IDLE.

---

12 General purpose timer (timer 0, timer 1, timer 2)

12.1 Timer 0

12.1.1 Timer 0 Introduction

The timer or counter function is selected by the CT0 bit (TMOD[2]), with CT0=0 selected as a timer and CT0=1 selected as a counter. When used as a timer, the clock is 12 divisions of the system clock. When used as a counter, the clock is the input clock of T0. Since it takes 2 clock cycles to detect a change in the input edge of T0, the maximum input baud rate when used as a counter is 1/2 the internal system clock frequency. the T0 input signal is not limited in duty cycle, however, in order to fully recognize a 0 or 1 state, the signal needs to be held for at least 1 internal system clock cycle time. Timer 0 has 4 operating modes, which are selected by the T0M0, T0M1 bits (TMOD[1:0]).

- **Mode 0**

In this mode, timer 0 acts as a 13-bit timer/counter. TH0 holds the high 8 bits of the 13-bit timer/counter, TL0[4:0] holds the low 5 bits, and TL0[7:5] is invalid and should be ignored when read. When timer 0 overflows, interrupt flag bit TF0 (TCON[5]) will be set to 1. After the interrupt is responded, TF0 bit will be cleared to 0 automatically. When GATE0 (TCON[3]) = 0, the timer/counter is enabled to count by TR0 (TCON[4]) bit, when GATE0 = 1, the timer/counter is enabled by pin INT0 control, when INT0 is high count, and when INT0 is low, it stops counting.

- **Mode 1**

In this mode, Timer 0 functions as a 16-bit timer/counter and is otherwise identical to Mode 0.

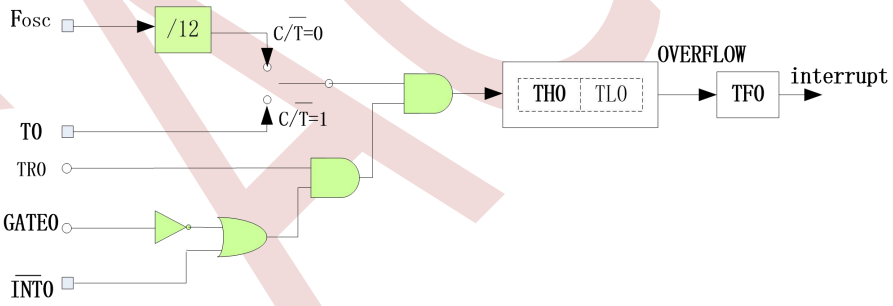


Figure 12-1-1-1 Mode 0 and 1 of Timer 0

- **Mode 2**

In this mode, timer 0 acts as an 8-bit auto-reload timer/counter, and only TL0 is auto-accumulated. When TL0 count overflows, not only the interrupt flag TF0 is generated, but also the initial value of count is automatically loaded from TH0 to TL0. Other setting methods are the same as modes 0 and 1.

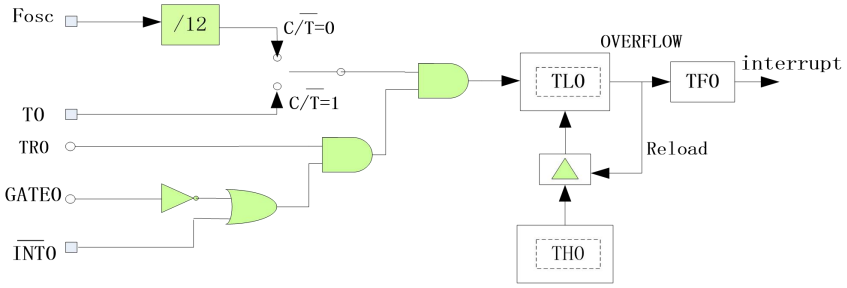


Figure 12-1-1-2 Mode 2 of Timer 0

- **Mode 3**

In this mode, TL0 and TH0 act as two independent 8-bit timers/counters. TL0 can act as timer or counter, while TH0 can only act as timer. Where TL0 occupies the control bits CT0, GATE0, TR0, TF0, INT0 of timer 0, while TH0 can only occupy the control bits TR1, TF1 of timer 1. Other control methods are the same as modes 0 and 1. When timer 0 works in mode 3, timer 1 and TH0 share control bit TR1, but timer 1 can only work in situations where interrupt generation is not required because TF1 is already occupied by TH0, for example, as a UART's baud rate generator.

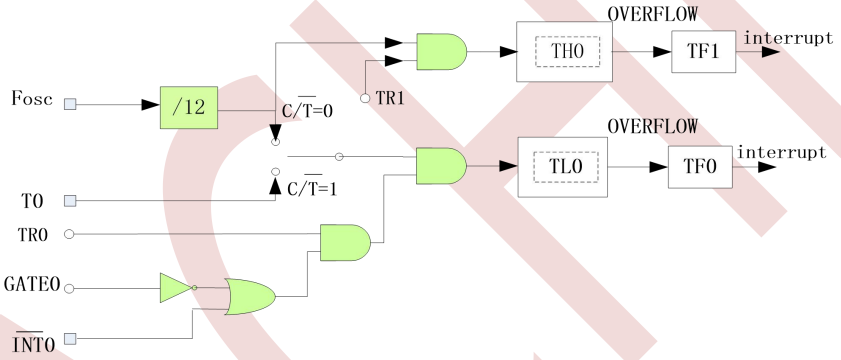


Figure 12-1-1-3 Mode 3 of Timer 0

12.1.2 Timer 0 Register Descriptions

Table 12-1-2-1 Register TCON

88H	7	6	5	4	3	2	1	0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	TF1	TH0 overflow/timer 1 overflow flag bit of timer 0 mode 3, which is automatically cleared to 0 when the interrupt is responded.
6	TR1	Timer 1 operation control bit, 1 valid
5	TF0	Timer 0 overflow flag bit, automatically clear 0 when interrupt is responded.
4	TR0	Timer 0 run control bit, 1 valid
3	IE1	External interrupt 1 enable bit, 1 active
2	IT1	External interrupt 1 trigger type control bit 0: External interrupt 1 is triggered on the rising edge of the input pin

		1: External interrupt 1 is triggered on the falling edge of the input pin
1	IE0	External interrupt 0 enable bit, 1 active
0	IT0	External interrupt 0 trigger type control bit 0: External interrupt 0 is triggered on the rising edge of the input pin 1: External interrupt 0 is triggered on the falling edge of the input pin

Table 12-1-2-2 Register TMOD

89H	7	6	5	4	3	2	1	0
TMOD	GATE1	CT1	T1M1	T1M0	GATE0	CT0	T0M1	T0M0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	GATE1	Timer 1 gated control bit, 1 is valid. Timer 1 is switched by INT1 control when valid
6	CT1	Timer 1 counter/timer selection bit 0: timer, clocked at 12 divisions of the system clock 1: Counter, clocked as T1 input clock
5	T1M1	[T1M1,T1M0] is timer 1 mode selection bit 00: Mode 0, TL1 and TH1 form a 13-bit timer/counter 01: Mode 1, TL1 and TH1 form a 16-bit timer/counter 10: Mode 2, TL1 as 8-bit timer/counter, TH1 as auto reload register 11: Mode 3, this mode will lock TH1/TL1, equivalent to TR1=0
4	T1M0	
3	GATE0	Timer 0 gated control bit, 1 is valid. Timer 0 is switched by INT0 control when valid
2	CT0	Timer 0 counter / timer selection bit 0: Timer, clocked at 12 divisions of the system clock 1: Counter, clocked as T0 input clock
1	T0M1	[T0M1,T0M0] is timer 0 mode selection bit 00: Mode 0, TL0 and TH0 form a 13-bit timer/counter 01: Mode 1, TL0 and TH0 form a 16-bit timer/counter 10: Mode 2, TL0 as 8-bit timer/counter, TH0 as auto reload register 11: Mode 3, TL0 and TH0 as two completely independent 8-bit timer/counters
0	T0M0	

Table 12-1-2-3 Register TL0

8AH	7	6	5	4	3	2	1	0
TL0	TL0							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description

7~0	TL0	Timer 0 low byte of mode 0/1 count value, mode 2/3 count value

Table 12-1-2-4 Register TH0

8CH	7	6	5	4	3	2	1	0
TH0	TH0							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
Bit Number	Bit Symbol	Description						
7~0	TH0	Timer 0 high byte of mode 0/1 count value, mode 2 reload value, mode 3 count value						

12.2 Timer 1

12.2.1 Timer 1 Introduction

The timer or counter function is selected by the CT1 bit (TMOD[6]), with CT1=0 selected as a timer and CT1=1 selected as a counter. When used as a timer, the clock is 12 divisions of the system clock. When used as a counter, the clock is the input clock of T1. Since it takes 2 clock cycles to detect T1 input edge changes, the maximum input baud rate as a counter is 1/2 of the internal system clock frequency. the T1 input signal is not limited in duty cycle, however, in order to fully identify a 0 or 1 state, the signal needs to be held for at least 1 internal system clock cycle time. Timer 1 has 4 operating modes, which are selected by T1M0, T1M1 bits (TMOD[5:4])

- **Mode 0**

In this mode, timer 1 acts as a 13-bit timer/counter. TH1 holds the high 8 bits of the 13-bit timer/counter, TL1[4:0] holds the low 5 bits, and TL1[7:5] is invalid and should be ignored when read. When timer 1 overflows, interrupt flag bit TF1 (TCON[7]) will be set to 1. TF1 bit will be automatically cleared to 0 after the interrupt is responded. when GATE1 (TCON[7]) = 0, the timer/counter is enabled to count by TR1 (TCON[6]) bit, when GATE1 = 1, the timer/counter is enabled by pin INT1 control, when INT1 is high When GATE1=1, the timer/counter is enabled by pin INT1 and stops counting when INT1 is high.

- **Mode 1**

In this mode, timer 1 acts as a 16-bit timer/counter, TH1 holds the high 8 bits of the 16-bit timer/counter and TL1 holds the low 8 bits. When timer 1 overflows, interrupt flag bit TF1 (TCON[7]) will be set to 1. TF1 bit will be cleared to 0 automatically when the interrupt is responded. When GATE1=1, the timer/counter is enabled by pin INT1 and stops counting when INT1 is high.

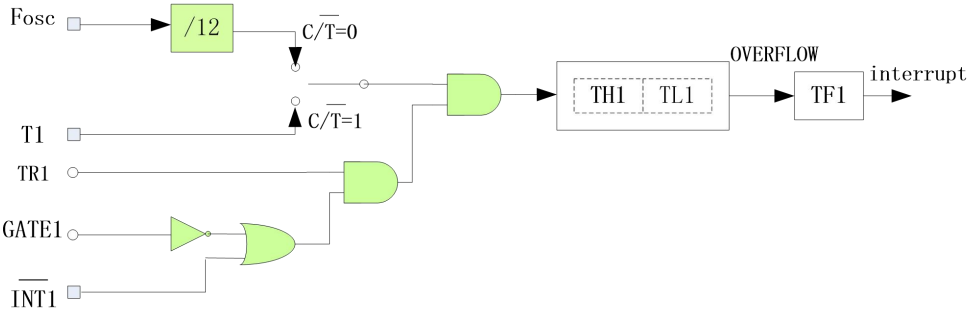


Figure 12-2-1 Mode 0 and 1 of Timer 1

- **Mode 2**

In this mode, Timer 1 serves as an 8-bit automatic overload timer/counter, and only TL1 automatically accumulates. When the TL1 count overflows, not only does it generate the interrupt flag TF1, but it also automatically loads the count Initial Value from TH1 to TL1. The other setting methods and modes 0 and 1 are the same.

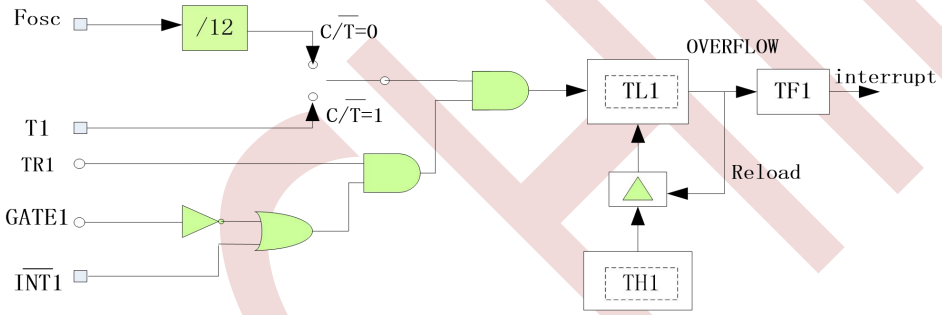


Figure 12-2-2 Mode 2 of Timer 1

- **Mode 3**

In this mode, TH1 and TL1 will be locked, which is equivalent to TR1=0.

12.2.2 Timer 1 Register Description

The registers TCON and TMOD are shown in Table 12-1-2-1 and Table 12-1-2-2.

Table 12-2-2-1 Register TL1

8BH	7	6	5	4	3	2	1	0
TL1	TL1							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
Bit Number	Bit Symbol	Description						
7~0	TL1	Timer 1 low byte of mode 0/1 count value, mode 2/3 count value						

Table 12-2-2-2 Register TH1

8DH	7	6	5	4	3	2	1	0
TH1	TH1							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~0	TH1	Timer 1 high byte of mode 0/1 count value, mode 2 reload value, mode 3 count value

12.3 Timer 2

12.3.1 Timer2 Introduction

Timer 2 is a 16 bit timer, and the clock of Timer 2 is the system clock (note: unlike timers 0 and 1, the clock has not undergone a 12 division). Set different working modes through T2M.

When T2M=0, timer 2 operates in timer mode, and T2CRH and T2CRL store the upper limit value of the count. When Timer 2 is enabled, the 16 bit counter automatically accumulates. When the timer count reaches the set upper limit value, a timed interrupt flag TF1 is generated. The 16 bit counter is reset to zero, and the interrupt flag TF2 is cleared by writing 1 to 0.

When T2M=1, timer 2 operates in capture mode. When the trigger edge of pin T2CP occurs, the count value of timer 2 is locked to T2CRH and T2CRL. The trigger edge can be set through the CPEDGESEL bit. After the capture event occurs, the capture interrupt flag CF2 is set to 1. If timer 2 interrupts, it will trigger the capture interrupt, and CF2 will clear 0 by writing 1. In capture mode, counter overflow will generate overflow interrupt flag OF2, which is cleared by writing 1 to OF2.

Note: The T2CP pin can be mapped to different GPIO pins, as detailed in the "15-2-9 Pin Multiplexing Function Mapping Table".

12.3.2 Timer2 Register Description

Table 12-3-2-1 Register T2CON

A4H	7	6	5	4	3	2	1	0
T2CON	TR2	IE2	TF2	OF2	CF2	CPEDGESEL		T2M
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	TR2	Timer 2 working enabled, 1 effective
6	IE2	Timer 2 interrupt enable, 1 valid
5	TF2	Timer interrupt flag, write 1 clear 0

4	OF2	Overflow interrupt flag, write 1 clear 0
3	CF2	Capture interrupt flag bit, write 1 clear 0
2~1	CPEDGESEL	Capture mode trigger edge selection: 0, 3: Double edge trigger 1: Descending edge 2: Rising edge
0	T2M	Timing/capture function selection: 0: Timer mode 1: Capture mode

Table 12-3-2-2 Register T2CRL

A6H	7	6	5	4	3	2	1	0
T2CRL	TL2							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
Bit Number	Bit Symbol	Description						
7~0	T2CRL	T2M=0: Timer Count Upper Limit Low Byte T2M=1: Capture result low byte						

Table 12-3-2-3 Register T2CRH

A5H	7	6	5	4	3	2	1	0
T2CRH	TH2							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
Bit Number	Bit Symbol	Description						
7~0	T2CRH	T2M=0: Timer count upper limit value high byte T2M=1: Capture high byte of result						

13 Watchdog Timer (WDT)

13.1 Watchdog Timer (WDT) Function Introduction

The watchdog timer is a 27 bit subtraction counter with an optional clock source and 16 bit adjustment accuracy. Watchdogs are mainly used for monitoring systems to prevent CPU crashes due to external interference. If the software cannot refresh the watchdog timer before overflow, the watchdog will generate an internal reset or interrupt. Writing A5H to register WDFLG will refresh the watchdog, and reading WDFLG will obtain the watchdog status. In STOP mode, if the watchdog is in the enabled state, the clock source selected by the watchdog is working normally. At this time, if the watchdog is set to interrupt, the watchdog interrupt can wake up the CPU.

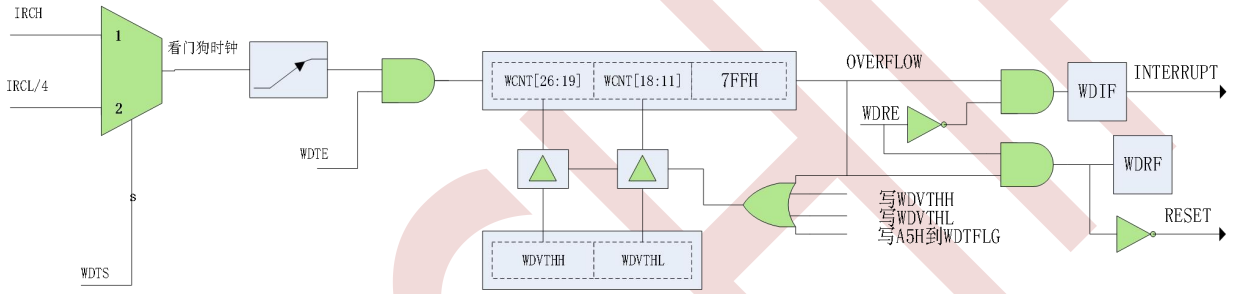


Figure 13-1-1 Watchdog Module Architecture

13.2 Watchdog Timer (WDT) Register Description

Table 13-2-1 Register WDCON

A7H	7	6	5	4	3	2	1	0
WDCON	WDTS[1:0]		-	-	-	-	-	WDRE
R/W	R/W		-	-	-	-	-	R/W
Initial Value	0	0	-	-	-	-	-	0

Bit Number	Bit Symbol	Description
7~6	WDTS	WDT Clock selection 001: IRCH 010: IRCL with frequency divided by 4 Other: WDT disabled
5~1	-	-
0	WDRE	WDT function selection 0: interrupt happens when WDT overflows 1: reset happens when WDT overflows

Table 13-2-2 Register WDFLG

A1H	7	6	5	4	3	2	1	0
WDFLG	-						WDIF	WDRF
R/W	-						R/W	R/W
Initial Value	-	-	-	-	-	-	0	0

Bit Number	Bit Symbol	Description
7~2	-	-
1	WDIF	WDT interrupt flag, writing A5H to the register will clear it
0	WDRF	WDT reset flag, writing A5H to the register will clear it

Table 13-2-3 Register WDVTHL, WDVTHH

A2H	7	6	5	4	3	2	1	0
WDVTHL	WDVTH[7:0]							
R/W	R/W							
Initial Value	1	1	1	1	1	1	1	1
A3H	7	6	5	4	3	2	1	0
WDVTHH	WDVTH[15:8]							
R/W	R/W							
Initial Value	1	1	1	1	1	1	1	1

Bit Number	Bit Symbol	Description
15~0	WDVTH	WDT threshold setting, the equation is as follows: WDT trigger time ＝ (WDVTH * 800H+7FFH) * clock cycle

13.3 Watchdog Timer Control Example

◆ Example for Watchdog interrupt mode

For example, if the watchdog clock is set to IRCH, the frequency of IRCH is 12MHz, the watchdog is set to interrupt mode, and the overflow time is 1 second, the program is as follows:

```
--------------------------------------------------------------------------------
void WDT_init(void)
{
    WDCON = (1<<6) | 0;              // set the clock as IRCH and watchdog in interrupt mode
    WDVTHH = 0x16;                   // set one second as the time for watchdog
    WDVTHL = 0xE2;
    WDFLG = 0xA5;                    // Refresh the Watchdog
    INT4EN = 1;                      // Turn on watchdog interrupt
    EA = 1;                          // Turn on total interruption
}
void WDT_ISR (void) interrupt 6
{
    if(WDFLG & 0x02)
    {
        WDFLG = 0xA5;                // Refresh Watchdog
    }
}
--------------------------------------------------------------------------------
```

◆ Example for watchdog reset mode

For example, if the watchdog clock is set to IRCH, the frequency of IRCH is 12MHz, the watchdog is set to reset mode, and the overflow time is 1 second, the program is as follows:

```
--------------------------------------------------------------------------------
void WDT_init(void)
{
    WDCON = (1<<6) | 1;              // Set watchdog clock to IRCH, watchdog reset mode
    WDVTHH = 0x16;                   // set one second as the time for watchdog
    WDVTHL = 0xE2;
    WDFLG = 0xA5;                    // Refresh the Watchdog
}
--------------------------------------------------------------------------------
```

14 TMC Timer

14.1 TMC Function Introduction

The clock source of TMC timer can be IRCL or XOSCL. When the clock source is IRCL, the minimum unit of interrupt time is 512 clock cycles. When the clock source is XOSCL, the minimum unit of interrupt is 128 clock cycles, and the configurable interrupt time is 1-256 minimum unit times. In STOP/IDLE mode, TMC interrupts can wake up the CPU.

14.2 TMC Register Description

Table 14-2-1 Register TMCON

D5H	7	6	5	4	3	2	1	0
TMCON	TME	-	-	-	-	-	-	TMF
R/W	R/W	-	-	-	-	-	-	R
Initial Value	0	-	-	-	-	-	-	0

Bit Number	Bit Symbol	Description
7	TME	TME module enable, 1 active
6~1	-	-
0	TMF	TMC interrupt flag, 1 valid, write 1 to clear 0

Table 14-2-2 Register TMSNU

D6H	7	6	5	4	3	2	1	0
TMSNU	TMSNU[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	-

Bit Number	Bit Symbol	Description
7~0	TMSNU	TMC interrupt time configuration register When the clock source of the TMC timer is IRCL, the interrupt time of the TMC is (TMSNU+1) × 512 × Tircl; When the clock source of the TMC timer is XOSCL, the interrupt time of the TMC is (TMSNU+1) x128 × Txoscl

14.3 TMC Control Routines

program as follows.

```
-------------------------------------------------------------------------------
#define TME(N)                  (N<<7)    // N=0-1 TME module enabled, 1 effective
#define TMF                     (1<<0)    // TMC interrupt flag, 1 valid, write 1 clear 0

#define XLCKE                   (1<<4)    // XOSC clock enable control bit
#define ILCKE                   (1<<6)    // IRCL enable control bit
#define TMCS(N)                 (N<<1)    // N=0-1, TMC counting clock selection
#define TMC_CLK_SELECT                    ILCKE
void INT3_ISR (void) interrupt 5
{
    if(TMCON & TMF)                       // Determine TMC interrupt flag
    {
        TMCON |= TMF;                     // Clear TMC interrupt flag

    }
}

void TMC_Init(void)
{
#if (TMC_CLK_SELECT == ILCKE)
    CKCON |= ILCKE;                       // Turn on IRCL clock
    CKCON |= TMCS(0);                     // TMC counting clock selection IRCL clock
#elif (TMC_CLK_SELECT == XLCKE)
    P55F = 10;                            // Set P5.5 as the crystal oscillator pin
    P54F = 10;                            // Set P5.4 as the crystal oscillator pin
    CKCON |= XLCKE;                       // Enable XOSCL clock
    CKCON |= TMCS(1);                     // TMC counting clock XOSCL clock
#endif
    TMCON = TME(1);                       // TMC enable
    TMSNU = 0;                            // Set interruption time
    INT3EN =1;                            // Enable TMC interrupt
    EA = 1;                               // Enable Total Interrupt
}
-------------------------------------------------------------------------------
```

15 General Purpose Input/Output(GPIO) and Alternate Functions

15.1 Function Introduction

The CA51F155 series chip has a maximum package of 46 I/O pins, each of which is a multiplexed function pin. It can be independently programmed as an input/output port and can also be set as other function pins. Each pin is assigned a function setting register PnxF (corresponding to pin Pnx, where n=0~5 represents P0, P1, P2, P3, P4, P5, x=0~7 represents Pn. 0~Pn. 7), and users can configure the main function and other options of the pin through the register PnxF. Please refer to the register section for details.

Main features of GPIO：

- High impedance mode configurable
- The I/O structure can independently set pull-up and pull-down resistors
- Output mode can be open-drain or push-pull output
- Data output latch supports read modify write
- When pushing and pulling output, the maximum current of a single GPIO source can reach 15mA@5v The maximum current can reach 40mA@5v
- 8 high current GPIOs (P3.0~P3.7), with a maximum current of up to 90ma@5v , can be used for bright LED screen display

The GPIO push-pull mode structure diagram is shown in Figure

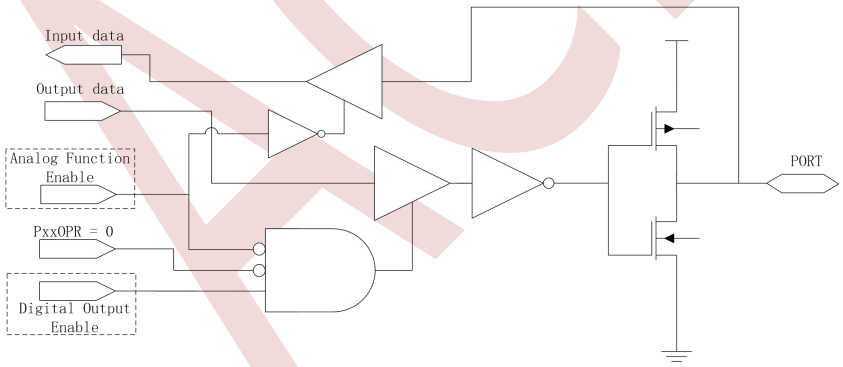


Figure 15-1-1 I/O Push-pull Mode Structure

The Figure 15-1-2 shows GPIO Open-drain Mode Structure

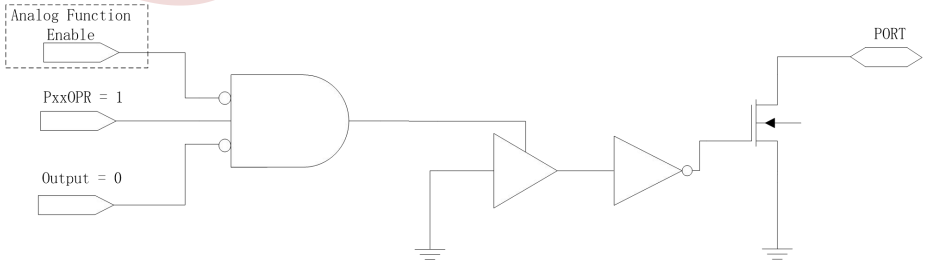


Figure 15-1-2 I/O Open-drain Mode Structure

The GPIO pull-down structure diagram is shown in Figure 15-1-3.

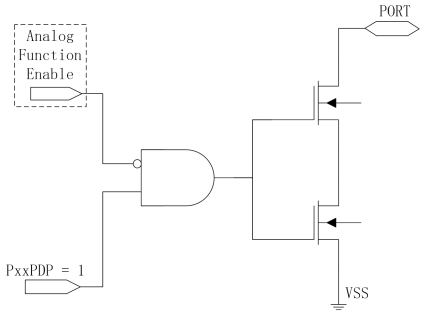


Figure 15-1-3 I/O Pull-down Mode Structure

The Figure 15-1-4 shows GPIO Pull-up Mode Structure

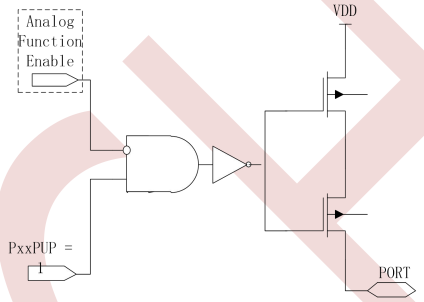


Figure 15-1-4 I/O Pull-up Mode Structure

15.2 Pin Register Description

Table 15-2-1 Register P0

80H	7	6	5	4	3	2	1	0
P0	P07	P06	P05	P04	P03	P02	P01	P00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0
Bit Number	Bit Symbol	Description						
7~0	P0x	Data register for pin P0x，valid when the pin function is set to GPIO 0:P0x is low level when the pin is set to input; when the pin set to output,P0x outputs low level signal						

		1:P0x is high level when the pin is set to input; when the pin set to output,P0x outputs high level signal

Table 15-2-2 Register P1

90H	7	6	5	4	3	2	1	0
P1	P17	P16	P15	P14	P13	P12	P11	P10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~0	P1x	Data register for pin P1x,valid when the pin function is set to GPIO 0: P1x is low level when the pin is set to input; when the pin set to output,P1x outputs low level signal 1: P1x is high level when the pin is set to input; when the pin set to output,P1x outputs high level signal

Table 15-2-3 Register P2

A0H	7	6	5	4	3	2	1	0
P2	P27	P26	P25	P24	P23	P22	P21	P20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~0	P2x	Data register for pin P2x，valid when the pin function is set to GPIO 0: P2x is low level when the pin is set to input; when the pin set to output,P2x outputs low level signal 1: P2x is high level when the pin is set to input; when the pin set to output,P2x outputs high level signal

Table 15-2-4 Register P3

B0H	7	6	5	4	3	2	1	0
P3	P37	P36	P35	P34	P33	P32	P31	P30
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~0	P3x	Data register for pin P3x, valid when the pin function is set to GPIO 0: P3x is low level when the pin is set to input; when the pin set to output,P3x outputs low level signal 1: P3x is high level when the pin is set to input; when the pin set to output,P3x outputs high

		level signal

Table 15-2-5 Register P4

E1H	7	6	5	4	3	2	1	0
P4	P47	P46	P45	P44	P43	P42	P41	P40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~0	P4x	Data register for pin P4x, valid when the pin function is set to GPIO 0: P4x is low level when the pin is set to input; when the pin set to output,P4x outputs low level signal 1: P4x is high level when the pin is set to input; when the pin set to output,P4x outputs high level signal

Table 15-2-6 Register P5

E2H	7	6	5	4	3	2	1	0
P5	-	-	P55	P54	P53	P52	P51	P50
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	-	-	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
5~0	P5x	Data register for pin P5x, valid when the pin function is set to GPIO 0: P5x is low level when the pin is set to input; when the pin set to output,P5x outputs low level signal 1: P5x is high level when the pin is set to input; when the pin set to output,P5x outputs high level signal

Table 15-2-7 Pin Function Control Register

8000H	7	6	5	4	3	2	1	0
P00F	P00PUP	P00PDP	P00OPR	-	P00S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	1	1	0
8001H	7	6	5	4	3	2	1	0
P01F	P01PUP	P01PDP	P01OPR	-	P01S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	1	1	1

8002H	7	6	5	4	3	2	1	0
P02F	P02PUP	P02PDP	P02OPR	-	P02S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8003H	7	6	5	4	3	2	1	0
P03F	P03PUP	P03PDP	P03OPR	-	P03S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8004H	7	6	5	4	3	2	1	0
P04F	P04PUP	P04PDP	P04OPR	-	P04S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8005H	7	6	5	4	3	2	1	0
P05F	P05PUP	P05PDP	P05OPR	-	P05S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8006H	7	6	5	4	3	2	1	0
P06F	P06PUP	P06PDP	P06OPR	-	P06S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8007H	7	6	5	4	3	2	1	0
P07F	P07PUP	P07PDP	P07OPR	-	P07S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8008H	7	6	5	4	3	2	1	0
P10F	P10PUP	P10PDP	P10OPR	-	P10S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8009H	7	6	5	4	3	2	1	0
P11F	P11PUP	P11PDP	P11OPR	-	P11S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
800AH	7	6	5	4	3	2	1	0
P12F	P12PUP	P12PDP	P12OPR	-	P12S			
R/W	R/W	R/W	R/W	-	R/W			

Initial Value	0	0	0	-	0	0	0	0
800BH	7	6	5	4	3	2	1	0
P13F	P13PUP	P13PDP	P13OPR	-	P13S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
800CH	7	6	5	4	3	2	1	0
P14F	P14PUP	P14PDP	P14OPR	-	P14S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
800DH	7	6	5	4	3	2	1	0
P15F	P15PUP	P15PDP	P15OPR	-	P15S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
800EH	7	6	5	4	3	2	1	0
P16F	P16PUP	P16PDP	P16OPR	-	P16S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
800FH	7	6	5	4	3	2	1	0
P17F	P17PUP	P17PDP	P17OPR	-	P17S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8010H	7	6	5	4	3	2	1	0
P20F	P20PUP	P20PDP	P20OPR	-	P20S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8011H	7	6	5	4	3	2	1	0
P21F	P21PUP	P21PDP	P21OPR	-	P21S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8012H	7	6	5	4	3	2	1	0
P22F	P22PUP	P22PDP	P22OPR	-	P22S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8013H	7	6	5	4	3	2	1	0

P23F	P23PUP	P23PDP	P23OPR	-	P23S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8014H	7	6	5	4	3	2	1	0
P24F	P24PUP	P24PDP	P24OPR	-	P24S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8015H	7	6	5	4	3	2	1	0
P25F	P24PUP	P25PDP	P25OPR	-	P25S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8016H	7	6	5	4	3	2	1	0
P26F	P26PUP	P26PDP	P26OPR	-	P26S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-		0	0	0
8017H	7	6	5	4	3	2	1	0
P27F	P27PUP	P27PDP	P27OPR	-	P27S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8018H	7	6	5	4	3	2	1	0
P30F	P30PUP	P30PDP	P30OPR	-	P30S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8019H	7	6	5	4	3	2	1	0
P31F	P31PUP	P31PDP	P31OPR	-	P31S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
801AH	7	6	5	4	3	2	1	0
P32F	P32PUP	P32PDP	P32OPR	-	P32S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
801BH	7	6	5	4	3	2	1	0
P33F	P33PUP	P33PDP	P33OPR	-	P33S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0

801CH	7	6	5	4	3	2	1	0
P34F	P34PUP	P34PDP	P34OPR	-	P34S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
801DH	7	6	5	4	3	2	1	0
P35F	P35PUP	P35PDP	P35OPR	-	P35S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
801EH	7	6	5	4	3	2	1	0
P36F	P36PUP	P36PDP	P36OPR	-	P36S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
801FH	7	6	5	4	3	2	1	0
P37F	P37PUP	P37PDP	P37OPR	-	P37S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8040H	7	6	5	4	3	2	1	0
P40F	P40PUP	P40PDP	P40OPR	-	P40S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8041H	7	6	5	4	3	2	1	0
P41F	P41PUP	P41PDP	P41OPR	-	P41S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8042H	7	6	5	4	3	2	1	0
P42F	P42PUP	P42PDP	P42OPR	-	P42S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8043H	7	6	5	4	3	2	1	0
P43F	P43PUP	P43PDP	P43OPR	-	P43S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8044H	7	6	5	4	3	2	1	0
P44F	P44PUP	P44PDP	P44OPR	-	P44S			

R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8045H	7	6	5	4	3	2	1	0
P45F	P45PUP	P45PDP	P45OPR	-	P45S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8046H	7	6	5	4	3	2	1	0
P46F	P46PUP	P46PDP	P46OPR	-	P46S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8047H	7	6	5	4	3	2	1	0
P47F	P47PUP	P47PDP	P47OPR	-	P47S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8048H	7	6	5	4	3	2	1	0
P50F	P50PUP	P50PDP	P50OPR	-	P50S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
8049H	7	6	5	4	3	2	1	0
P51F	P51PUP	P51PDP	P51OPR	-	P51S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
804AH	7	6	5	4	3	2	1	0
P52F	P52PUP	P52PDP	P52OPR	-	P52S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
804BH	7	6	5	4	3	2	1	0
P53F	P53PUP	P53PDP	P53OPR	-	P53S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0
804CH	7	6	5	4	3	2	1	0
P54F	P54PUP	P54PDP	P54OPR	-	P54S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0

804DH	7	6	5	4	3	2	1	0
P55F	P55PUP	P55PDP	P55OPR	-	P55S			
R/W	R/W	R/W	R/W	-	R/W			
Initial Value	0	0	0	-	0	0	0	0

Bit Number	Bit Symbol	Description
7	PnxPUP	Pull-up resistor enable control 0: disable pull-up resistor 1: enable pull-up resistor
6	PnxPDP	Pull-down resistor enable 0: disable pull-down resistor 1: enable pull-down resistor
5	PnxOPR	Open-drain enable control, only valid when the pin is set to be digital output 0: disable open-drain 1: enable open-drain
4	-	-
3~0	PnxS	The pin reuse function settings are detailed in Table 15-2-9

Note: Pnx → n=0, 1, 2, 3,4,5 representing P0, P1, P2, P3,P4,P5 X=0~7, representing Pn. 0~Pn. 7

Table 15-2-8 Register PnxC

8120H	7	6	5	4	3	2	1	0
P00C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8121H	7	6	5	4	3	2	1	0
P01C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8122H	7	6	5	4	3	2	1	0
P02C	-	SMIT_EN	-	-		-	DRV	SR
R/W	-	R/W	-	-		-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8123H	7	6	5	4	3	2	1	0
P03C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8124H	7	6	5	4	3	2	1	0

P04C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8125H	7	6	5	4	3	2	1	0
P05C	-	SMIT_EN	-	-		-	DRV	DRV
R/W	-	R/W	-	-		-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8126H	7	6	5	4	3	2	1	0
P06C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	0	0	0	0	0
8127H	7	6	5	4	3	2	1	0
P07C	-	SMIT_EN	-	-	-	-	DRV	DRV
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8128H	7	6	5	4	3	2	1	0
P10C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8129H	7	6	5	4	3	2	1	0
P11C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
812AH	7	6	5	4	3	2	1	0
P12C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
812BH	7	6	5	4	3	2	1	0
P13C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
812CH	7	6	5	4	3	2	1	0
P14C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0

812DH	7	6	5	4	3	2	1	0
P15C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
812EH	7	6	5	4	3	2	1	0
P16C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
812FH	7	6	5	4	3	2	1	0
P17C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8130H	7	6	5	4	3	2	1	0
P20C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8131H	7	6	5	4	3	2	1	0
P21C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8132H	7	6	5	4	3	2	1	0
P22C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8133H	7	6	5	4	3	2	1	0
P23C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8134H	7	6	5	4	3	2	1	0
P24C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8135H	7	6	5	4	3	2	1	0
P25C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W

Initial Value	-	1	-	-	-	-	0	0
8136H	7	6	5	4	3	2	1	0
P26C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8137H	7	6	5	4	3	2	1	0
P27C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8138H	7	6	5	4	3	2	1	0
P30C	-	SMIT_EN	-	SINK[1:0]		SINK_EN	DRV	SR
R/W	-	R/W	-	R/W		R/W	R/W	R/W
Initial Value	-	1	-	0	0	0	0	0
8139H	7	6	5	4	3	2	1	0
P31C	-	SMIT_EN	-	SINK[1:0]		SINK_EN	DRV	SR
R/W	-	R/W	-	R/W		R/W	R/W	R/W
Initial Value	-	1	-	0	0	0	0	0
813AH	7	6	5	4	3	2	1	0
P32C	-	SMIT_EN	-	SINK[1:0]		SINK_EN	DRV	SR
R/W	-	R/W	-	R/W		R/W	R/W	R/W
Initial Value	-	1	-	0	0	0	0	0
813BH	7	6	5	4	3	2	1	0
P33C	-	SMIT_EN	-	SINK[1:0]		SINK_EN	DRV	SR
R/W	-	R/W	-	R/W		R/W	R/W	R/W
Initial Value	-	1	-	0	0	0	0	0
813CH	7	6	5	4	3	2	1	0
P34C	-	SMIT_EN	-	SINK[1:0]		SINK_EN	DRV	SR
R/W	-	R/W	-	R/W		R/W	R/W	R/W
Initial Value	-	1	-	0	0	-	0	0
813DH	7	6	5	4	3	2	1	0
P35C	-	SMIT_EN	-	SINK[1:0]		SINK_EN	DRV	SR
R/W	-	R/W	-	R/W		R/W	R/W	R/W
Initial Value	-	1	-	0	0	0	0	0
813EH	7	6	5	4	3	2	1	0

P36C	-	SMIT_EN	-	SINK[1:0]		SINK_EN	DRV	SR
R/W	-	R/W	-	R/W		R/W	R/W	R/W
Initial Value	-	1	-	0	0	0	0	0
813FH	7	6	5	4	3	2	1	0
P37C	-	SMIT_EN	-	SINK[1:0]		SINK_EN	DRV	SR
R/W	-	R/W	-	R/W		R/W	R/W	R/W
Initial Value	-	1	-	0	0	0	0	0
8050H	7	6	5	4	3	2	1	0
P40C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8051H	7	6	5	4	3	2	1	0
P41C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8052H	7	6	5	4	3	2	1	0
P42C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8053H	7	6	5	4	3	2	1	0
P43C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8054H	7	6	5	4	3	2	1	0
P44C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8055H	7	6	5	4	3	2	1	0
P45C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0
8056H	7	6	5	4	3	2	1	0
P46C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0

8057H	7	6	5	4	3	2	1	0
P47C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0

8058H	7	6	5	4	3	2	1	0
P50C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0

8059H	7	6	5	4	3	2	1	0
P51C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0

805AH	7	6	5	4	3	2	1	0
P52C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0

805BH	7	6	5	4	3	2	1	0
P53C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0

805CH	7	6	5	4	3	2	1	0
P54C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0

805DH	7	6	5	4	3	2	1	0
P55C	-	SMIT_EN	-	-	-	-	DRV	SR
R/W	-	R/W	-	-	-	-	R/W	R/W
Initial Value	-	1	-	-	-	-	0	0

Bit Number	Bit Symbol	Description
7	-	-
6	SMIT_EN	SMIT enable for input 1, inverter enable for input 0
5	-	-

4~3	SINK[1:0]	P3.0~P3.7 Selection of current injection intensity Note: 1. Invalid settings for pins other than P3.0~P3.7 2. The fourth level drive current is optional, please refer to the electrical characteristics section for details
2	SINK_EN	SINK_ EN: P3.0~P3.7 pin high current enable Note: 1. Invalid settings for pins other than P3.0~P3.7 2. When SINK_ When EN=0, the output strength of pins P3.0~P3.7 is set by DRV
1	DRV	Output intensity selection Note: The two-stage drive current is optional, please refer to the Electrical Characteristics section for details
0	SR	Output slope control 0: Slowest slope control 1: Fastest slope control

Table 15-2-9 Pin Multiplexing Function Mapping Table

Take value / Name	0	1	2	3	4	5	6	7	8	9	10	11	12
P00S	High resistance	Digital Input	Digital Output	PWM0	ADC0	TK0	I2C_SDA	I2C_SCL	UART0_RX	UART0_TX	C2N	-	-
P01S	High resistance	Digital Input	Digital Output	PWM1	ADC1	TK1	I2C_SDA	I2C_SCL	UART0_RX	UART0_TX	C2P	-	-
P02S	High resistance	Digital Input /T0	Digital Output	PWM2	ADC2	TK2	I2C_SDA	I2C_SCL	UART0_RX	UART0_TX	C1N	SEG21	-
P03S	High resistance	Digital Input /T1	Digital Output	PWM3	ADC3	TK3	I2C_SDA	I2C_SCL	UART0_RX	UART0_TX	C1P	SEG20	-
P04S	High resistance	Digital Input	Digital Output	PWM4	ADC4	TK4	I2C_SDA	I2C_SCL	UART0_RX	UART0_TX	-	SEG19	-
P05S	High resistance	Digital Input	Digital Output	PWM5	ADC5	TK5	I2C_SDA	I2C_SCL	UART0_RX	UART0_TX	-	SEG18	-
P06S	High resistance	Digital Input	Digital Output	PWM0	ADC6	TK6	I2C_SDA	I2C_SCL	UART0_RX	UART0_TX	-	SEG17	-
P07S	High resistance	Digital Input	Digital Output	PWM1	ADC7	TK7	I2C_SDA	I2C_SCL	UART0_RX	UART0_TX	-	SEG16	-
P10S	High resistance	Digital Input	Digital Output	PWM2	ADC8	TK8	I2C_SDA	I2C_SCL	UART1_RX	UART1_TX	T2CP	SEG15	-
P11S	High resistance	Digital Input	Digital Output	PWM3	ADC9	TK9	I2C_SDA	I2C_SCL	UART1_RX	UART1_TX	T2CP	SEG14	-
P12S	High resistance	Digital Input	Digital Output	PWM4	ADC10	TK10	I2C_SDA	I2C_SCL	UART1_RX	UART1_TX	SPI_CS	SEG13	-
P13S	High resistance	Digital Input	Digital Output	PWM5	ADC11	TK11	I2C_SDA	I2C_SCL	UART1_RX	UART1_TX	SPI_CLK	SEG12	-
P14S	High	Digital	Digital	PWM0	ADC12	TK12	I2C_SDA	I2C_SCL	UART1_RX	UART1_TX	SPI_MISO	SEG11	SPI_MOSI

	resistance	Input	Output										
P15S	High resistance	Digital Input	Digital Output	PWM1	ADC13	TK13	I2C_SDA	I2C_SCL	UART1_RX	UART1_TX	SPI_MOSI	SEG10	SPI_MISO
P16S	High resistance	Digital Input	Digital Output	PWM2	ADC14	TK14	I2C_SDA	I2C_SCL	UART1_RX	UART1_TX	T2CP	SEG9	-
P17S	High resistance	Digital Input	Digital Output	PWM3	ADC15	TK15	I2C_SDA	I2C_SCL	UART1_RX	UART1_TX	T2CP	SEG8	-
P20S	High resistance	Digital Input	Digital Output	PWM4	ADC16	TK16	I2C_SDA	I2C_SCL	UART1_RX	UART1_TX	T2CP	SEG7	-
P21S	High resistance	Digital Input	Digital Output	PWM5	ADC17	TK17	I2C_SDA	I2C_SCL	UART1_RX	UART1_TX	T2CP	SEG6	-
P22S	High resistance	Digital Input	Digital Output	PWM0	ADC18	TK18	I2C_SDA	I2C_SCL	UART1_RX	UART1_TX	T2CP	SEG5	-
P23S	High resistance	Digital Input	Digital Output	PWM1	ADC19	TK19	I2C_SDA	I2C_SCL	UART1_RX	UART1_TX	T2CP	SEG4	-
P24S	High resistance	Digital Input	Digital Output	PWM2	ADC20	TK20	I2C_SDA	I2C_SCL	UART1_RX	UART1_TX	T2CP	SEG3	-
P25S	High resistance	Digital Input	Digital Output	PWM3	ADC21	TK21	I2C_SDA	I2C_SCL	UART1_RX	UART1_TX	SPI_CLK	SEG2	-
P26S	High resistance	Digital Input	Digital Output	PWM4	ADC22	TK22	I2C_SDA	I2C_SCL	UART1_RX	UART1_TX	SPI_MISO	SEG1	-
P27S	High resistance	Digital Input	Digital Output	PWM5	ADC23	TK23	I2C_SDA	I2C_SCL	UART1_RX	UART1_TX	SPI_MOSI	SEG0	-
P30S	High resistance	Digital Input	Digital Output	PWM0	ADC24	TK24	I2C_SDA	I2C_SCL	UART2_RX	UART2_TX	SPI_CS	-	COM0
P31S	High resistance	Digital Input	Digital Output	PWM1	ADC25	TK25	I2C_SDA	I2C_SCL	UART2_RX	UART2_TX	T2CP	-	COM1
P32S	High resistance	Digital Input	Digital Output	PWM2	ADC26	TK26	I2C_SDA	I2C_SCL	UART2_RX	UART2_TX	T2CP	-	COM2

P33S	High resistance	Digital Input	Digital Output	PWM3	ADC27	TK27	I2C_SDA	I2C_SCL	UART2_RX	UART2_TX	SPI_CLK	-	COM3
P34S	High resistance	Digital Input	Digital Output	PWM4	ADC28	TK28	I2C_SDA	I2C_SCL	UART2_RX	UART2_TX	SPI_MOSI	SEG35	COM4
P35S	High resistance	Digital Input	Digital Output	PWM5	ADC29	TK28	I2C_SDA	I2C_SCL	UART2_RX	UART2_TX	SPI_MISO	SEG34	COM5
P36S	High resistance	Digital Input	Digital Output	PWM0	ADC30	TK30	I2C_SDA	I2C_SCL	UART2_RX	UART2_TX	SPI_CS	SEG33	COM6
P37S	High resistance	Digital Input	Digital Output	PWM1	ADC31	TK31	I2C_SDA	I2C_SCL	UART2_RX	UART2_TX	T2CP	SEG32	COM7
P40S	High resistance	Digital Input	Digital Output	PWM2	ADC32	TK32	I2C_SDA	I2C_SCL	UART2_RX	UART2_TX	T2CP	SEG31	-
P41S	High resistance	Digital Input	Digital Output	PWM3	ADC33	TK33	I2C_SDA	I2C_SCL	UART2_RX	UART2_TX	T2CP	SEG30	-
P42S	High resistance	Digital Input	Digital Output	PWM4	ADC34	T34	I2C_SDA	I2C_SCL	UART2_RX	UART2_TX	T2CP	SEG29	-
P43S	High resistance	Digital Input	Digital Output	PWM5	ADC35	TK35	I2C_SDA	I2C_SCL	UART2_RX	UART2_TX	T2CP	SEG28	-
P44S	High resistance	Digital Input	Digital Output	PWM0	ADC36	TK36	I2C_SDA	I2C_SCL	UART2_RX	UART2_TX	T2CP	SEG27	-
P45S	High resistance	Digital Input	Digital Output	PWM1	ADC37	TK37	I2C_SDA	I2C_SCL	UART2_RX	UART2_TX	T2CP	SEG26	-
P46S	High resistance	Digital Input	Digital Output	PWM2	ADC38	TK38	I2C_SDA	I2C_SCL	UART2_RX	UART2_TX	T2CP	SEG25	-
P47S	High resistance	Digital Input	Digital Output	PWM3	ADC39	TK39	I2C_SDA	I2C_SCL	UART2_RX	UART2_TX	T2CP	SEG24	-
P50S	High resistance	Digital Input	Digital Output	PWM4	ADC40	TK40	I2C_SDA	I2C_SCL	UART0_RX	UART0_TX	T2CP	SEG23	-
P51S	High resist	Digital Input	Digital Output	PWM5	ADC41	TK41	I2C_SDA	I2C_SCL	UART0_RX	UART0_TX	T2CP	SEG22	-

	ance												
P52S	High resistance	Digital Input	Digital Output	PWM0	ADC42	TK42	I2C_SDA	I2C_SCL	UART0_RX	UART0_TX	T2CP	-	-
P53S	High resistance	Digital Input	Digital Output	PWM1	ADC43	TK43	I2C_SDA	I2C_SCL	UART0_RX	UART0_TX	T2CP	RESET	-
P54S	High resistance	Digital Input	Digital Output	PWM2	ADC44	TK44	I2C_SDA	I2C_SCL	UART0_RX	UART0_TX	XTAL_IN	-	-
P55S	High resistance	Digital Input	Digital Output	PWM2	ADC45	TK45	I2C_SDA	I2C_SCL	UART0_RX	UART0_TX	XTAL_OUT	-	-

15.3 Pin control Example

◆ **Set the Pin function**

For example, P0.0 is set to push-pull output, outputting high and low levels. The program is as follows:

```
P00F = 2;
P00 = 1;        //Output High Level
P00 = 0;        //Output low level
```

P0.0 is set to open drain output, and the program is as follows:

```
P00F = (1<<5)|2;
```

P0.0 is set to open drain output and pull-up is turned on. The program is as follows:

```
P00F = (1<<7) | (1<<5) | 2;
```

P0.0 is set as the input function and pull-up is turned on. The program is as follows:

```
P00F = (1<<7) | 1;
```

P3.0 is set to push-pull output and set to high current mode. The program is as follows:

```
P30F = 2;
P30C = (P30C&0x40) | (3<<3) | (1<<2);
```

Note: P4 and P5 do not support bit operations

P4.0 is set to push-pull output, outputting high and low levels. The program is as follows:

```
P40F = 2;
P4|=0x01;           // Output High Level
P4&=~0x01;          // Output low level
```

P4.0 is set as the input function, and the program is as follows:

```
P40F = 1;
If(P4&0x01)
{
}
else
{
}
```

16 Universal Asynchronous Receiver/Transmitter (UART0/UART1/UART2)

16.1 Function Introduction

UART0/1/2 are two fully duplex asynchronous serial data transceivers with identical designs. UARTx (x=0, 1, 2, referring to UART0, UART1, UART2) also has a one byte receive cache. UARTx has two different working modes, as shown in Table 16-1-1.

The TX/RX of UART0/1/2 can be mapped to different GPIO pins, as detailed in the "15-2-9 Pin Multiplexing Function Mapping Table".

SMx	Mode	Description	Baud rate
0	A	9-bit asynchronous mode	CPUCLK/(32*(1024-SxREL))
1	B	8-bit asynchronous mode	CPUCLK/(32*(1024-SxREL))

Table 16-1-1 UARTx Working mode

The UARTx is designed with a dedicated baud rate generator and the baud rate is configured through registers SxRELL, SxRELH.

Figure 16-1-1 shows the schematic diagram of UARTx.

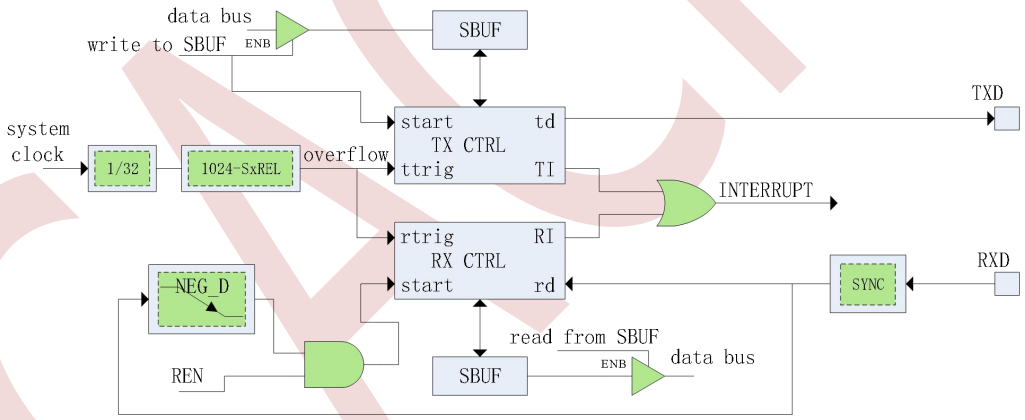


Figure 16-1-1 Schematic diagram of UARTx working principle

- **Mode A**

In mode A, the UARTx can send and receive 9 bits of data simultaneously asynchronously. Writing data to register SxBUF initiates UARTx data transmission. The first bit transmitted is the start bit (for 0), followed by 9 bits of data (low first), the 9th bit of data is the TB81 bit of register SxCON, and the last bit transmitted is the stop bit (for 1). In the receive state, UARTx is synchronized by detecting the falling edge of pin RX. After the transmission process is completed, the low 8 bits of data are stored in register SxBUF and the 9th bit of data is stored in bit RB8x.

- **Mode B**

Mode B differs from Mode A in that Mode B is an 8-bit data transfer, and the stop bit holds a valid stop bit.

Other functions are the same as Mode A.

- **UARTx Multi-Machine Communication**

There is a mechanism in UARTx mode A that is specifically applicable to multi-machine communication. When the SM2x position of register SxCON is 1, only the slave that receives the 9th bit data as 1 (RB8x=1) will generate the receive interrupt. Using this function, multi-machine communication can be performed; the slaves set all their SM2x bits to 1, and the host sets the 9th bit data to 1 when transmitting the slave's address, so that all the slaves will generate the receive interrupt; the slave's software uses their own address and the If they agree, the addressed slave sets SM2x=0, and then the host sets bit 9 to 0 when it continues to transmit the next data, because the other slaves still have SM2x set to 1, so that only the addressed slave generates a receive interrupt.

- **Fast baud rate setting**

In the UART of the standard 51 microcontroller, the baud rate of UART is fixed at 32 divisions of the timer overflow rate. Due to the CPU clock of the CA51F155 series MCU being 12MHz (or 12MHz division), the configured baud rate has a significant error compared to the standard baud rate. Therefore, in the CA51F155 series MCU, a mechanism for correcting baud rate is designed, and the baud rate of UART is not fixed at 32 divisions of the timer overflow rate, but can be set by the register UDCKS. For example, when the baud rate of UART is fixed at 32 times the overflow rate of the timer, timer 2 is selected as the baud rate generator of UART. To configure the baud rate to 115200, the calculation formula is: 1200000 ÷ 32 ÷ 115200=3.26. Since the timer count can only take integers, it is taken as 3 (i.e. every 3 system clock cycles, the timer overflows), with an error rate of about 8.5%. If the error rate is too high, it can lead to abnormal communication. Due to the fixed system clock, achieving a more accurate baud rate can only be achieved by modifying the division coefficient. If the timer is set to overflow for 13 clock cycles, then: 12000000 ÷ 115200 ÷ 13=8.01. If the division frequency is 8, then the baud rate is 115385. Compared with 115200, the error rate is about 0 16%, generally not affecting UART communication. In addition, smaller division frequencies can also achieve higher baud rate configurations.

The default frequency division coefficient of the chip is 32, which is the same as the standard 51. If you want to change the division coefficient, enable it by setting UDEx=1. The value of DNUM represents different division coefficients, as described in register UDCKSx.

16.2 UART0/1/2 Register Description

Table 16-2-1 Register S0CON

98H	7	6	5	4	3	2	1	0
S0CON	SM0	U0IE	SM20	REN0	TB80	RB80	TI0	RI0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	SM0	UART0 mode selection , for more information please refer to Table 16-1-1
6	U0IE	UART0 interrupt enable , 1 valid

5	SM20	Multi-computer communication enable control, 1 enables
4	REN0	Serial receive enable control, 1 enables
3	TB80	The 9th data bit to transmit In mode A, this bit is used for UART0 to transmit data and corresponds to bit 9 of the transmitted data (e.g. parity or multi-host communication), controlled by software
2	RB80	The 9th bit of the data received In mode A, this bit is used for UART0 to receive data, corresponding to bit 9 of the received data In mode B, this bit is the received stop bit
1	TI0	Transmit interrupt flag bit, 1 valid, write 1 to clear 0
0	RI0	Receive interrupt flag bit, 1 valid, write 1 to clear 0

Table 16-2-2 Register S0BUF

99H	7	6	5	4	3	2	1	0
S0BUF	S0BUF[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~0	S0BUF	UART0 transceiver buffer Writing S0BUF will start sending the written data Reading S0BUF will result in the received data

Table 16-2-3 Register UDCKS0

D8H	7	6	5	4	3	2	1	0
UDCKS0	UDE	-	-	DNUM[4:0]				
R/W	R/W	-	-	R/W				
Initial Value	0	-	-	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	UDE	Fast baud rate configuration enable control bit, 1 valid Note: When UDE=0, the UART0 baud rate is configured according to the original configuration, and when UDE=1, the UART0 baud rate is configured by DNUM.
6~5	-	-
4~0	DNUM	Fast baud rate configuration register, only valid when UDE=1 When sending, DNUM>=0 must be met; When receiving, DNUM>=6 BR=Fsys * (1/(DNUM+1) * (1024-S0REL))

Table 16-2-4 Register S0RELL、S0RELH

D9H	7	6	5	4	3	2	1	0
S0RELL	S0RELL[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
DAH	7	6	5	4	3	2	1	0
S0RELH	-	-	-	-	-	-	S0REL[9:8]	
R/W	-	-	-	-	-	-	R/W	
Initial Value	-	-	-	-	-	-	0	0

Bit Number	Bit Symbol	Description
9~0	S0REL	Baud rate configuration register Baud rate is CPUCLK/(32 * (1024 – S0REL))

Table 16-2-5 Register S1CON

B1H	7	6	5	4	3	2	1	0
S1CON	SM1	U1IE	SM21	REN1	TB81	RB81	TI1	RI1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	SM1	UART1 mode selection , for more information please refer to Table 16-1-1
6	U1IE	UART1 interrupt enable , 1 valid
5	SM21	Multi-computer communication enable control, 1 enables
4	REN1	Serial receive enable control, 1 enables
3	TB81	The 9th data bit to transmit In mode A, this bit is used for UART1 to transmit data and corresponds to bit 9 of the transmitted data (e.g. parity or multi-host communication), controlled by software
2	RB81	The 9th bit of the data received In mode A, this bit is used for UART1 to receive data, corresponding to bit 9 of the received data In mode B, this bit is the received stop bit
1	TI1	Transmit interrupt flag bit, 1 valid, write 1 to clear 0
0	RI1	Receive interrupt flag bit, 1 valid, write 1 to clear 0

Table 16-2-6 Register S1BUF

B2H	7	6	5	4	3	2	1	0
S1BUF	S1BUF[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~0	S1BUF	Receiver/Transmitter buffer Writing data to S1BUF will starts the data transmission Reading S1BUF will reads the data received

Table 16-2-7 Register UDCKS1

B5H	7	6	5	4	3	2	1	0
UDCKS1	UDE	-	-	DNUM[4:0]				
R/W	R/W	-	-	R/W				
Initial Value	0	-	-	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	UDE	Fast baud rate configuration enable control bit, 1 valid Note: When UDE=0, the UART1 baud rate is configured according to the original configuration, and when UDE=1, the UART1 baud rate is configured by DNUM.
6~5	-	-
4~0	DNUM	Fast baud rate configuration register, only valid when UDE=1 When sending, DNUM>=0 must be met; When receiving, DNUM>=6 BR=Fsys * (1/(DNUM+1) * (1024-S1REL))

Table 16-2-8 Register S1RELL、S1RELH

B3H	7	6	5	4	3	2	1	0
S1RELL	S1RELL[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
B4H	7	6	5	4	3	2	1	0
S1RELH	-	-	-	-	-	-	S1REL[9:8]	
R/W	-	-	-	-	-	-	R/W	
Initial Value	-	-	-	-	-	-	0	0

Bit Number	Bit Symbol	Description
9~0	S1REL	Baud rate configuration register Baud rate is CPUCLK/(32 * (1024 - S1REL))

Table 16-2-9 Register S2CON

B9H	7	6	5	4	3	2	1	0
S2CON	SM2	U2IE	SM22	REN2	TB82	RB82	TI2	RI2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	SM2	UART2 mode selection bits, see Table 16-1-1 for details
6	U2IE	Serial port 2 interrupt enable bit, 1 valid
5	SM22	Multi-computer communication enable bit, 1 valid
4	REN2	Serial receive enable bit, 1 valid
3	TB82	The ninth bit of the sent data In mode A, this bit is used for data transmission on serial port 1 and corresponds to bit 9 of the transmitted data (e.g. parity or multi-host communication), controlled by software
2	RB82	The ninth bit of the received data In mode A, this bit is used for UART2 to receive data and corresponds to bit 9 of the received data In mode B, this bit is the received stop bit
1	TI2	Transmit interrupt flag bit, 1 valid, write 1 to clear 0
0	RI2	Receive interrupt flag, 1 valid, write 1 to clear 0

Table 16-2-10 Register S2BUF

BAH	7	6	5	4	3	2	1	0
S0BUF	S0BUF[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~0	S0BUF	Transceiver buffer Write S2BUF will start sending the written data Reading S2BUF will get the data already received

表 16-2-11 寄存器 UDCKS2

BDH	7	6	5	4	3	2	1	0
UDCKS2	UDE	-	-	DNUM[4:0]				
R/W	R/W	-	-	R/W				
Initial Value	0	-	-	0	0	0	0	0

Bit Number	Bit Symbol	Description

7	UDE	Fast baud rate configuration enable control bit, 1 valid *Note:* *When UDE=0, the UART2 baud rate is configured as original, UDE=1, the UART2 baud rate is configured by DNUM.*
6~5	-	-
4~0	DNUM	Fast baud rate configuration register, valid only when UDE=1 When sending, DNUM >=0; when receiving, DNUM>=6 BR = F_{sys}/(((DNUM+1)*(1024-S2REL))

Table 16-2-12 Register S2RELL、S2RELH

BBH	7	6	5	4	3	2	1	0
S2RELL	S2RELL[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
BCH	7	6	5	4	3	2	1	0
S2RELH	-	-	-	-	-	-	S2REL[9:8]	
R/W	-	-	-	-	-	-	R/W	
Initial Value	-	-	-	-	-	-	0	0

Bit Number	Bit Symbol	Description
9~0	S2REL	Baud rate configuration register Baud rate is CPUCLK/(32 * (1024 – S2REL))

17 I²C Interface

17.1 Function Introduction

I2C modules enables the chip to communicate with peripheral I2C devices by serial transmission standard which complies with standard I2C specification. It can be set to either slave or master and configured to standard/fast/high speed mode.

The I2C pin SCL/SDA can be mapped to any GPIO pin, as detailed in the "15-2-9 Pin Multiplexing Function Mapping Table".

17.2 I²C Main Features

- Simple but strong communication port, bi-directional bus with 2 wires
- Slave/Master mode configurable
- Able to operate in receiver/transmitter mode
- 7 bit slave address
- Supports multimaster's arbitration
- Broadcast function supported
- Support SCL/SDA mapping to any GPIO

17.3 I²C Function Description

I2C modules supports I2C standard bus specification. I2C bus includes 2 wires to transfer data among devices, one is SCL(Serial Clock) and the other is SDA(Serial Data), as Figure 17-3-1 shows. Since the it is open-drain port for I2C, there must be pull-up resistor on I2C bus. The pull-up resistor can be connected externally or enabled internally. Each device that connects to the bus has its own 7-bit address.

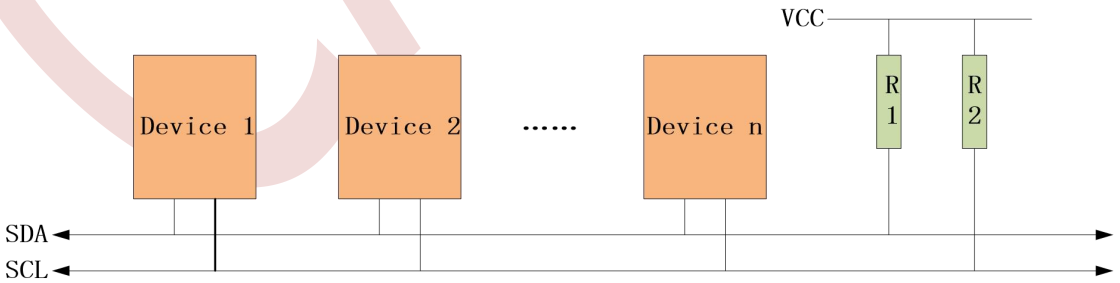


Figure 17-3-1 I2C Bus Interconnection Diagram

I2C module principle is as Figure 17-3-2 shows.

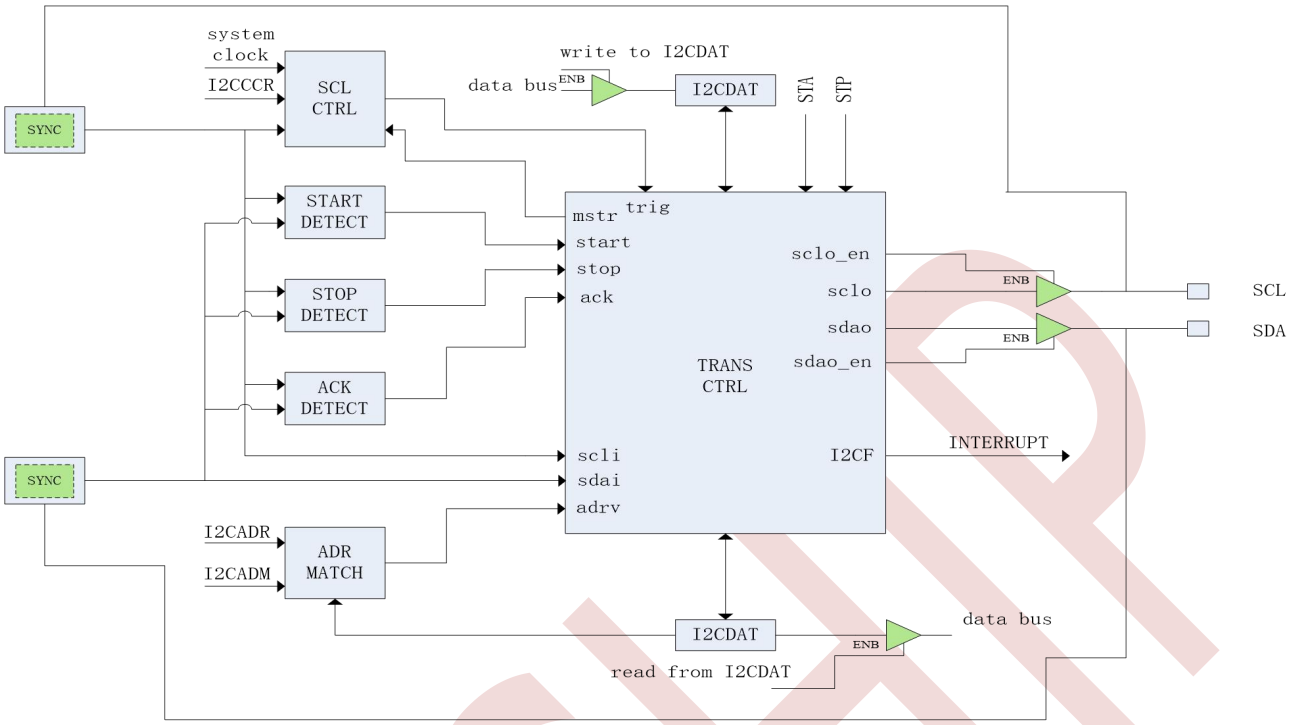


Figure 17-3-2 I²C Schematic diagram of the module princip

- **I²C Mode Selection**

I2C can operate in one of the following four modes: slave transmit mode, slave receive mode, host transmit mode, and host receive mode. By default, I2C is in slave mode. I2C automatically switches from slave mode to host mode when a start signal is generated, and then automatically switches back to slave mode when arbitration fails or a STOP signal is generated.

- **I2C Bus Data Transmission Pattern**

In general, the standard I2C communication consists of four parts: start signal, slave address transmission, data transmission and end signal. 8 bits of data are transmitted on the I2C bus, high bit first, each byte sent must be followed by an answer bit, there is no limit to the number of data bytes per communication; at the end of all data transmission, the host sends a stop signal to end the communication.

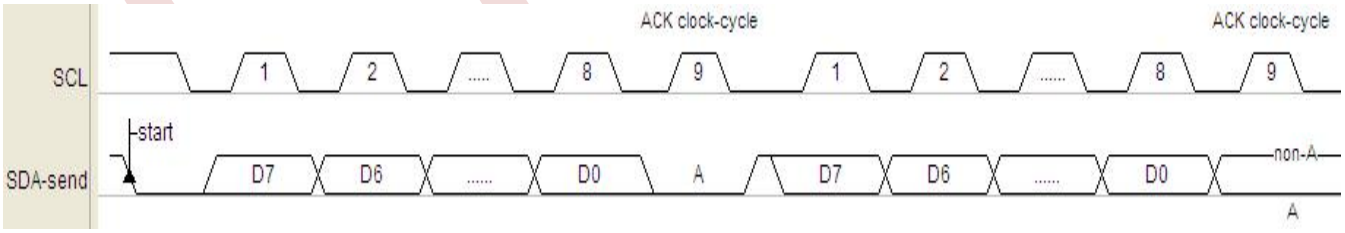


Figure 17-3-3 I2C Bus Data Transfer Format

- **Communication Process**

In host mode, the I2C interface initiates the data transfer and generates the clock signal. The serial data transfer always starts with the START signal and ends with the STOP signal. both the START signal and the STOP signal are generated in host mode by software control, the START signal is generated by setting STA=1

and the STOP signal is generated by setting STP=1.

In slave mode, the I2C interface can recognize its own address (7-bit address) and the broadcast address. The software can enable or disable the recognition of the broadcast address via the GCE bit.

Address and data are transmitted in bytes, and the address is sent by the host after the START signal. In the 9th clock cycle after 8 clocks of a byte transmission, the receiver must send back an answer bit to the transmitter. The answer bit is set via the AAK bit. Setting the answer bit must be set before a byte is finished transmitting, and the answer signal is automatically generated when the receiver finishes receiving a byte. During data transmission, events such as data sending/receiving finished one byte, arbitration failure will generate interrupt flag I2CF, and the status of the event is indicated by register I2CSTA (please refer to register I2CSTA introduction for details), the software should set the next operation of data transmission according to the status of the event after generating interrupt flag, clearing interrupt flag I2CF will start the next operation. After the communication ends the host generates the STOP signal will also generate the interrupt flag I2CSTP at the slave side to indicate the completion of the communication process. When the interrupt flag I2CF is generated, if SHD=1, SCL will be pulled low by the slave before clearing I2CF, and the host will detect that SCL is released before the next operation; if SHD=0, the slave will not pull low SCL, which is designed to be compatible with the application that the host is software emulating I2C, at this time, the host's software must wait long enough for the slave to respond to each byte of data transfer is processed.

When the I2C interface serves as a slave, the SCL clock is input by the master and is independent of the slave's clock configuration. As a slave, it is necessary to ensure that the width of SCL at low levels is at least 6.5 system clocks, while at high levels it is at least 2.5 system clocks. So, the SCL frequency sent by the external host is up to 1/9 of the system clock frequency.

17.4 I²C Communication Pin Mapping

For the convenience of hardware design, I2C communication pins can have different mappings, as described in the "15-2-9 Pin Multiplexing Function Mapping Table" for details.

17.5 Register Description

Table 17-5-1 Register I2CCON

C0H	7	6	5	4	3	2	1	0
I2CCON	I2CE	I2CIE	STA	STP	SHD	AAK	CBSE	STFE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	1	0	0	0	0	1	0	0

Bit Number	Bit Symbol	Description
7	I2CE	I2C module enable control, 1 enables it
6	I2CIE	I2C interrupt enable control, 1 enables it1
5	STA	I2C START signal transfer control,valid when it is 1, it will be cleared automatically when START signal detected
4	STP	I2C STOP signal transfer control, valid when it is 1, it will be cleared automatically when STOP

		signal detected
3	SHD	When it is 1, if I2CF=1, I2CF will make SCL remain low after SCL becomes low
2	AAK	I2C ACK signal transfer control, 1 enables it Note : When I2C is configured as slave, this bit must be set to 1 beforehand, otherwise even the address matches it will not reply ACK
1	CBSE	CBUS compatible enable control When it is set to 1, the ACK will be ignored during the transmission to be compatible with CBUS bus. Since the address for CBUS bus is 7 bits, thus GCE must be set to 0.
0	STFE	When STFE=1, I2CF will be set to 1 if I2C module detects the START signal

Table 17-5-2 Register I2CADR

C1H	7	6	5	4	3	2	1	0
I2CADR	GCE	I2CADRL[6:0]						
R/W	R/W	R/W						
Initial Value	1	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	GCE	Broadcast address recognition(00H)enable control, 1 enables it
6~0	I2CADRL	I2C slave address, only valid when it operates as slave Note： (when AAK=1) when the address is 7 bits and the higher 7 bits of first received address matches I2CADR, reply with ACK and enters slave mode

Table 17-5-3 Register I2CADM

C2H	7	6	5	4	3	2	1	0
I2CADM	SPFE	I2CADML[6:0]						
R/W	R/W	R/W						
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	SPFE	When SPFE=1, I2CF will be set to 1 if I2C module detects the STOP signal
6~0	I2CADML	I2C address mask by bit control, valid only when it operates as slave When I2CADM[n](n=0~6)=1, the corresponding address bit I2CADR[n] will not be compared (which means no matter what is received, it is seen as matched)

Table 17-5-4 Register I2CCCR

C3H	7	6	5	4	3	2	1	0
I2CCCR	I2CCCR[7:0]							
R/W	R/W							
Initial Value	0	0	1	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~0	I2CCCR	I2C clock configuration register The sampling frequency is the division of the $2^{I2CCCR\ [7:5]}$ of the I2C working clock, when I2CCCR [7:5] is equal to 000:$F_{sample}=F_{i2cclk}$ 001:$F_{sample}=F_{i2cclk}/2$ 010:$F_{sample}=F_{i2cclk}/4$ ... 111:$F_{sample}=F_{i2cclk}/128$ (I2CCCR [4:0]+1) division with an output frequency of sampling frequency, $F_{scl}=F_{i2cclk}/(2^{I2CCCR}$ [7:5] * (I2CCCR [4:0]+1)) For example, when I2CCR [4:0]=9, when I2CCR [7:5] is equal to 000: $F_{scl}=F_{i2cclk}/(1*10)$ 001: $F_{scl}=F_{i2cclk}/(2*10)$ 010: $F_{scl}=F_{i2cclk}/(4*10)$ ... 111: $F_{scl}=F_{i2cclk}/(128*10)$ Note: When I2CCCR [7:5]=0, if a value less than 9 is written to I2CCCR [4:0], it will be automatically calculated based on the value of 9. When I2CCCR [7:5]>0, if a value less than 7 is written to I2CCCR [4:0], it will be automatically calculated based on the value of 7.

Table 17-5-5 Register I2CDAT

C4H	7	6	5	4	3	2	1	0
I2CDAT	I2CDAT[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~0	I2CDAT	Data buffer for receiving/transmission *Note：* *When I2CF is 1, it is recommended to make I2CF remain 1 when users overwrite/read I2CDAT. I2CF should be cleared after the process is over, and then the transmission continues so that there will be no transmission errors*

Table 17-5-6 Register I2CSTA

C5H	7	6	5	4	3	2	1	0
I2CSTA	I2CSTA[7:0]							
R/W	R							
Initial Value	1	1	1	1	1	0	0	0

Bit Number	Bit Symbol	Description
7~0	I2CSTA	I2C status register 00H: (master/slave) bus error 08H: (master/slave)START signal detected (valid only when STFE=1) 18H: (master)address and write bit sent, ACK signal received 20H: (master)address and write bit sent, no ACK signal received 28H: (master)one byte data received/transmitted, ACK signal detected 30H: (master)one byte data received/transmitted, no ACK signal detected 38H: (master)arbitration lost(master will change to slave after arbitration lost) 40H: (master)address and read bit transmitted, ACK signal received 48H: (master)address and read bit transmitted, no ACK signal received 60H: (slave)address and write bit received, with ACK signal is sent 70H: (master/slave)broadcast address received with ACK signal is sent(master/slave will become slave) 80H: (slave)one byte data received/transmitted, ACK signal detected 88H: (slave)one byte data received/transmitted, no ACK signal detected A0H: (master/slave)STOP signal detected(valid only when SPFE=1) A8H: (slave)address and read bit received, with ACK signal is sent F8H: (master/slave) bus is idle

Table 17-5-7 Register I2CFLG

C6H	7	6	5	4	3	2	1	0
I2CFLG	-	-	-	-	-	-	-	I2CF
R/W	-	-	-	-	-	-	-	R
Initial Value	-	-	-	-	-	-	-	0

Bit Number	Bit Symbol	Description
7~1	-	-
0	I2CF	I2C interrupt flag, 1 indicates the interrupt, cleared by writing 1 to it Note： 1. I2CF will be set to 1 every time after a one-byte data or the address transmission completes (with ACK/NAK received/sent) 2. I2CF will be set to 1 when there is bus error 3. If STFE=0, I2CF will not be set to 1 when START signal detected

		4. If SPFE=0, I2CF will not be set to 1 when STOP signal detected

Table 17-5-8 Register I2CCKS

D7H	7	6	5	4	3	2	1	0
I2CCKS	I2CKS	-	-	-	-	-	-	-
R/W	R/W	-	-	-	-	-	-	-
Initial Value	0	-	-	-	-	-	-	-

Bit Number	Bit Symbol	Description
7	I2CKS	I2C working clock selection bit 0: System clock 1: Internal high-speed clock
6~0	-	-

18 PWM

18.1 PWM Function Introduction

The CA51F155 series chip supports up to 6 PWM outputs, each of which can be individually controlled. The cycle and duty cycle can be configured arbitrarily within a 16 bit range.

Supports complementary mode and dead zone mode, supports setting edge alignment and center alignment modes, supports direct output of internal clock function, supports PWM interrupt function, and can select different pins as PWM output pins for each PWM channel. Please refer to the "15-2-9 Pin Reuse Function Mapping Table" for details.

18.2 PWM Function Description

Each PWM channel has a dedicated 16 bit counter, and the PWM cycle is set through register PWMDIV, while register PWMDUT corresponds to the PWM duty cycle. PWM is enabled through register PWMEN, and each bit of register PWMEN corresponds to a channel of PWM. The PWM module has a PWM data update register PWMUPD. When rewriting registers PWMDIV, PWMDUT, and PWMCKD, register PWMUPD must be set to the corresponding bit to update the data. After the data is refreshed, the corresponding bit of PWMUPD automatically clears to 0. PWM can set the PWM pin output to invert through the PWMTOG bit. PWM has multiple clock sources to choose from, which are set in two PWM units: PWM0 and PWM1, PWM2 and PWM3, PWM4 and PWM5. That is to say, the clock sources for each set of PWM are set together, and the clock sources are selected through the PWMCKS of the control register PWMCON corresponding to PWM0, PWM2, and PWM4. In addition, the clock division of each PWM can be independently set through PWMCKD.

- **Edge alignment mode and center alignment mode**

The edge alignment mode and center alignment mode of PWM are selected through the PWMMS bit. After PWM is enabled, the PWM counter starts counting from 0. When the count value is less than PWMDUT, the PWM pin outputs a high level (PWMTOG=0). When the count value is greater than or equal to PWMDUT, the PWM pin outputs a low level (PWMTOG=0). In edge alignment mode, when the count value is equal to PWMDIV, one PWM cycle is completed, the PWM counter is reset to 0, and the next cycle count begins. In center alignment mode, when the count value reaches the PWMDIV value, the counting direction is reversed and the counting begins to decrease. During this stage, when the count value is also less than PWMDUT, the PWM pin outputs a high level (PWMTOG=0), and when the count value is greater than or equal to PWMDUT, the PWM pin outputs a low level (PWMTOG=0); When the count decreases to 0, one PWM cycle is completed, and the count starts again to accumulate for the next cycle.

When the edge alignment mode and center alignment mode are used, the single PWM output waveforms are shown in Figures 18-2-1 and 18-2-2 (note: all PWM waveforms below meet the condition PWMDIV>PWMDUT>0). As shown in the figure, setting the same PWMDIV and PWMDUT values, the center alignment mode has one PWM cycle that is twice as long as the edge alignment mode.

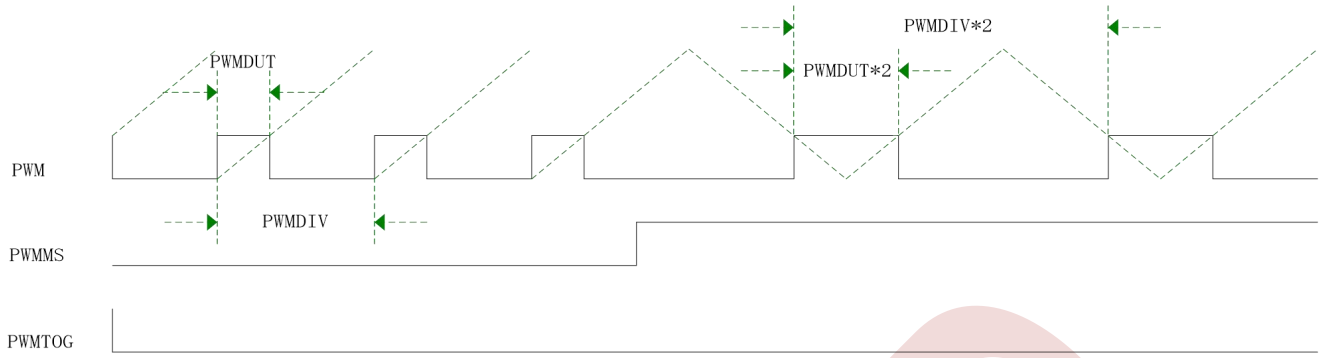


Figure 18-2-1 PWM output waveform when PWMTOG=0

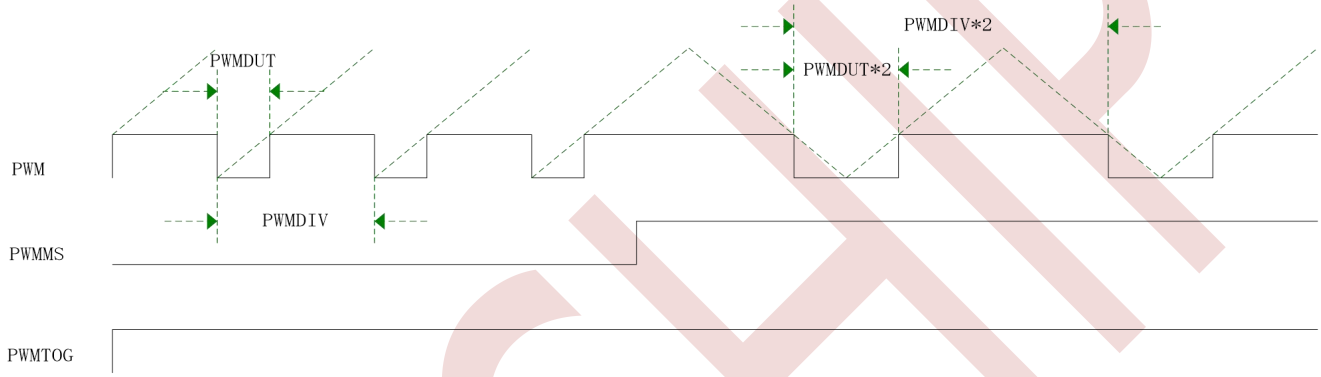


Figure 18-2-2 PWM output waveform when PWMTOG=1

It is worth noting that when PWMDIV=0, the PWM pin directly outputs a PWM clock. If PWMCKD=0, the PWM pin outputs the clock signal of the selected clock source; When PWMDIV is not 0 and PWMDUT is 0, the PWM pin outputs a low level (PWMTOG=0); When PWMDUT>=PWMDIV>0, the PWM pin outputs a high level (PWMTOG=0).平（PWMTOG=0）

- **Complementary mode**

In complementary mode, 6 PWM channels can form 3 pairs of complementary channels: PWM0 and PWM1, PWM2 and PWM3, PWM4 and PWM5. The complementary mode of PWM is set through the PWMMOD bit of the control registers PWMCON of PWM1, PWM3, and PWM5. In complementary mode, PWM alignment, cycle, duty cycle, and pre division clock are all set by the registers corresponding to PWM0, PWM2, and PWM4, while only PWMTOG is still independently controlled by the corresponding registers of each channel. The schematic diagram of PWM complementary mode is shown in Figure 18-2-3.

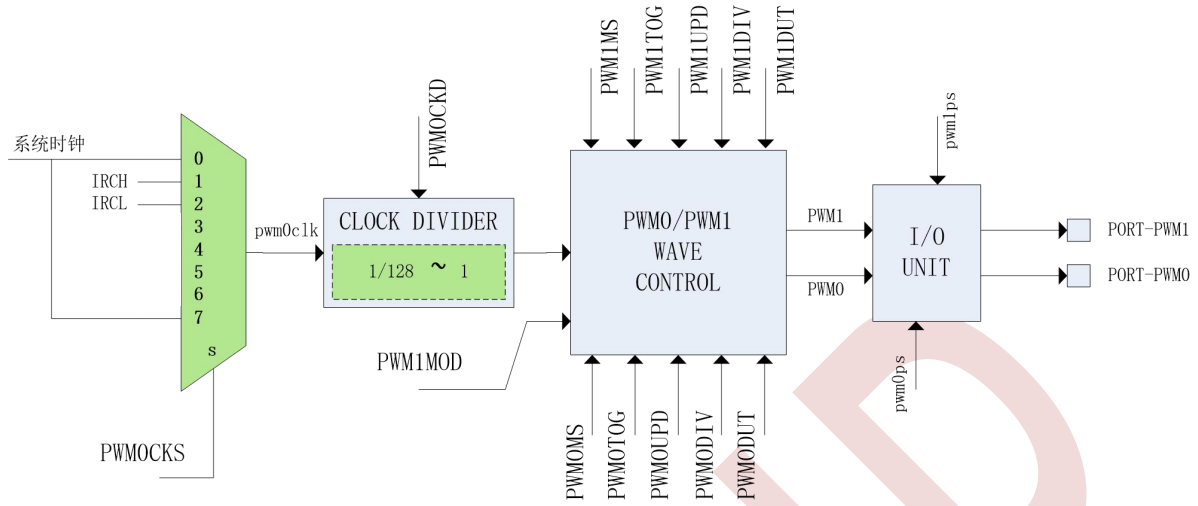


Figure 18-2-3 Schematic diagram of PWM0 and PWM1 principles

The waveforms output by each group of PWM are complementary in phase, as shown in Figures 18-2-4 and 18-2-5 (using PWM0 and PWM1 as examples).

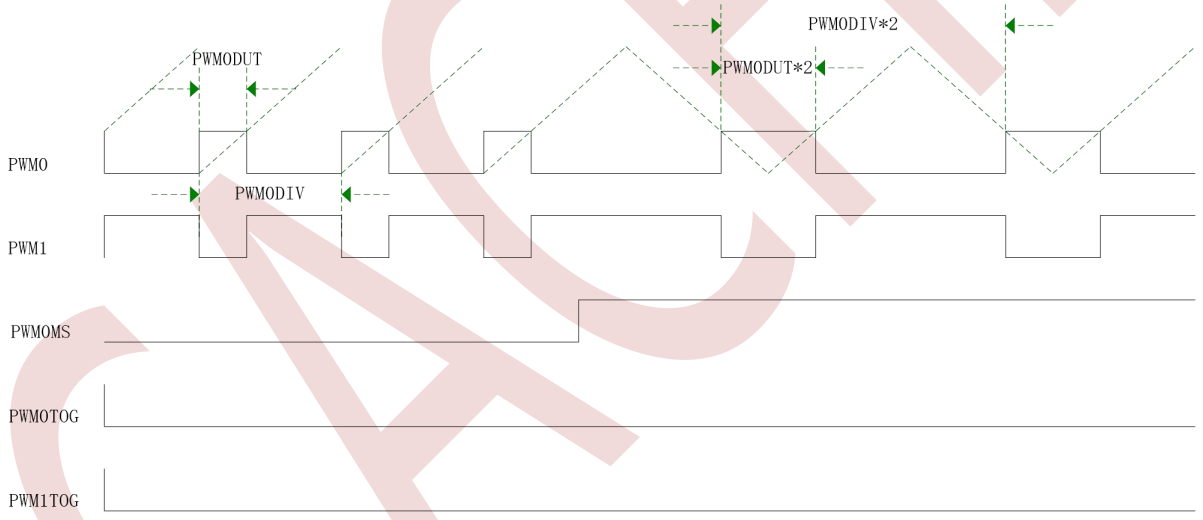


Figure 18-2-4: When PWMTOG=0, PWM0 and PWM1 output complementary waveforms

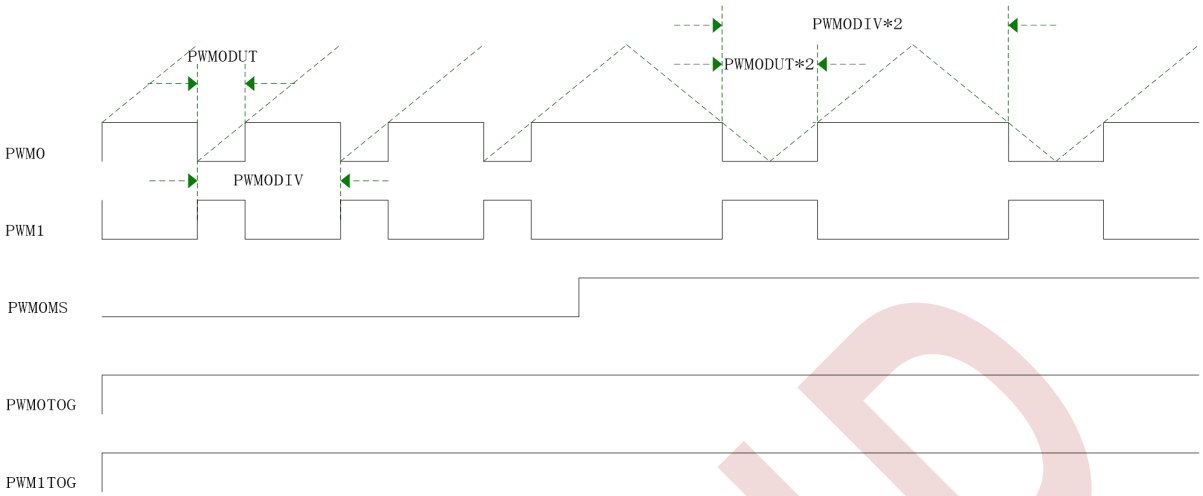


Figure 18-2-5: When PWMTOG=1, PWM0 and PWM1 output complementary waveforms

Dead zone control

In the bridge drive circuit, to prevent the upper and lower half bridges from conducting simultaneously, it is necessary to insert a dead zone control in the PWM complementary signal. The dead time is set by the registers PWMDIV and PWMDUT corresponding to PWM1, PWM3, and PWM5. PWMDIV sets the left dead time, while PWMDUT sets the right dead time. The dead time setting needs to meet the following conditions (using PWM0 and PWM1 as examples):

In edge alignment mode, PWMDIV1<PWMDUT0 and PWMDUT1<(PWMDIV0- PWMDUT0);

In center alignment mode, PWMDIV1<(PWMDIV0- PWMDUT0) x 2 or PWMDUT1<(PWMDIV0- PWMDUT0) x 2.

The output waveform of dead zone control is shown in Figure 18-2-6 (taking PWM0 and PWM1 as examples).

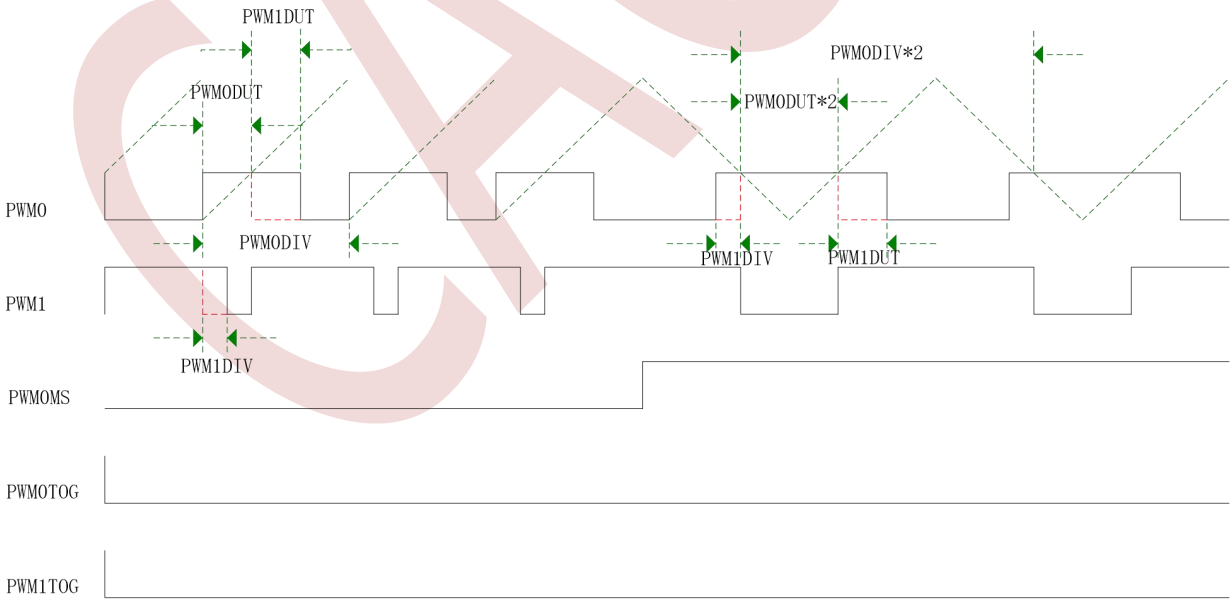


Figure 18-2-6 Deadband control waveforms of PWM0 and PWM1 when PWMTOG=0

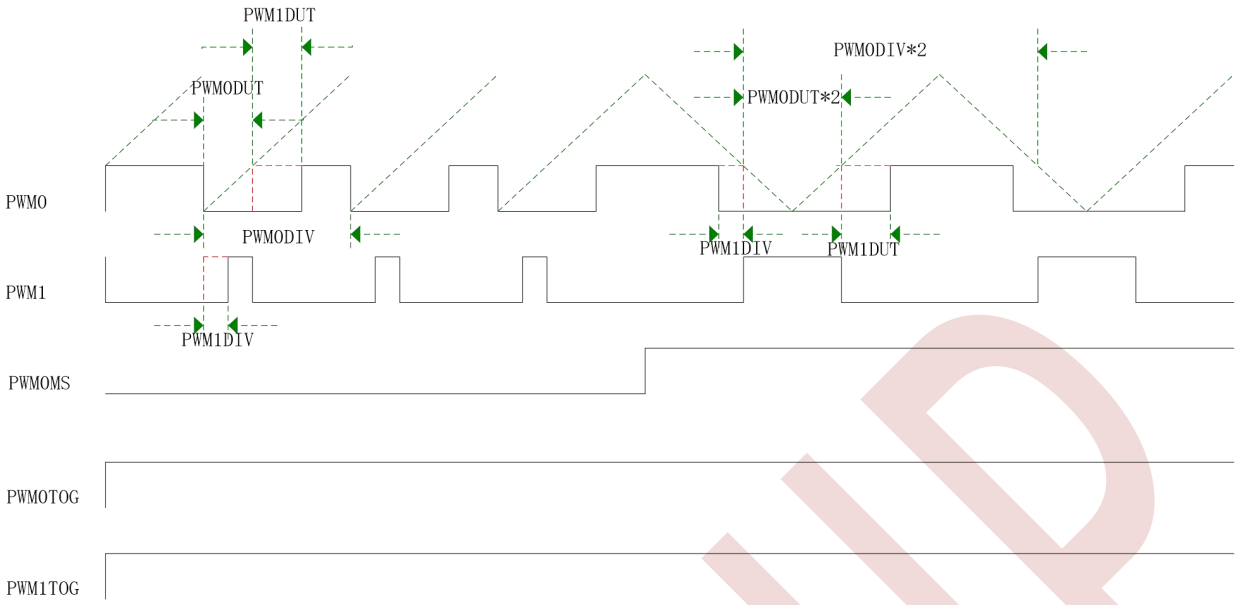


Figure 18-1-6 Deadband Control Waveform of PWM0 and PWM1 at PWMTOG=1

- PWM interrupt

PWM interrupts are enabled through the PWMTIE, PWMZIE, and PWMPIE bits of the PWMCON register. The PWMTIE bit corresponds to the interrupt generated when the PWM counter counts to the vertex (i.e. equal to PWMDIV), the PWMZIE bit corresponds to the interrupt generated when the PWM counter counts to the lowest point (i.e. equal to 0), and the PWMPIE bit corresponds to the interrupt generated when the output pin rises. Among them, in edge alignment mode, there are no interrupts corresponding to PWMTIE and PWMZIE bits. Registers PWMAIF, PWMBIF, PWMCIF, and PWMDIF are interrupt status registers for six channels, where PWMxTIF, PWMxZIF, and PWMxPIF correspond to enable bits PWMTIE, PWMZIE, and PWMPIE, respectively.

In addition, PWM can set the number of interrupt events that occur before generating an interrupt through the register PWMCMX. For example, if PWMCMX=3 and PWMPIE=1 are set, the PWM pin will only generate a rising edge interrupt after 4 rising edges.

Note: PWM falling edge interrupt is not supported.

18.3 PWM Register Description

Table 18-3-1 Register PWMEN

91H	7	6	5	4	3	2	1	0
PWMEN	-	-	-	-	PWMEN[3:0]			
R/W	-	-	-	-	R/W			
Initial Value	-	-	-	-	0	0	0	0

Bit Number	Bit Symbol	Description
7~4	-	-
3~0	PWMEN	3~0 bit correspond to PWM channel 3~0's enable control, 1 enables it

Table 18-3-2 Registers PWMUPD

92H	7	6	5	4	3	2	1	0
PWMUPD	-	-	PWMUPD[5:0]					
R/W	-	-	R/W					
Initial Value	-	-	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~0	PWMUPD	5~0 bits correspond to PWM channel 5~0 data update enable control bit, 1 is valid Remarks: After configuring the data for a certain channel (PWMDIV/PWMDUT/PWMCKD), position 1 of the corresponding channel for PWMUPD is set so that the data is updated after the PWM counter overflows, and the corresponding bit will automatically clear 0 after the data update is completed.

Table 18-3-3 Registers PWMCMAX

93H	7	6	5	4	3	2	1	0
PWMCMAX	PWMCMAX[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0

Note: PWMCMX is an indexed register, set INDEX=0~5 to correspond to PWMCMAX0~PWMCMAX5 respectively

Bit Number	Bit Symbol	Description
7~0	PWMCMAX	Register for setting the number of effective intervals for PWM channel interrupts. Interval count=PWMCMAX+1, for example, if INDEX=0 and PWMCMAX=7 are set, then all interrupts in PWM0 will generate 8 interrupt events before setting the interrupt flag.

Table 18-3-4 Register PWMCON

94H	7	6	5	4	3	2	1	0
PWMCON①	PWMTIE	PWMZIE	PWMPIE	-	PWMMS	PWMCKS[2:0]		
R/W	R/W	R/W	R/W	-	R/W	R/W		
Initial Value	0	0	0	-	0	0	0	0
PWMCON②	PWMTIE	PWMZIE	PWMPIE	-	PWMMS	-	-	PWMMOD
R/W	R/W	R/W	R/W	-	R/W	-	-	R/W
Initial Value	0	0	0	-	0	-	-	0

Bit Number	Bit Symbol	Description
Remarks:		

1. PWMCON is the control register for PWM0/PWM2/PWM4 channels; *PWMCON is the control register for PWM1/PWM3/PWM5 channels.* *2. PWMCON is an indexed register, with INDEX=0~5 corresponding to PWMCON0~5, respectively*		
7	PWMTIE	PWM counter vertex interrupt enable control bit, 1 valid
6	PWMZIE	PWM counter lowest point interrupt enable control bit, 1 valid
5	PWMPIE	PWM rising edge interrupt enable control bit, 1 effective
4	-	-
3	PWMMS	PWM mode selection bit 0: Edge alignment mode 1: Center alignment mode
PWMCON①[2~0]	PWMCKS	PWM working clock selection bit 001: IRCH 010: IRCL When INDEX=0/1, select TKRC; When INDEX is a different value, select the system clock. Other: System clock *Remarks:* *PWM0/PWM1, both configured by PWMCKS0;* *PWM2/PWM3 are configured by PWMCKS2;* *PWM4/PWM5 are both configured by PWMCKS4.*
PWMCON②[0]	PWMMOD	Complementary mode enable register, 1 valid *Remarks:* *Set PWMMOD1=1, and PWM0 and PWM1 enter complementary mode;* *Set PWMMOD3=1, and PWM2 and PWM3 enter complementary mode;* *Set PWMMOD5=1, and PWM4 and PWM5 enter complementary mode.*

Table 18-3-5 Registers PWMCFG

95H	7	6	5	4	3	2	1	0
PWMCFG	PWMTOG	PWMCKD[6:0]						
R/W	R/W	R/W						
Initial Value	0	0	0	0	0	0	0	0
Note: PWMCFG is an indexed register, set INDEX=0~5 to correspond to PWMCFG0~PWMCFG5 respectively								
Bit Number	Bit Symbol	Description						
7	PWMTOG	PWM output reverse enable register, 1 valid						
6~0	PWMCKD	PWM working clock pre division configuration register 000000: No frequency division 000000 1:2 frequency division 00000 10:3 division frequency ..... 1111110:127 frequency division 1111111:128 frequency division						

Table 18-3-6 Registers PWMDIVL, PWMDIVH

96H	7	6	5	4	3	2	1	0
PWMDIVL	PWMDIV[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
97H	7	6	5	4	3	2	1	0
PWMDIVH	PWMDIV[15:8]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
Note: PWMDIV is an indexed register, set INDEX=0~5 to correspond to PWMDIV0~PWMDIV5 respectively								

Bit Number	Bit Symbol	Description
15~0	PWMDIV	PWM cycle configuration register *Remarks:* *In complementary mode, PWMDIV1/PWMDIV3/PWMDIV5 has different meanings, refer to the description of registers PWMDUT*

Table 18-3-7 Registers PWMDUTL, PWMDUTH

9BH	7	6	5	4	3	2	1	0
PWMDUTL	PWMDUT[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
9AH	7	6	5	4	3	2	1	0
PWMDUTH	PWMDUT[15:8]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
Note: PWMDUT is an indexed register, set INDEX=0~5 to correspond to PWMDUT0~PWMDUT5 respectively								

Bit Number	Bit Symbol	Description
15~0	PWMDUT	PWM duty cycle configuration register In complementary mode, PWMDUT1/PWMDUT3/PWMDUT5 has different meanings, as shown in the table below:

PWMDIV1	Control the width of the dead zone on the left side of PWM0/PWM1
PWMDUT1	Control the width of the dead zone on the right side of PWM0/PWM1
PWMDIV3	Control the width of the dead zone on the left side of PWM2/PWM3
PWMDUT3	Control the width of the dead zone on the right side of PWM2/PWM3

		PWMDIV5 — Control the width of the dead zone on the left side of PWM4/PWM5 PWMDUT5 — Control the width of the dead zone on the right side of PWM4/PWM5

Table 18-3-8 Registers PWMAIF

9CH	7	6	5	4	3	2	1	0
PWMAIF	PWM1TIF	PWM1ZIF	PWM1PIF	-	PWM0TIF	PWM0ZIF	PWM0PIF	-
R/W	R	R	R	-	R	R	R	-
Initial Value	0	0	0	-	0	0	0	-

Bit Number	Bit Symbol	Description
7	PWM1TIF	PWM1 counter vertex interrupt flag, write 1 clear 0
6	PWM1ZIF	PWM1 counter lowest point interrupt flag, write 1 clear 0
5	PWM1PIF	PWM1 rising edge interrupt flag, write 1 clear 0
4	-	-
3	PWM0TIF	PWM0 counter vertex interrupt flag, write 1 clear 0
2	PWM0ZIF	PWM0 counter lowest point interrupt flag, write 1 clear 0
1	PWM0PIF	PWM0 rising edge interrupt flag, write 1 clear 0
0	-	-

Table 18-3-9 Registers PWMBIF

9DH	7	6	5	4	3	2	1	0
PWMBIF	PWM3TIF	PWM3ZIF	PWM3PIF	-	PWM2TIF	PWM2ZIF	PWM2PIF	-
R/W	R	R	R	-	R	R	R	-
Initial Value	0	0	0	-	0	0	0	-

Bit Number	Bit Symbol	Description
7	PWM3TIF	PWM3 counter vertex interrupt flag, write 1 clear 0
6	PWM3ZIF	PWM3 counter lowest point interrupt flag, write 1 clear 0
5	PWM3PIF	PWM3 rising edge interrupt flag, write 1 clear 0
4	-	-
3	PWM2TIF	PWM2 counter vertex interrupt flag, write 1 clear 0
2	PWM2ZIF	PWM2 counter lowest point interrupt flag, write 1 clear 0
1	PWM2PIF	PWM2 rising edge interrupt flag, write 1 clear 0
0	-	-

Table 18-3-10 Registers PWMCIF

9EH	7	6	5	4	3	2	1	0
PWMCIF	PWM5TIF	PWM5ZIF	PWM5PIF	-	PWM4TIF	PWM4ZIF	PWM4PIF	-
R/W	R	R	R	-	R	R	R	-
Initial Value	0	0	0	-	0	0	0	-

Bit Number	Bit Symbol	Description
7	PWM5TIF	PWM5 counter vertex interrupt flag, write 1 clear 0
6	PWM5ZIF	PWM5 counter lowest point interrupt flag, write 1 clear 0
5	PWM5PIF	PWM5 rising edge interrupt flag, write 1 clear 0
4	-	-
3	PWM4TIF	PWM4 counter vertex interrupt flag, write 1 clear 0
2	PWM4ZIF	PWM4 counter lowest point interrupt flag, write 1 clear 0
1	PWM4PIF	PWM4 rising edge interrupt flag, write 1 clear 0
0	-	-

19 SPI interface

19.1 Function Introduction

The SPI interface enables the chip to transfer data with other devices in half/full duplex synchronization. The peripheral devices can be other MCUs, ADCs, sensors, or flash memory, etc. The SPI can be three or four wires and has the following features.

- Supports host or slave operation
- Selectable lowest or highest bit priority transmission
- 4 programmable bit rates
- Programmable polarity and phase
- Send end of interrupt flag
- Write to conflict flag protection mechanism
- Support main mode failure error interrupt

Figures 19-1-1 and 19-1-2 are schematic diagrams of the SPI master mode and slave mode, respectively.

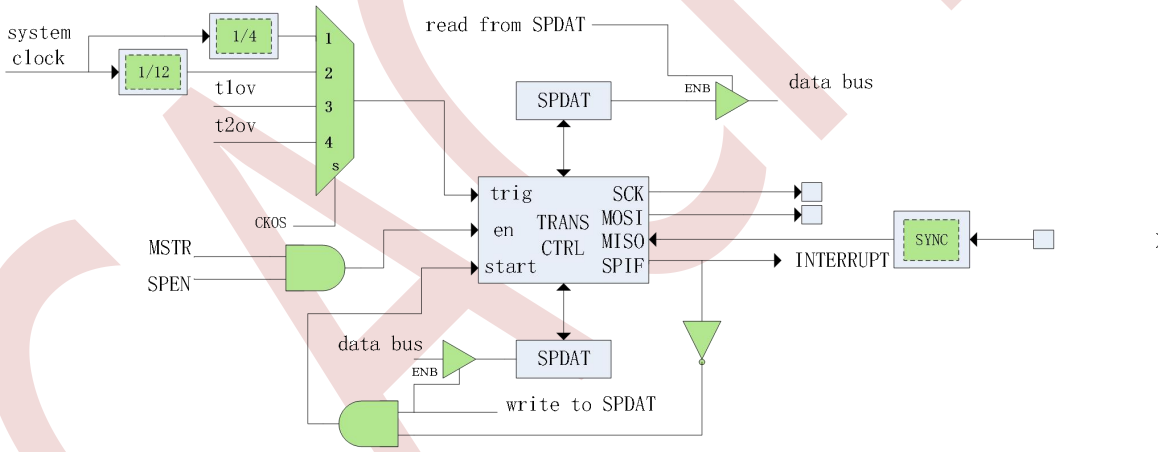


Figure 19-1-1 SPI host mode schematic

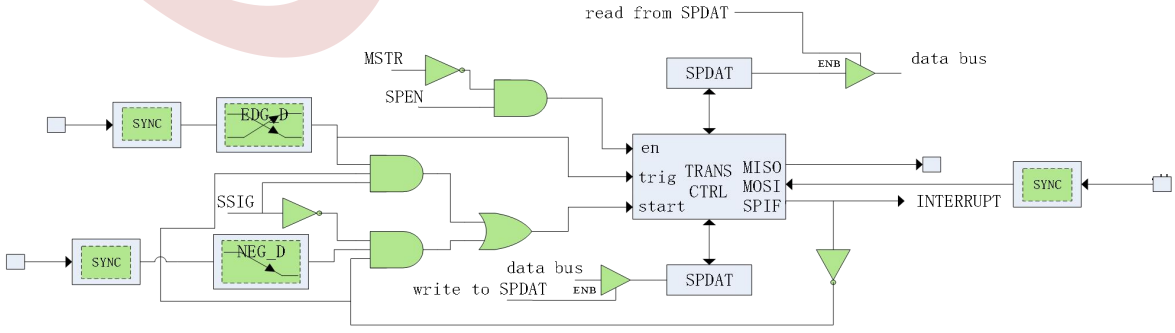


Figure 19-1-2 Schematic diagram of SPI slave mode

Table 19-1-1 SPI Operating Modes

Name	Description
Host Mode	All transmission actions are initiated by the host, including the generation of SCK and SSB signals, etc. When the MSTR (SPCON[4]) bit is set to 1, the SPI is in master mode. The user needs to select another GPIO as a chip select pin to connect to the slave SSB, and the host pulls this pin low before the data transfer starts and high after the transfer ends. In host mode, writing to register SPDAT initiates data transfer. Data is shifted out from MOSI on the valid edge of the clock.
Slave Mode	When the MSTR bit is set to 0, the SPI is in slave mode. When SSIG (SPCON[5]) is 1, the SSB pin is invalid, the SPI is three-wire communication, and the slave is valid for chip selection by default; when SSIG is 0, the SSB pin is valid and SSB is low to indicate that the slave is chip selected.

Table 19-1-2 SPI Interface Pin Descriptions

Name	Description
MOSI	Host output, slave input This pin is the master data output port when the SPI is used as a host and the slave data input port when it is used as a slave.
MISO	Host output, slave input This pin is the master data input port when the SPI is the host and the slave data output port when the SPI is the slave.
SCK	Serial Clock This pin is the serial clock output port when the SPI is the host and the serial clock input port when the SPI is the slave
SSB	Slave Selection This pin selects the input port for the slave when the SPI pin is the master, and the input port for the slave when it is the slave.

Table 19-1-3 SPI Phase and Polarity

Name	Description
CPHA	Phase control bits 0：denotes the data sampled at the odd edges of SCK (1,3,5,... ,15) sampled data 1：denotes data sampled at the even edges of SCK (2,4,6,... ,16) sampled data
CPOL	Polarity control bit 0：Indicates a low level when SCK is idle 1：Indicates that SCK is high when idle

Combined with Table 19-1-3, the waveforms during actual transmission are shown in Figure 19-1-3 and Figure 19-1-4.

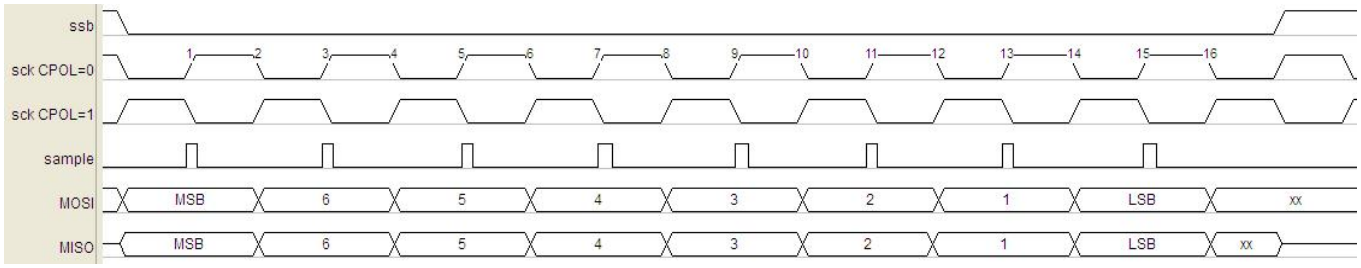


Figure 19-1-3 SPI Timing Diagram when CPHA=0

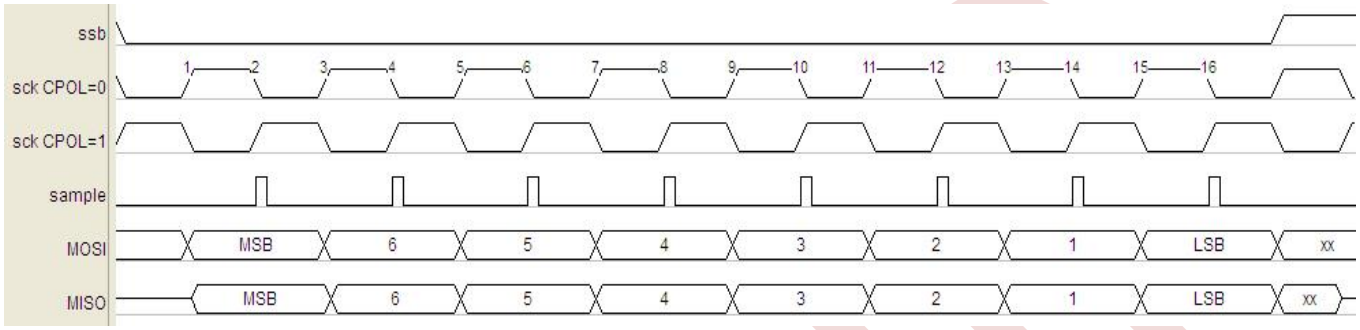


Figure 19-1-4 SPI Timing Diagram when CPHA=1

19.2 Register Description

Table 19-2-1 Register SPCON

A9H	7	6	5	4	3	2	1	0
SPCON	SPEN	LSBF	SSIG	MSTR	CPOL	CPHA	CKOS[1:0]	
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	SPEN	SPI module enable bit, 1 valid
6	LSBF	Low or high priority transmit/receive selection bit 0: High position first 1: Low position first
5	SSIG	SSB pin invalid control bit, the default is 0, when the SSB signal is valid.
4	MSTR	Host/Slave selection bit 0： Slave 1： Host
3	CPOL	Clock polarity selection bit 0: Clock is low by default 1: Clock is high by default
2	CPHA	Clock phase selection bit 0: Sample data when the clock leaves the default case 1: Sample data when the clock returns to the default case

1~0	CKOS	SPI output clock select bit 00:1/8 system clock 01: 1/24 system clock 10: Use timer 1 overflow flag to transfer data every two overflows

Table 19-2-2 Register SPDAT

AAH	7	6	5	4	3	2	1	0
SPDAT	RBUF[7:0]							
R/W	R							
Initial Value	0	0	0	0	0	0	0	0
SPDAT	TBUF[7:0]							
R/W	W							
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~0	SPDAT	When writing SPDAT, write to internal TBUF, when reading SPDAT, read from RBUF

Table 19-2-3 Register SPSTA

ABH	7	6	5	4	3	2	1	0
SPSTA	SPIE	-	-	-	-	WCOL	MODF	SPIF
R/W	R/W	-	-	-	-	R/W	R/W	R/W
Initial Value	0	-	-	-	-	0	0	0

Bit Number	Bit Symbol	Description
7	SPIE	SPI interrupt enable bit, 1 valid
6~3	-	-
2	WCOL	The write conflict flag bit is generated when the data is being sent, if there is a software operation to write SPDAT, then the data cannot be written, that is, the write conflict flag is generated. This bit is valid for 1, clear 0 for write 1, no interrupt will be generated when it is valid.
1	MODF	Fault mode flag bit, 1 valid, indicates SSB at incorrect logic level, write 1 to clear 0, valid will generate interrupt
0	SPIF	Data transfer completion flag bit, 1 is valid, write 1 to clear 0, interrupt will be generated when valid

20 Analog/Digital Converter (ADC)

20.1 Function Introduction

The analog/digital converter is a 12 bit successive approximation register (SAR) ADC that provides up to 46 input channels. The ADC clock source is the system clock, which can be set for clock pre division. ADC has multiple reference voltage sources to choose from, among which selecting the internal voltage as the reference voltage can be used to detect the chip power supply voltage. ADC has an automatic correction function when selecting internal voltage as the reference voltage to avoid chip consistency issues.

20.2 Main Features

- 12 bit resolution
- 46 input channels at most
- Supports ADC interrupt
- ADC clock frequency division configurable
- Alternate reference voltage：internal reference voltage, VDD
- Support the measurement of VDD and reference ground voltage
- Automatic data correction supported when internal reference voltage is selected
- When selecting an internal reference voltage, VDD voltage can be measured
- Input voltage range：VSS<=VIN<=VDD

20.3 Block Diagram

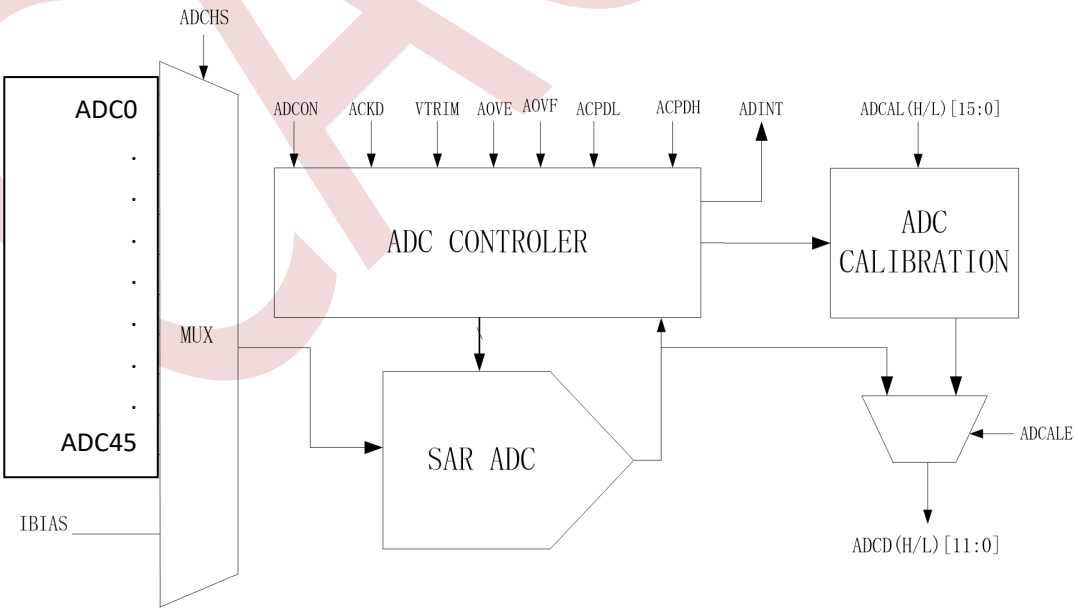


Figure 20-3-1 ADC Architecture

20.4 Function Introduction

ADC can be enabled by AST. When AST=1, the input voltage selected by ADCHS will be analog/digital converted. The clock for ADC is the system clock with frequency division set by ACKD beforehand. When ADC clock is constant, the time for single conversion is set by HTME. The conversion time is (13+2^HTME) ADC clock cycle periods. 12-bit A/D will be stored in register ADCDH and ADCDL after the conversion. AST will be cleared automatically 2.5 clock cycles later. The interrupt flag ADCIF will be set to 1 at the same time. If ADC interrupt is enabled then, ADC interrupt occurs. The shortest ADC conversion time is 0.5us. Figure 20-4-1 is the sequence diagram for ADC conversion.

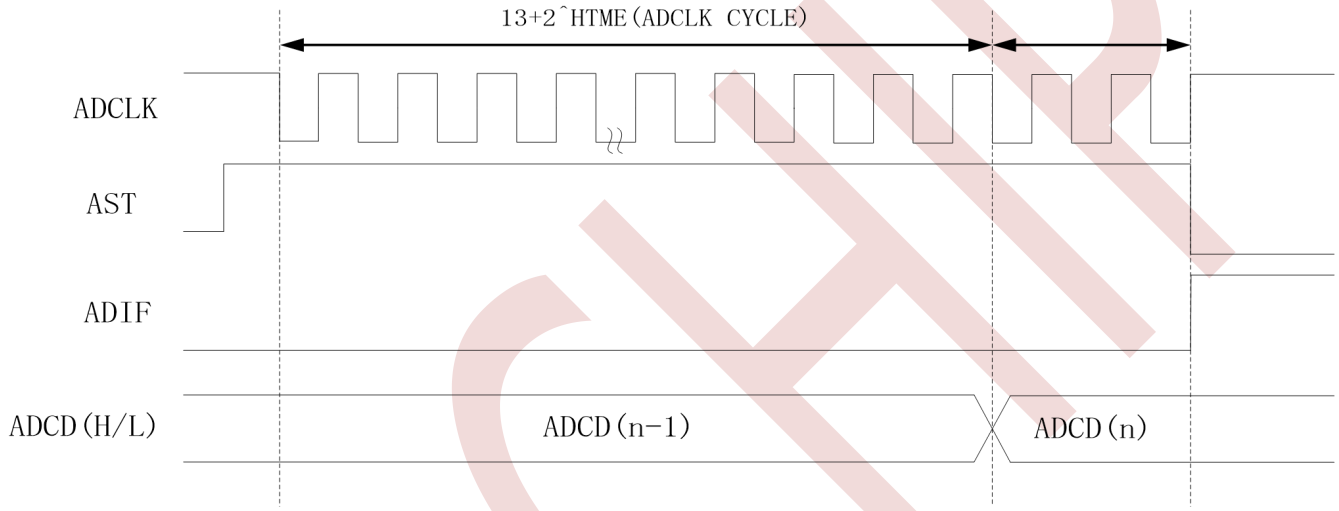


Figure 20-4-1 ADC Sequence Diagram

- **ADC Data Calibration**

When internal voltage(1.5V) is selected as the reference voltage, due to the discreteness of the chips, the internal voltage in each chip can not be exactly the same which induces different ADC conversion results consequentially. Thus, it is necessary to correct the AD value after the conversion. The internal voltage will be tested and a correction value will be obtained when chips leave factory. When the chip's powered on, the correction value will be loaded into register ADCALL and ADCALH. The accurate AD value will be obtained by calculation according to the correction value. The final accurate result for AD will be stored in register ADCD. The function can be enabled by ADCALE. Users only need to set ADCALE=1 and the correction will be done automatically.

20.5 Register Description

Table 20-5-1 Register ADCON

8060H	7	6	5	4	3	2	1	0
ADCON	AST	ADIE	ADIF	HTME			ADCALE	VSEL
R/W	R/W	R/W	R/W	R/W			R/W	R/W
Initial Value	0	0	0	0	1	0	1	0

Bit Number	Bit Symbol	Description
7	AST	ADC conversion enable control, the conversion starts when 1 is written to it, the hardware will clear it automatically after the conversion
6	ADIE	ADC interrupt enable control, 1 enables it
5	ADIF	ADC interrupt flag bit, write 1 to clear 0
4~2	HTME	The number of sampling periods is 2 power HTME
1	ADCALE	ADC calibration enable bit, 1 valid This bit is only valid when the reference voltage is selected as internal 1.5V. When ADCALE=1, the ADC conversion result will be calibrated based on the value of the ADCAL register. Please refer to register ADCAL Description for specific details.
0	VSEL	ADC reference voltage selection 0: internal 1.5V(INNER_VREF)as reference voltage 1: Power supply as reference voltage

Table 20-5-2 Register ADCFGL

8061H	7	6	5	4	3	2	1	0
ADCFGL	-	-	ADCHS					
R/W	-	-	R/W					
Initial Value	-	-	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~6	-	-
5~0	ADCHS	ADC channel enable selection bit field 6'h00: Channel closed 6'h01~6'h08: Channel AD_ CH0~AD_ CH7 6'h09~6'h10: Channel AD_ CH8~AD_ CH15 6'h11~6'h18: Channel AD_ CH16~AD_ CH23 6'h19~6'h20: Channel AD_ CH24~AD_ CH31 6'h21~6'h28: Channel AD_ CH32~AD_ CH39 6'h29~6'h2e: Channel AD_ CH40~AD_ CH45 6'h2f: Detect 1/4 enable of VDD Other: Channel closed

Table 20-5-4 Register ADCAL

8064H	7	6	5	4	3	2	1	0
ADCALL	ADCAL[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0

8065H	7	6	5	4	3	2	1	0
ADCALH	ADCAL[15:8]							
R/W	R/W							
Initial Value	0	0	0	1	0	0	0	0

Bit Number	Bit Symbol	Description
15~0	ADCAL	ADC calibration register, only ADCALE=1 and the reference voltage is selected as internal 1.5V is valid. When valid, the ADC output is in accordance with the following formula: ADCDL=(ADC conversion result*ADCAL)/32768 Remarks: ADCAL is automatically loaded by the system after power-on, and users are not allowed to modify it.

Table 20-5-5 Register ADCD

8062H	7	6	5	4	3	2	1	0
ADCDL	ADCDL[3:0]				-	-	-	-
R/W	R				-	-	-	-
Initial Value	0	0	0	0	-	-	-	-
8063H	7	6	5	4	3	2	1	0
ADCDH	ADCDH[11:4]							
R/W	R							
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
11~0	ADCD	ADC conversion value

Table 21-5-2 Register ADCKD

8066H	7	6	5	4	3	2	1	0
ADCFGL	ACKD			-				
R/W	R/W			-				
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~5	ACKD	ADC clock division setting 000: No frequency division 001:2 Frequency division 010:4 frequency division … 111:14 frequency division

21 Capacitive touch key (Touch Key)

21.1 Function Introduction

The touch function module of the CA51F155 series chip has superior anti-interference performance and can pass tests such as EFT and CS. The touch module can support up to 46 channels at most. Equipped with a built-in touch sensing controller, there is no need for external capacitors during application. For applications with low power consumption requirements, support touch low power mode to achieve product power-saving function.

21.2 Main features

- Built in touch sensing controller
- Supports up to 46 touch channels without the need for external capacitors
- High anti-interference performance, in compliance with EMC (CS) standards
- Support touch interruption
- Support parallel connection of touch channels, enabling low-power touch mode

21.3 Function Description

The touch function requires setting corresponding parameters through a series of registers, including charging and discharging clock frequency, counting clock frequency, counting digits, discharge resistance, comparator voltage, charging current source current, etc. After setting the parameters, enable the touch function through TKEN. After setting the touch channel, set TKST=1 to start the touch data collection of the corresponding channel. After data collection is completed, the 16 bit touch data is stored in TKDH and THDL, and the touch interrupt flag TKIF is generated.

The touch module supports multiple touch channels in parallel, which can significantly reduce power consumption when used in touch power-saving mode.

For more touch related content, please refer to the touch library and related documentation, and it is recommended to conduct secondary development based on the touch library provided by our company.

21.4 Register description

Table 21-4-1 Register TKST

F8H	7	6	5	4	3	2	1	0
TKST	-	-	-	-	-	-	-	TKST
R/W	-	-	-	-	-	-	-	RW
Initial Value	-	-	-	-	-	-	-	0

Bit Number	Bit Symbol	Description
7~1	-	-
0	TKST	Data collection start enable bit, 1 is valid, automatically cleared to 0 after collection is completed

Table 21-4-2 Register TKCFG1

F9H	7	6	5	4	3	2	1	0
TKCFG1	-	TKEN	TKDIV					
R/W	-	R/W	R/W					
Initial Value	-	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	-	-
6	TKEN	Enable touch simulation module
5~0	TKDIV	Charging and discharging clock selection: 0-61: The charging and discharging clock has a fixed frequency, and the clock frequency is F=24/(TKDIV+4) 62~63: Charge and discharge clock frequency hopping, maximum frequency 3M, minimum frequency 1M, center frequency 1.5MHz

Table 21-4-3 Register TKCFG2

FAH	7	6	5	4	3	2	1	0
TKCFG2	TKPULL8	PAREN	TKCADDR					
R/W	R/W	R/W	R/W					
Initial Value	0	1	0					

Bit Number	Bit Symbol	Description
7	TKPULL8	Charging current source configuration highest bit
6	PAREN	0: Single channel 1: All enabled channels are connected in parallel
5~0	TKCADDR	Channel selection bit: 6'h00~6'h07: TK0~ TK7 6'h08~6'h0f : TK8~ TK15 6'h10~6'h17: TK16~ TK23 6'h18~6'h1f : TK24~ TK31 6'h20~6'h27: TK32~ TK39 6'h28~6'h2d: TK40~ TK45

Table 21-4-4 Register TKCFG3

FBH	7	6	5	4	3	2	1	0
TKCFG3	-	RESO			TKCKSEL		CHGSEL	DCHSEL
R/W	-	R/W			R/W		R/W	R/W
Initial Value	-	0	0	1	1	1	1	1

Bit Number	Bit Symbol	Description
7~5	-	-
6~4	RESO	Counter bit selection 000: 9 digits 001: 10 digits 010: 11 digits 011: 12 digits 100: 13 digits 101: 14 digits 110: 15 digits 111: 16 digits
3~2	TKCKSEL	Count clock selection 0: 24Mhz 3: 4Mhz Other values: invalid
1	CHGSEL	Pre charging time selection 0:20 us 1: 40us
0	DCHSEL	Pre discharge time selection 0:2 us 1: 10us

Table 21-4-5 Register TKPULL

FEH	7	6	5	4	3	2	1	0
TKPULL[7:0]	TKPULL[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~0	TKPULL	Setting the charging current source to 8 low bits

Table 21-4-6 Register TKDL/TKDH

FCH	7	6	5	4	3	2	1	0
TKDL	TKD[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
FDH	7	6	5	4	3	2	1	0
TKDH	TKD[15:8]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~0	TKD	The current sampling value of the touch channel

Table 21-4-7 Register TKPULLTRIM

F2H	7	6	5	4	3	2	1	0
TKPULLTRIM	-	-	TKPULLTRIM [5:0]					
R/W	-	-	RW					
Initial Value	-	-	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~0	TKPULLTRIM	Charging current compensation value

Table 21-4-8 Register TKIE

F4H	7	6	5	4	3	2	1	0
TKIE	TKIE	-	-	-	-	-	-	TKIF
R/W	RW	-	-	-	-	-	-	R
Initial Value	0	-	-	-	-	-	-	0

Bit Number	Bit Symbol	Description
7	TKIE	Touch interrupt enable bit, 1 valid
6~1	-	-
0	TKIF	Touch to collect interrupt flag bit, write 1 clear 0

Table 21-4-9 Register TKCFG4

FFH	7	6	5	4	3	2	1	0
TKCFG4	-	-	RBSEL			VRSEL		
R/W	-	-	RW			RW		
Initial Value	-	-	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7~6	-	-
5~3	RBSEL	Selection of discharge resistance size 000:20K 001:30K 010:40K 011:50K 100:70K 101:90K 110:200K 111:350K
2~0	VRSEL	Comparator threshold voltage selection 000:1.8V 001:2.1V 010:2.5V 011:2.8V 100:3.2V 101:3.5V 110:3.9V 111:4.1V

22 Low Voltage Detection (LVD)

22.1 Function Introduction

Low voltage detection (LVD) is used to monitor the power supply VDD of the chip itself, and the detection voltage range can be set to 2.2V, 2.5V, 2.7V, 3.0V, 3.3V, 3.6V, 3.9V, and 4.2V. When the VDD is less than the set voltage value, a trigger interrupt or reset can be set.

Note: Due to the production process, there is a certain difference in LVD trigger voltage between chips.

Figure 22-1-1 shows the architecture of LVD.

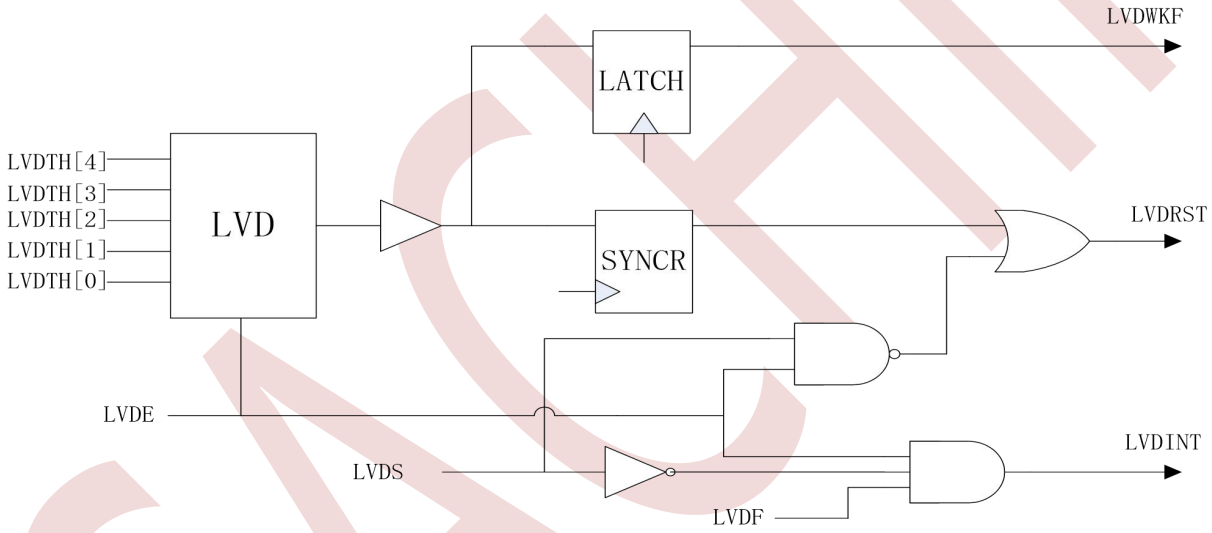


Figure 22-1-1 LVD Schematic

22.2 Function Description

The LVD function is enabled via the LVDE bit, while the detected voltage is set via the LVDTH bit field. When the chip VDD is less than the set voltage, the flag LVDF bit generated by the LVD function will set to 1. If LVDS = 0, an LVD interrupt will be generated, and if LVDS = 1, a reset will be generated. It should be noted that after LVD reset is generated, the circuit of LVD itself will not be reset, and the register LVDCON will keep the previous state. Therefore, if VDD continues to fall below the set voltage after LVD reset is generated, the chip will remain in the reset state. Similarly, when the LVD interrupt is generated, the LVD interrupt will be generated repeatedly if VDD continues to fall below the set voltage.

22.3 Register Description

Table 22-3-1 Register LVDCON

E8H	7	6	5	4	3	2	1	0
LVDCON	LVDE	LVDS	LVDF				LVDTH[1:0]	
R/W	R/W	R/W	R/W				R/W	
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	LVDE	LVD enable control, 1 enables it
6	LVDS	LVD function selection 0: Interrupt 1: Reset
5	LVDF	LVD generate flag ,cleared when 1 is written to it
1~0	LVDTH	LVD trigger level selection bit field 000:2.2V 001: 2.5V 010:2.7V 011:3.0V 100:3.3V 101:3.6V 110:3.9V 111:4.2V

22.4 LVD control routines

LVD interrupt routines

For example, if LVD is set to interrupt mode and the detection voltage is 3V, the program is as follows：

```
-------------------------------------------------------------------------------------------
#define LVDE(N)          (N<<7)    //N=0~1
#define LVDS_reset       (1<<6)
#define LVDS_int         (0<<6)
#define LVDF             (1<<5)
#define LVDTH_3V         3
void LVD_init(void)
{
    LVDCON = LVDE(1) | LVDS_int | LVDF |LVDTH_3V;  // Set LVD enable, LVD is interrupt mode, detection
                                                    // voltage is 3V
    INT4EN = 1;                  // INT4 interrupt enable
    EA = 1;                      // Turn on total interruption
}
void INT4_ISR (void) interrupt 6
{
    if(LVDCON & LVDF)
    {
        LVDCON |= LVDF;          // Clear the LVD interrupt flag
    }
}
-------------------------------------------------------------------------------------------
```

LVD Reset Routine

For example, setting LVD to reset mode and detecting a voltage of 3V, the program is as follows.

```
-------------------------------------------------------------------------------------------
#define LVDE(N)          (N<<7)    //N=0~1
#define LVDS_reset       (1<<6)
#define LVDS_int         (0<<6)
#define LVDF             (1<<5)
#define LVDTH_3V         3
void LVD_init(void)
{
    LVDCON = LVDE(1) | LVDS_reset | LVDF | LVDTH_3V;// Set LVD enable, LVD is interrupt mode, detection
                                                    // voltage is 3V
}
-------------------------------------------------------------------------------------------
```

23 LCD/LED driver

23.1 LCD driver

23.1.1 Function Introduction

The built-in LCD driver can support up to 40 output pins, including 8com x 32seg, 7com x 33seg, 6com x 34seg, 5com x 35seg, and 4com x 36seg. Programmable duty cycles are: 1/2, 1/3, 1/4, 1/5, 1/6, 1/7, 1/8. The programmable bias ratio is: 1/2, 1/3, 1/4. The programmable LCD driver has a strength of 8 levels. Figure 23-1-1-1 is a schematic diagram of the principle of LCD.

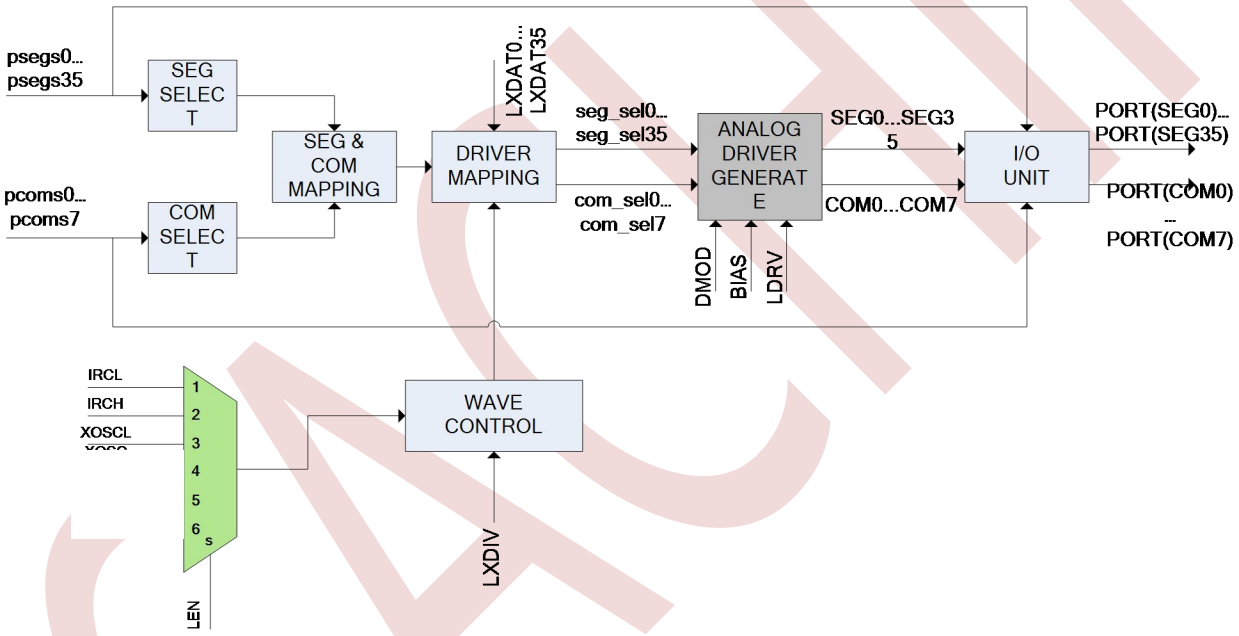


Figure 23-1-1-1 Schematic diagram of LCD principle

23.1.2 LCD bias voltage

The programmable bias ratio of LCD is 1/2, 1/3, and 1/4, and the corresponding signal diagrams are shown below.

- LCD bias ratio of 1/2

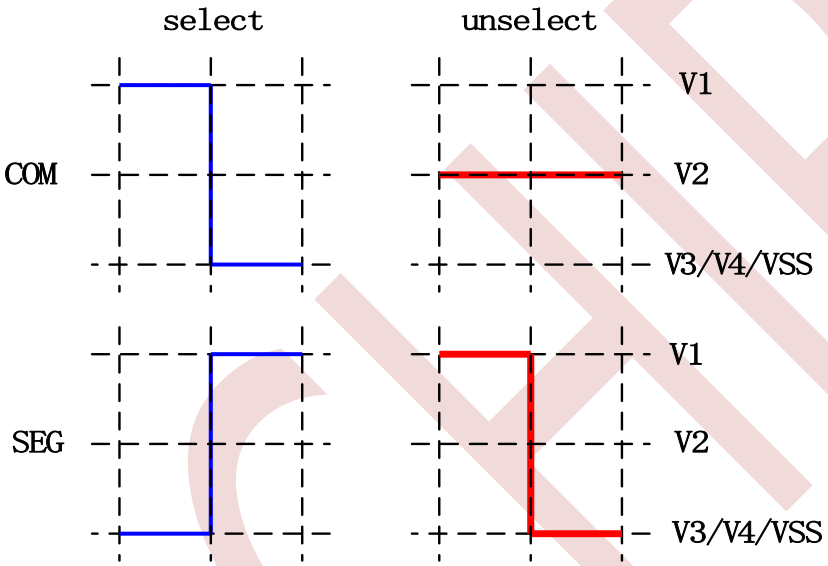


Figure 23-1-1-2 LCD Bias Ratio 1/2 Signal

- LCD bias ratio of 1/3

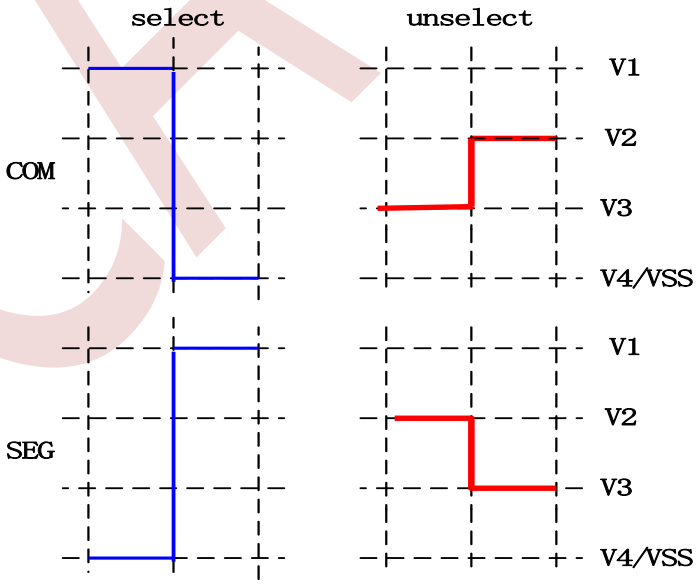


Figure 23-1-1-3 LCD bias ratio 1/3 signal

- LCD bias ratio of 1/4

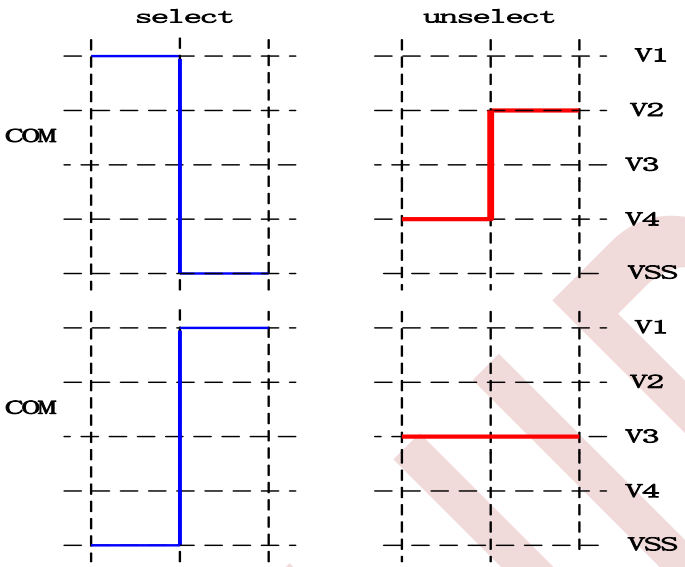


Figure 20-1-1-4 LCD bias ratio 1/4 signal

23.1.3 LCD Function Description

The LCD mode is selected by setting LMOD=1. The LCD driver can select a clock source through LEN, and when the clock source is selected, the LCD driver is also enabled; It should be noted that when setting the clock source, it is necessary to ensure that the clock source is turned on and working properly. Register LXDIV is an LCD clock divider that can set different division coefficients for different clock sources. The typical frame frequency for LCD scanning is 64Hz. The LCD driver has 8 levels of adjustable driving intensity, which can be set through LDRV. The output voltage varies with different driving intensities, and this value can be adjusted for different LCD displays during application. To meet different power consumption requirements, LCD drivers have four levels of drive current selection, which is set through DMOD. When the drive current is smaller, the power consumption of the driver itself is also smaller, but the noise on the LCD pins is also larger.

The programmable duty cycle of LCD is: 1/2, 1/3, 1/4, 1/5, 1/6, 1/7, 1/8. The duty cycle is determined by the number of enabled COMs. For example, if 3 COMs are enabled, the duty cycle is 1/3, and if 8 COMs are enabled, the duty cycle is 1/8. Enabling COM does not need to be done in the order of COM pin numbers, and can be combined arbitrarily. However, the enabled COM pins correspond to actual COM0, COM1, COM2, etc. in ascending order of serial numbers. For example, if enabled pins COM3, COM5, and COM7 are COM ports, then COM3 corresponds to actual COM0, COM5 corresponds to actual COM1, and COM7 corresponds to actual COM2, with a duty cycle of 1/3. The SEG pin can also be enabled arbitrarily, and the enabled SEG pins correspond to the actual SEG0, SEG1, SEG2, etc. in ascending order of their serial numbers. For example, if the enabled pins SEG3, SEG5, SEG7... are enabled, then SEG3 corresponds to the actual SEG0, SEG5 corresponds to the actual SEG1, and SEG7 corresponds to the actual SEG2. The COM and SEG pins that are not enabled can be set for other functions and do not conflict with the LCD driver.

The LCD driver has a 36 byte LCD display cache. The LCD display cache corresponds to the actual COM and SEG. The 36 byte display cache corresponds to SEG0~SEG35 in order, while COM0~COM7 corresponds to the 0-7 bits of each byte. The display cache is accessed through the index register INDEX and data register LXDAT, with INDEX set to 0-35 corresponding to the display cache of SEG0-SEG35 in order.

23.2 LED drive

23.2.1 Function Introduction

The built-in LED driver can support up to 8com x 32seg, and shares display cache and driver pins with the LCD driver. The LED driver has 8 levels of adjustable brightness. Built in global flicker function, flickering at a frequency of 1Hz at a scanning frequency of 256Hz. Figure 23-1-1 is a schematic diagram of the principle of LED.

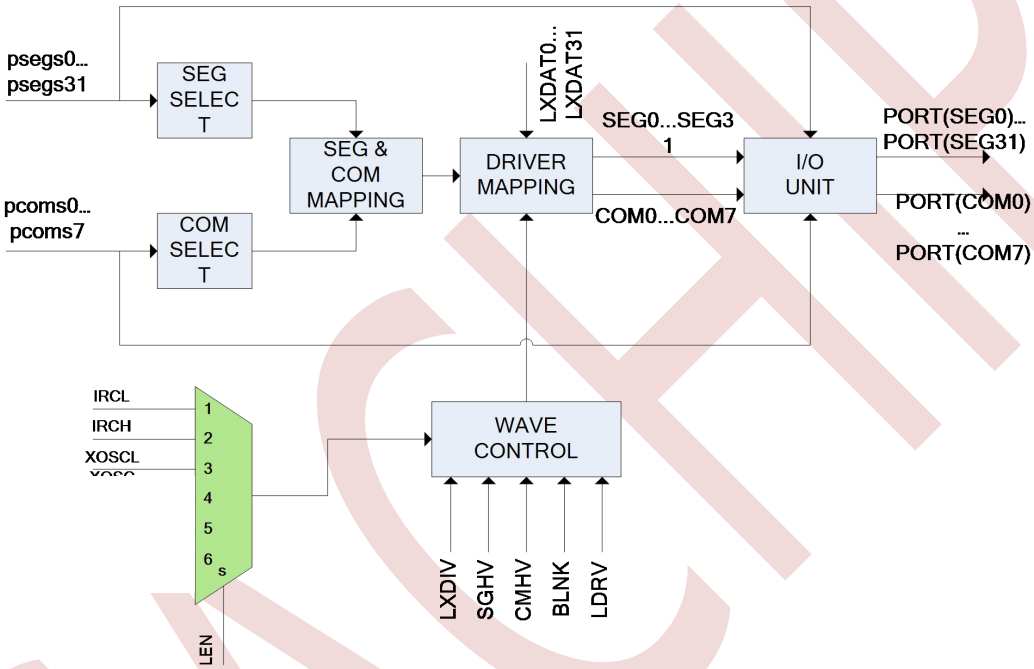


Figure 23-2-1-1 Schematic diagram of LED principle

Figures 23-2-1-2 show the driving waveform of the LED:

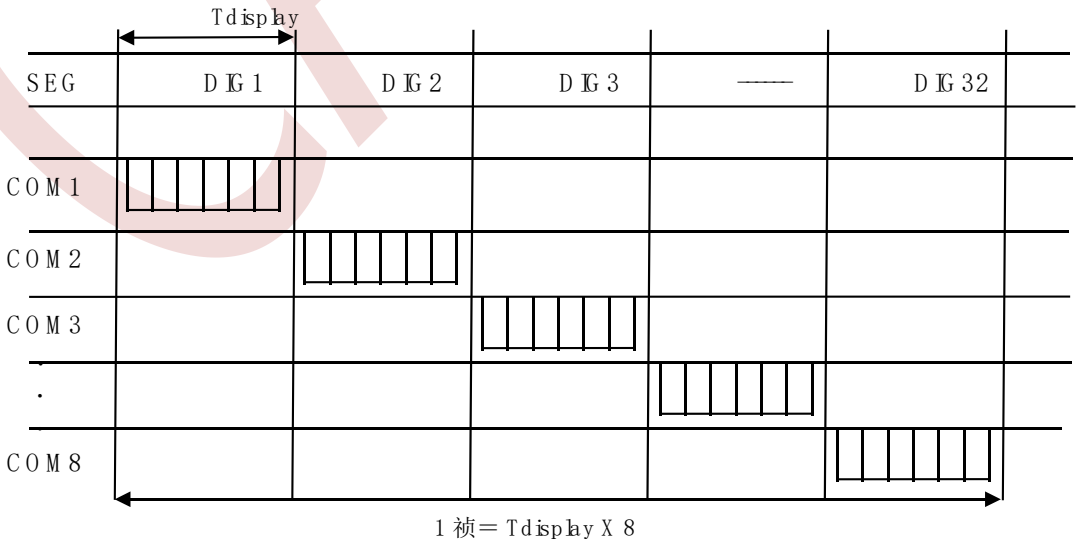


Figure 23-2-1-2 LED Drive Waveform

23.2.2 LED Function Description

The LED mode is selected by setting LMOD=0. The LED driver can select the clock source through LEN, and when the clock source is selected, the LED driver is also enabled; It should be noted that when setting the clock source, it is necessary to ensure that the clock source is turned on and working properly. Register LXDIV is an LED clock divider that can set different division coefficients for different clock sources. The typical frame frequency for LED scanning is 256Hz. The LED driver has 8 levels of adjustable brightness, which can be set through LDRV, and different values correspond to different duty cycles.

Similar to LCD drivers, the basic duty cycle of LEDs is also determined by the number of enabled COM pins. COM pins and SEG pins can also be combined arbitrarily, as described in the LCD section.

The LED driver and LCD driver jointly display the cache, and the corresponding relationship between the display cache and the COM and SEG ports, as well as the access method of the display cache, are the same as those of the LCD driver. You can also refer to the relevant descriptions in the LCD driver section.

23.3 LCD/LED Register description

Table 23-3-1 Register LXCON

E9H	7	6	5	4	3	2	1	0
LXCON	-	LEN[2:0]		LMOD	-	-	-	-
R/W	-	R/W		R/W	-	-	-	-
Initial Value	-	0	0	0	-	-	-	-

Bit Number	Bit Symbol	Description
7	-	-
6~5	LEN	LCD/LED clock selection bit 01: IRCL 10: IRCH 11: XOSCL Other: Module shutdown
4	LMOD	Mode selection bit 0: LCD mode 1: LED mode
3~0	-	-

Table 23-3-2 Registers LXCFG

EAH	7	6	5	4	3	2	1	0
LCD mode								
LXCFG	DMOD[1:0]			BIAS[1:0]		LDRV[2:0]		
R/W	R/W			R/W		R/W		
Initial Value	0	0	0	0	0	0	0	0
LED mode								
LXCFG	-	-	COMHV	SEGHV	BLNK	LDRV[2:0]		
R/W	-	-	R/W	R/W	R/W	R/W		
Initial Value	-	-	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
LCD mode		
7~5	DMOD	LCD driver current selection bit 000：5uA 001：40uA 010：80uA 011：130uA 100：200uA 101：320uA 110：450uA 111：600uA
4~3	BIAS	LCD bias selection bit 01：1/2 Bias 10：1/3 Bias other：1/4 Bias
2~0	LDRV	LCD driver intensity control bit 000：Level 1（Min） 001：Level 2 ... 111：Level 8（Max）
LED mode		
7~6	-	-
5	COMHV	When it is 0/1, it indicates that COM output 0/1 is valid
4	SEGHV	When it is 0/1, it indicates that SEG output 0/1 is valid
3	BLNK	LED global flashing control bit, 1 effective *Remarks:* *The flashing time is 128 frames of LED output. For example, if the LED working clock is set to 32.768KHz and LXDIV=0, the output frequency of the LED is 256Hz, and the flashing frequency is 1Hz.*

2~0	LDRV	LED brightness adjustment position 000：Level 1(Darkest） 001：Level 2 010：Level 3 011：Level 4 100：Level 5 101：Level 6 110：Level 7 111：Level 8(Brightest)

Table 23-3-3 Registers LXDAT

EBH	7	6	5	4	3	2	1	0
LXDAT	LXDAT[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
Note: LXDAT is an indexed register, set INDEX=0~35 to correspond to LXDAT0~LXDAT35 respectively								
Bit Number	Bit Symbol		Description					
7~0	LXDAT		Display cache read/write registers *Note: LXDAT32~LXDAT35 have no effect on LED drivers.*					

Table 23-3-4 Registers LXDIV

ECH	7	6	5	4	3	2	1	0
LXDIVL	LXDIV[7:0]							
R/W	R/W							
Initial Value	0	0	0	0	0	0	0	0
EDH	7	6	5	4	3	2	1	0
LXDIVH	-	-	-	-	LXDIV[11:8]			
R/W	-	-	-	-	R/W			
Initial Value	-	-	-	-	0	0	0	0
Bit Number	Bit Symbol		Description					
15~12	-		-					
11~0	LXDIV		LXD Clock Divider LCD scanning frame frequency=LXD clock frequency ÷ (LXDIV+1) x 512) LED selection high-speed clock scanning frame frequency=LXD clock frequency ÷ (LXDIV+1) x 1024) LED selection low-speed clock scanning frame frequency=LXD clock frequency ÷ (LXDIV+1) x 128) *Remarks:* *1. LED selection for high-speed clock representation, LED working clock selection for IRCH/XOSCH/PLL/TFRC; LED selects low-speed clock*					

		representation, and the LED working clock selects IRCL/XOSCL. 2. *When the LCD/LED clock is selected as IRCL, the clock frequency is 1/4 of IRCL.* 3. *The typical scanning frame frequency of LCD is 64Hz, and the typical scanning frame frequency of LED is 256Hz.*

Table 23-3-5 Registers LXCAD

EEH	7	6	5	4	3	2	1	0
LXCAD	-	-	-	-	CAD_MOD[1:0]		CAD_LTH[1:0]	
R/W	-	-	-	-	R/W		R/W	
Initial Value	-	-	-	-	0	1	0	1

Bit Number	Bit Symbol	Description
7~4	-	-
3~2	CAD_MOD	LCD_ CAD mode selection 00: Turn off LCD_ CAD 01: LCD_ The length of CAD is determined by the length of the digital signal Other: LCD_ CAD length controlled by analog signals *Note: In low-power mode, the LCD can be selected to be turned off_ CAD, the current can be reduced by about 5-10uA*
1~0	CAD_LTH	Analog signal control LCD_ CAD length selection, only available in CAD_ Effective when MOD=2/3 00：4us 01：8us 10：12us 11：16us

Table 23-3-6 LCD/LED Display Cache

INDEX	SEG	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7
0	0	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
1	1	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
2	2	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
3	3	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
4	4	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
5	5	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
6	6	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
7	7	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
8	8	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
9	9	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
10	10	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7

11	11	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
12	12	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
13	13	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
14	14	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
15	15	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
16	16	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
17	17	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
18	18	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
19	19	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
20	20	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
21	21	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
22	22	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
23	23	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
24	24	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
25	25	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
26	26	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
27	27	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
28	28	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
29	29	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
30	30	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
31	31	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
32	32	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	-
33	33	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	-	-
34	34	BIT0	BIT1	BIT2	BIT3	BIT4	-	-	-
35	35	BIT0	BIT1	BIT2	BIT3	-	-	-	-

24 Analog Comparator（COMP）

24.1 Function Introduction

- Integrate 2 independent analog comparators
- The reference signal of the inverter input end of the comparator 1/2 can be input from external sources or an internal power reference can be used
- Internal power benchmark with multiple adjustable levels

24.2 Register description

Table 24-2-1 Registers CMPCON

E5H	7	6	5	4	3	2	1	0
CMPCON	C2EN	C2HYEN	C2NCHS		C1EN	C1HYEN	C1NCHS	
R/W	R/W	R/W	R/W		R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	C2EN	Comparator 2 enable signal, 1 enable, 0 not enable
6	C2HYEN	Comparator 2 hysteresis enabled, 1 enabled, 0 not enabled
5-4	C2NCHS	Selection signal for INN2 input at the negative end of comparator 2: C2NCHS<1:0>=00，INN2=C2N C2NCHS<1:0>=01，INN2=0.75V C2NCHS<1:0>=10，INN2=1V C2NCHS<1:0>=11，INN2=1.25V
3	C1EN	Comparator 1 enable signal, 1 enable, 0 not enable
2	C1HYEN	Comparator 1 hysteresis enabled, 1 enabled, 0 not enabled
1~0	C1NCHS	Selection signal for INN1 input at the negative end of comparator 1: C1NCHS<1:0>=00，INN1=C1N C1NCHS<1:0>=01，INN1=0.75V C1NCHS<1:0>=10，INN1=1V C1NCHS<1:0>=11，INN1=1.25V

Table 24-2-2 Registers CMPOUT

E6H	7	6	5	4	3	2	1	0
CMPOUT	-	-	-	-	-	-	CMP2OUT	CMP1OUT
R/W	-	-	-	-	-	-	R	R
Initial Value	-	-	-	-	-	-	0	0

Bit Number	Bit Symbol	Description
7~2	-	-
1	CMP2OUT	Output of comparator 2
0	CMP1OUT	Output of comparator 1

25 Program download and simulation

25.1 Program Download

The CA51F155 series chips mainly use ISP to download programs, and the chips are connected to the download tool through the I2C interface. The download port varies for different models, as shown in Table 25-1-1.

Table 25-1-1 Download/Simulation Interface Table

Chip model	Download/Simulation Interface
CA51F155L0	P3.3（IIC_SDA）、P3.2（IIC_SCL）
CA51F155L1	P2.5（IIC_SDA）、P2.4（IIC_SCL）
CA51F155L2	P2.5（IIC_SDA）、P2.4（IIC_SCL）
CA51F155S6A	P1.4（IIC_SDA）、P1.2（IIC_SCL）
CA51F155S6B	P2.6（IIC_SDA）、P2.5（IIC_SCL）

For more details on the program download steps, please refer to the "CACHIP Development Download Tool Usage Description".

Important reminder:

In principle, the download/simulation interface will not reuse other functions to ensure normal online upgrades and simulation functions. In cases where GPIO is in short supply, it is recommended to use it as a button, touch, plug and unplug connector, etc.

25.2 Online Simulation

The CA51F155 series chip supports online simulation, and the chip communicates with the simulator through the I2C interface. The I2C interface is detailed in Table 25-1-1. It should be noted that due to the IIC communication between the chip and the simulator, the I2C interface pins connected to the simulator cannot be set to other functions, and the IIC function cannot be used in the application program, otherwise it will not be able to enter simulation mode. In addition, since the communication speed of I2C is determined by the main clock, the application cannot set the main clock to a low-speed clock or enter power-saving mode, otherwise it will affect the communication between the chip and the simulator.

When the chip enters simulation mode, the TSMODE bit (PCON [2]) is set to 1, and the application program can determine whether to switch to low-speed clock or enter power-saving mode by judging the status of this bit.

For more details on simulation functions, please refer to the relevant documentation of the simulator.

26 Electrical Characteristics

26.1 Limit parameters

Parameters	Minimum value	Maximum value	Unit
DC supply voltage	-0.3	6	V
I/O pin input voltage	-0.3	VDD+0.3	V
Working environment temperature	-40	85	℃
Storage temperature	-55	125	℃
CPU operating frequency	-	12	MHz

Note: Exceeding the "limit parameter" range may cause damage to the chip, and it is not possible to anticipate the working state of the chip outside the above range.

26.2 DC electrical characteristics

DC electrical characteristics (VDD=2.3-5.5V, TA=25 ℃, unless otherwise described)

Chip Parameters	Symbols	Operating Voltage	Minimum value	Typical values	Maximum value	Unit	Test conditions
Operating current	Iop1	VDD=2.7V	-	3.39	-	mA	The system clock is IRCH (12MHz), all other clocks are turned off, all output pins are unloaded, all Digital Input pins are not floating, all peripherals are turned off, and the CPU executes NOP instructions
		VDD=3.3V	-	4.31	-		
		VDD=5V	-	6.68	-		
	Iop3	VDD=2.2V	-	43	-	uA	The system clock is IRCL (128kHZ), all other clocks are turned off, all output pins are unloaded, all Digital Input pins are not floating, all peripherals are turned off, and the CPU executes NOP instructions
		VDD=3.3V	-	57	-		
		VDD=5V	-	80	-		
STOP mode current	I_{stp}	VDD=2.7V	-	4.8	-	uA	All clocks are turned off, all output pins are unloaded, all Digital Input pins are not floating, all peripherals are turned off, Flash enters sleep mode, and CPU enters STOP mode.
		VDD=3.3V	-	4.9	-		
		VDD=5V	-	5.1	-		

IDLE mode current	I_{idl1}	VDD=2.7V	-	2.09	-	mA	The system clock is set to IRCH (12MHz), other clocks are turned off, all output pins are unloaded, all Digital Input pins are not floating, all peripherals are turned off, Flash enters sleep mode, and CPU enters IDLE mode.
		VDD=3.3V	-	2.59	-		
		VDD=5V	-	4.18	-		
	I_{idl2}	VDD=2.2V	-	24	-	uA	The system clock is set to IRCL (128KHz), other clocks are turned off, all output pins are unloaded, all Digital Input pins are not floating, all peripherals are turned off, and the CPU enters IDLE mode.
		VDD=3.3V	-	34	-		
		VDD=5V	-	52	-		
IO port input high voltage (Smit mode on)	V_{hi1}	VDD=2.5V	1.17	-	2.5	V	-
		VDD=3.3V	1.73	-	3.3		
		VDD=5V	2.45	-	5		
IO port input high voltage (Smit mode off)	V_{hi2}	VDD=2.5V	-	0.5*VDD	VDD	V	-
		VDD=3.3V					
		VDD=5V					
IO port input low voltage (Smit mode on)	V_{lo1}	VDD=2.5V	0	-	1.02	V	-
		VDD=3.3V	0	-	1.30		
		VDD=5V	0	-	1.73		
IO port input low voltage (smit mode off)	V_{lo2}	VDD=2.5V	0	0.5*VDD	-	V	-
		VDD=3.3V					
		VDD=5V					
IO port push current	I_{pu}	VDD=3.3V	-	4mA @DRV=0 7mA @DRV=1	-	mA	IO set to push-pull output mode, with optional two-stage driving capability (DRV), Voh=0.9 * VDD
		VDD=5V	-	8mA @DRV=0 15mA @DRV=1	-		
IO port sink current	I_{ol}	VDD=3.3V	-	11mA @DRV=0 25mA @DRV=1	-	mA	IO set to push-pull output mode, with optional two-stage driving capability (DRV), Vol=0.1 * VDD
		VDD=5V	-	20mA @DRV=0 40mA @DRV=1	-		
P3.0~P3.7 Strong current injection	Isi	VDD=3.3V	-	30mA @DRV=0 37mA @DRV=1 43mA @DRV=2 49mA @DRV=3	-	mA	IO is set to push-pull output or PWM pin function, pin large current enable (SINK_1N=1, optional DRV for four level drive capability), Vol=0.1 * VDD
		VDD=5V	-	56mA @DRV=0 69mA @DRV=1 80mA @DRV=2 90mA @DRV=3	-		

IO port pull-down resistor	Rd1	VDD=2.2~5.5V	-	30	-	KΩ	-
IO port pull-up resistor	Ru1	VDD=2.2~5.5V	-	30	-	KΩ	-

Note: The above parameters are typical chip test results randomly selected for reference.

26.3 ESD/EFT Characteristics

symbol	mode	Conditions	package	Maximum value	Unit
V_{ESD}	electrostatic discharge (Human discharge mode HBM)	TA=+25℃	LQFP48	7000	V
	electrostatic discharge (Component discharge mode CDM)			1000	V

symbol	Conditions		package	pass through	Unit
EFT	F_{sys} = 12MHz / UART communicate	TA=+25℃	LQFP48	±4000	V

26.4 AC Electrical Characteristics

AC electrical characteristics (VDD=2.2-5.5V, TA=25°C, unless otherwise specified)

Chip Parameters	Symbol	Minimum value	Typical values	Maximum value	Unit	Conditions
Internal low speed clock (IRCL) start time	Trc1	-	50	-	us	IRCL frequency is 128Khz
Internal high speed clock (IRCH) start time	Trc2	-	10	-	us	IRCH frequency is 12MHz

Note: VDD=5V,TA=25 ℃,internal high speed clock factory frequency is 12MHz,accuracy is ±2%.

26.5 Internal RC clock temperature characteristics

- **IRCH temperature characteristic**

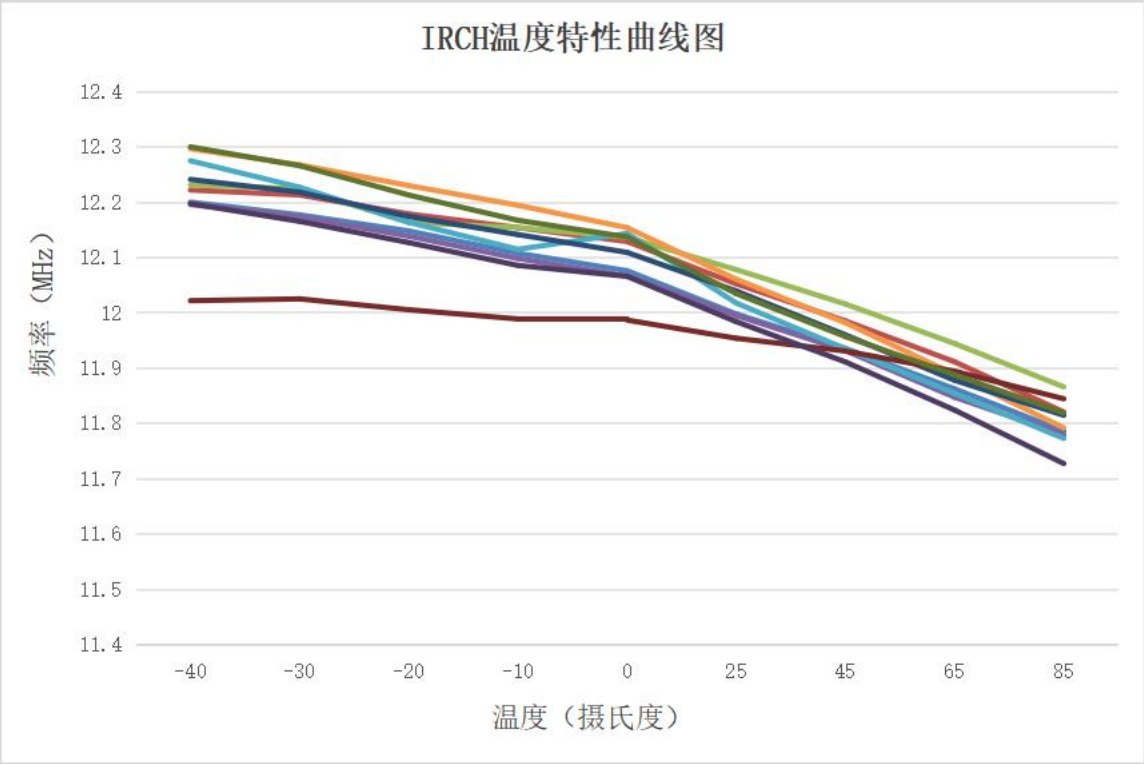
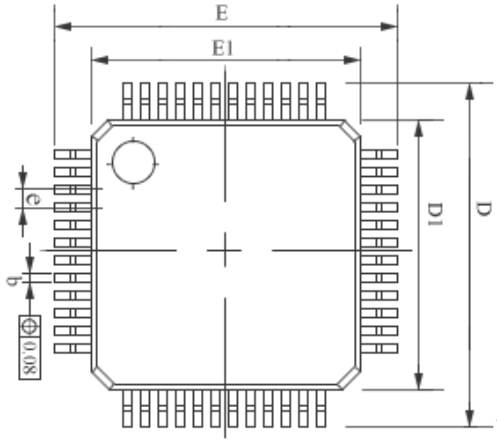


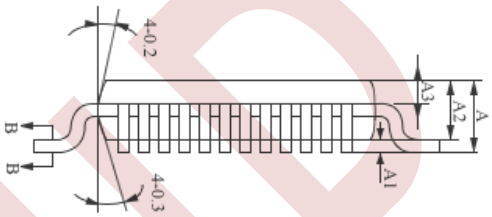
Figure 26-5-1 IRCH temperature characteristic curve

Note: The above graphic data is a randomly selected portion of chip test data, and the data is for reference only.

27 Package Type

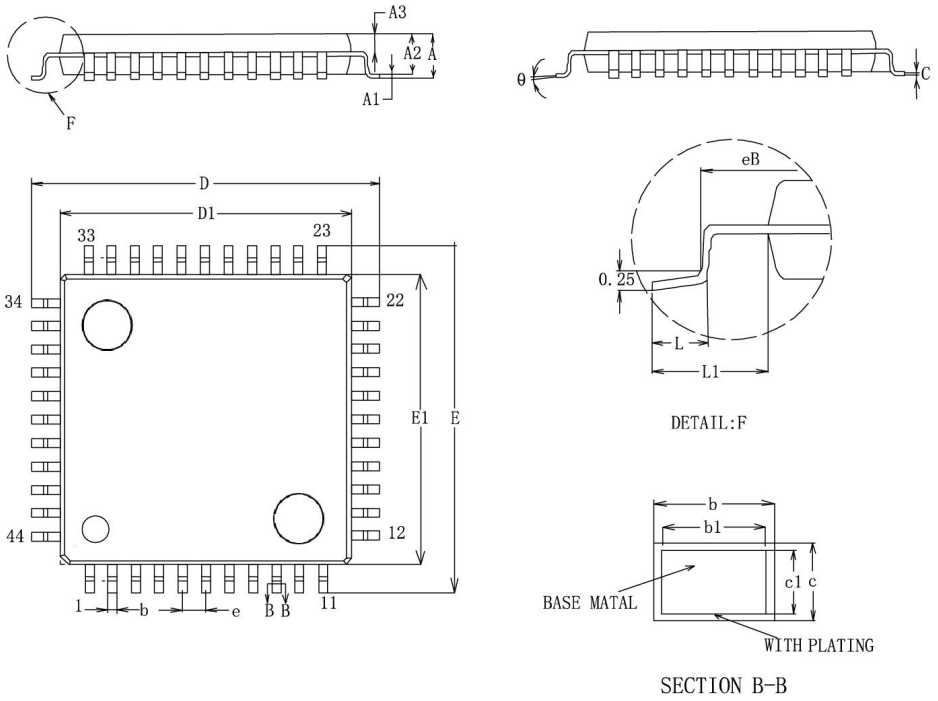
27.1 Package form:LQFP48(7x7mm)





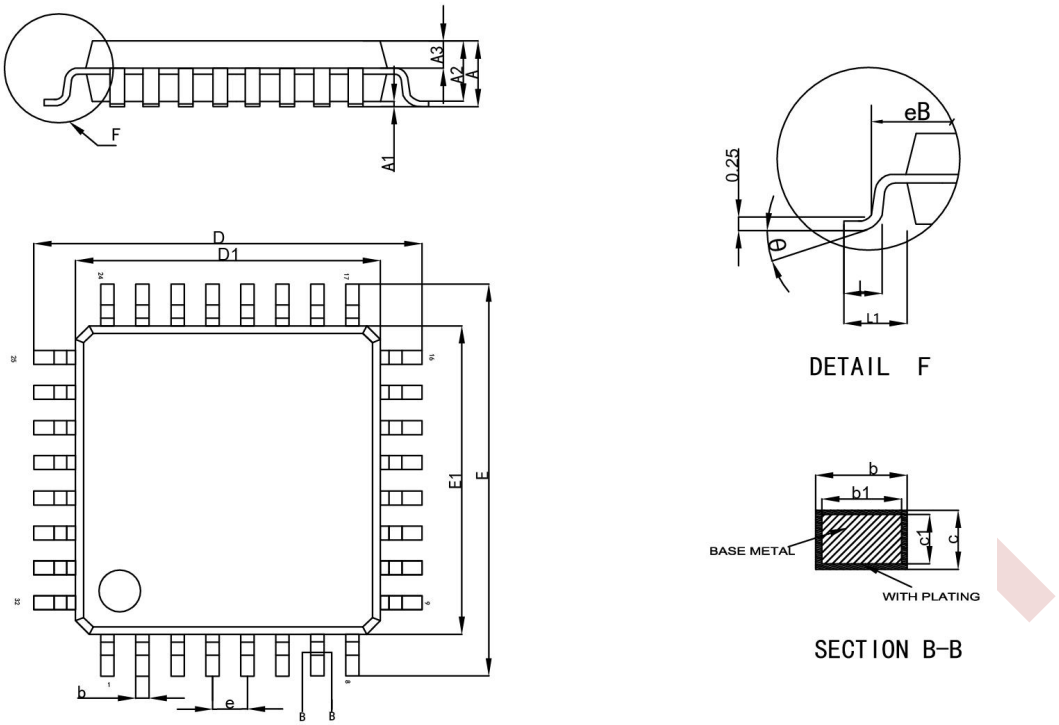
Serial number	Minimum value (mm)	Standard value (mm)	Maximum value (mm)
A	————	————	1.60
A1	0.05	————	0.15
A2	1.35	1.40	1.45
A3	0.59	0.54	0.69
b	0.18	————	0.27
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50		

27.2 Package form:LQFP44(10x10mm)



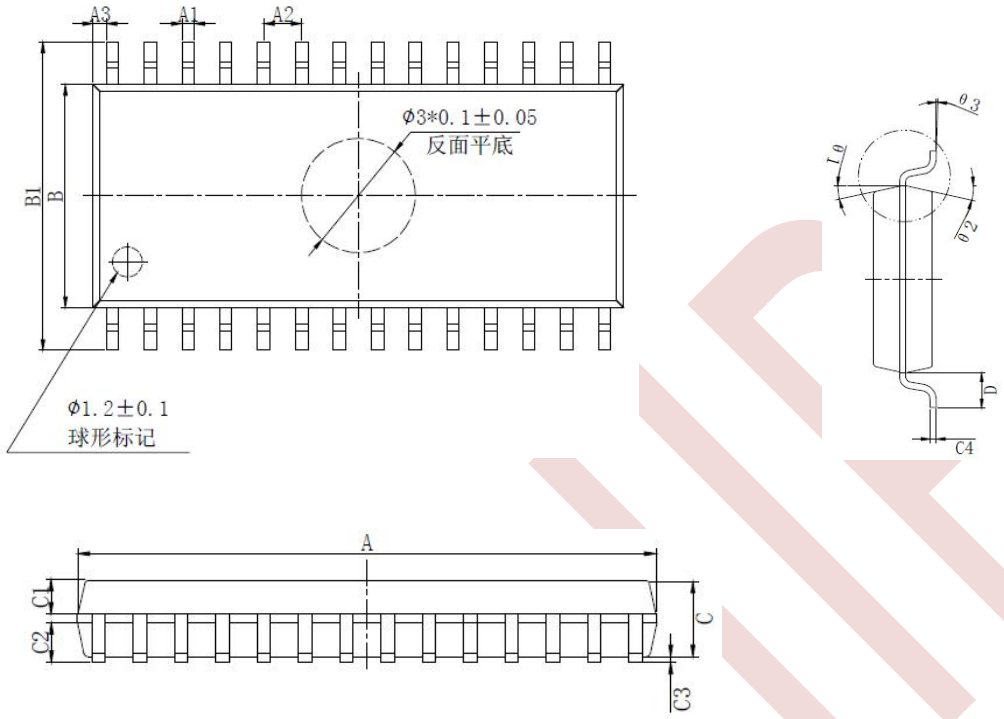
Serial number	Minimum value (mm)	Standard value (mm)	Maximum value (mm)
A	---	---	1.60
A1	0.05	---	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.28	---	0.36
b1	0.27	0.30	0.33
c	0.13	---	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.80BSC		
eB	11.05	---	11.25
L	0.45	---	0.75
L1	1.00REF		

27.3 Package form:LQFP32(7x7mm)



Serial number	Minimum value (mm)	Standard value (mm)	Maximum value (mm)
A	---	---	1.60
A1	0.05	---	0.15
A2	1.35	1.40	1.45
A3	0.60	---	0.65
b	0.33	0.35	0.38
c	0.13	---	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	---	8.25
e	0.80BSC		
L	0.40	---	0.65
L1	1.0REF		

27.4 Package form:SOP28



Serial number	Minimum value (mm)	Standard value (mm)	Maximum value (mm)
A	17.90	18.00	18.10
A1	0.356	0.40	0.456
A2	1.24	1.27	1.30
A3	---	0.542 TYP	---
B	7.40	7.50	7.60
B1	10.206	10.30	10.406
C	2.18	2.23	2.28
C1	0.938	1.0	1.038
C2	0.938	1.0	1.038
C3	0.03	0.09	0.17
D	1.353	1.40	1.453
C4	0.244	0.25	0.264

28 Appendix

Appendix 1 Instruction Set Quick Reference Table

Instruction	Description	Description	Periodicity
Data transfer command			
MOV A,Rn	The register contents are fed to the accumulator	(A) ← (Rn)	1
MOV A,direct	The data in the direct address cell is fed to the accumulator	(A) ← (direct)	1
MOV A,@Ri	Data from the indirect RAM is fed to the accumulator	(A) ← ((Ri))	1
MOV A,#data8	8-bit immediate number fed to accumulator	(A) ← #data	1
MOV Rn,A	The contents of the accumulator are fed into the register	(Rn) ← (A)	1
MOV Rn,direct	The data in the direct address cell is fed into the register	(Rn) ← (direct)	2
MOV Rn,#data8	8-bit immediate number sent to register	(Rn) ← #data	1
MOV direct,A	The contents of the accumulator are fed to the direct address unit	(direct) ← (A)	1
MOV direct,Rn	The register contents are fed to the direct address unit	(direct) ← (Rn)	2
MOV direct,direct	Data in the direct address unit is fed to the direct address unit	(direct) ← (direct)	2
MOV direct,@Ri	Data from the indirect RAM is fed to the direct address cell	(direct) ← ((Ri))	2
MOV direct,#data8	8-bit immediate number sent to direct address unit	(direct) ← #data	2
MOV @Ri,A	The contents of the accumulator are fed to the indirect RAM cell	((Ri)) ← (A)	1
MOV @Ri,direct	Data from the direct address cell is fed to the indirect RAM cell	((Ri)) ← (direct)	2
MOV @Ri,#data8	8-bit immediate number sent to indirect RAM cell	((Ri)) ← #data	1
MOV DPTR,#data16	16-bit immediate address fed into address register	(DPTR) ← #data116	2
MOV A,@A+DPTR	The data in the DPTR-based variable address addressing unit is fed to the accumulator	(A) ← ((A)) + (DPTR)	2
MOV A,@A+PC	The data in the PC-based address-variable addressing unit is fed to the accumulator	(PC) ← (PC) + 1 (A) ← ((A) + (PC))	2

MOVX A,@Ri	External RAM (8-bit address) is fed to the accumulator	(A) ← ((Ri))	2
MOVX A,@DPTR	External RAM (16-bit address) is fed to the accumulator	(A) ← ((DPTR))	2
MOVX @Ri,A	Accumulator feed to external RAM (8-bit address)	((Ri)) ← (A)	2
MOVX @DPTR,A	Accumulator feed to external RAM (16-bit address)	(DPTR) ← (A)	2
PUSH direct	Data in the direct address cell is pressed onto the stack	(SP) ← (SP) + 1 ((SP)) ← (direct)	2
POP DIRECT	Data in the stack is popped to the direct address unit	(direct) ← ((SP)) (SP) ← (SP) - 1	2
XCH A,Rn	Register and accumulator exchange	(A) ↔ (Rn)	1
XCH A,direct	Direct address unit exchange with accumulator	(A) ↔ (direct)	1
XCH A,@Ri	Indirect RAM to accumulator swap	(A) ↔ ((Ri))	1
XCHD A,@Ri	Indirect RAM with accumulator for low half-byte swap	(A.3,...,A.0) ↔ ((Ri).3,...,(Ri).0)	1
SWAP A	Accumulator half-byte swap	(A.3,...,A.0) ↔ (A.7,...,A.4)	1
Arithmetic operation class instruction			
ADD A, Rn	Register contents are added to the accumulator	(A) ← (A) + (Rn)	1
ADD A, direct	Direct address unit added to accumulator	(A) ← (A) + (direct)	1
ADD A, @Ri	Indirect RAM content added to accumulator	(A) ← (A) + ((Ri))	1
ADD A, #data8	8-bit immediate number added to accumulator	(A) ← (A) + #data	1
ADDC A, Rn	Register contents are added to the accumulator with rounding	(A) ← (A) + (C) + (Rn)	1
ADDC A, direct	Direct address unit with advance added to accumulator	(A) ← (A) + (C) + (direct)	1
ADDC A, @Ri	Indirect RAM content with rounding added to accumulator	(A) ← (A) + (C) + ((Ri))	1
ADDC A, #data8	8-bit immediate numbers with rounding added to accumulator	(A) ← (A) + (C) + #data	1
SUBB A, Rn	Accumulator with debit minus register content	(A) ← (A) - (C) - (Rn)	1
SUBB A, direct	Accumulator with debit minus direct address unit	(A) ← (A) - (C) - (direct)	1
SUBB A, @Ri	Accumulator with debit minus indirect RAM content	(A) ← (A) - (C) - ((Ri))	1

SUBB A, #data8	Accumulator with debit minus 8-bit immediate	(A) ← (A) - (C) - #data	1
INC A	Totalizer plus 1	(A) ← (A) + 1	1
INC Rn	Register plus 1	(Rn) ← (Rn) + 1	1
INC direct	Add 1 to the contents of the direct address unit	(direct) ← (direct) + 1	1
INC @Ri	Indirect RAM content plus 1	((Ri)) ← ((Ri)) + 1	1
INC DPTR	DPTR plus 1	(DPTR) ← (DPTR) + 1	2
DEC A	Totalizer minus 1	(A) ← (A) – 1	1
DEC Rn	Register minus 1	(Rn) ← (Rn) - 1	1
DEC direct	Direct address cell content minus 1	(direct) ← (direct) - 1	1
DEC @Ri	Indirect RAM content minus 1	((Ri)) ← ((Ri)) - 1	1
MUL AB	A multiplied by B	temp16 ← (A) X (B) (A)←(temp.7,temp.6,...,temp.0) (B)←(temp.15,temp.14,...,temp.8)	4
DIV AB	A divided by B	QUO ← (A) / (B) .....REM (A) ← QUO (B) ← REM	4

DA A	Accumulator for decimal conversion	IF (A.3,...,A.0) > 9 || AC = 1
		THEN
		temp16 ← (A) + 0x06
		(A) ← (temp.7,...,temp.0)
		
		IF (temp16) > 0xFF
		THEN
		CY ← 1
		
		IF (A.7,...,A.4) > 9 || CY = 1
		THEN
		temp16 ← (A) + 0x60
		(A) ←
			1

		(temp.7,...,temp.0) IF (temp16) > 0xFF THEN CY ← 1	
Logic operation class instruction			
ANL A, Rn	The accumulator is ANDed with the register	(A) ← (A) & (Rn)	1
ANL A, direct	The accumulator is ANDed with the direct address unit	(A) ← (A) & (direct)	1
ANL A, @Ri	The accumulator is ANDed with the indirect RAM content	(A) ← (A) & ((Ri))	1
ANL A, #data8	The accumulator is ANDed with 8-bit immediate data	(A) ← (A) & #data	1
ANL direct, A	The direct address unit and the accumulator are "AND''	(direct) ← (direct) & (A)	1
ANL direct, #data8	Direct address unit and 8-bit immediate data "AND"	(direct) ← (direct) & #data	2
ORL A, Rn	The accumulator is ORed with the register	(A) ← (A) | (Rn)	1
ORL A, direct	The accumulator is ORed with the direct address unit	(A) ← (A) | (direct)	1
ORL A, @Ri	Accumulator and indirect RAM content "OR"	(A) ← (A) | ((Ri))	1
ORL A, #data8	The accumulator is ORed with 8-bit immediate data	(A) ← (A) | #data	1
ORL direct, A	The direct address unit is ORed with the accumulator	(direct) ← (direct) | (A)	1
ORL direct, #data8	Direct address unit and 8-bit immediate data "OR"	(direct) ← (direct) | #data	2
XRL A, Rn	"Exclusive OR" between accumulator and register	(A) ← (A) ^ (Rn)	1
XRL A, direct	"Exclusive OR" between the accumulator and the direct address unit	(A) ← (A) ^ (direct)	1
XRL A, @Ri	"Exclusive OR" between the accumulator and the indirect RAM content	(A) ← (A) ^ ((Ri))	1
XRL A, #data8	"Exclusive OR" between accumulator and 8-bit immediate data	(A) ← (A) ^ #data	1
XRL direct, A	"Exclusive OR" between the direct address unit and the accumulator	(direct) ← (direct) ^ (A)	1
XRL direct, #data8	"Exclusive OR" between direct address unit and 8-bit immediate data	(direct) ← (direct) ^ #data	2
CLR A	Accumulator is cleared to 0	(A) ← 0	1
CPL A	Accumulator negation	(A) ← /(A)	1
RL A	Accumulator rotate left	(A) ←	1

		(A.6,A.5,...,A.0,A.7)	
RLC A	Accumulator rotates left with carry	C ← A.7 (A) ← (A.6,A.5,...,A.0,C)	1
RR A	The accumulator rotates right	(A) ← (A.0,A.7,...,A.2,A.1)	1
RRC A	Accumulator with carry cycle shift right	C ← A.0 (A) ← (C,A.7,...,A.2,A.1)	1
Control transfer instructions			
ACALL addr11	Absolute short call subroutine	(PC) ← (PC) + 2 (SP) ← (SP) + 1 ((SP)) ← (PC7-0) (SP) ← (SP) + 1 ((SP)) ← (PC15-8) (PC10-0) ← page address	2
LACLL addr16	Long call subroutine	(PC) ← (PC) + 3 (SP) ← (SP) + 1 ((SP)) ← (PC7-0) ((SP)) ← (PC15-8) (PC) ←addr15-0	2
RET	The subroutine returns	(PC15-8) ← ((SP)) (SP) ← (SP) - 1 (PC7-0) ← ((SP)) (SP) ← (SP) - 1	2
RETI	Interrupt return	(PC15-8) ← ((SP)) (SP) ← (SP) - 1 (PC7-0) ← ((SP)) (SP) ← (SP) - 1	2
AJMP addr11	Absolute short transfer	(PC) ← (PC) + 2 (PC10-0) ← page address	2
LJMP addr16	Long transfer	(PC) ← (PC) + 3 (SP) ← (SP) + 1 ((SP)) ← (PC7-0)	2

		(SP) ← (SP) + 1 ((SP)) ← (PC15-8) (PC10-0) ←addr15-0	
SJMP rel	Relative Transfer	(PC) ← (PC) + 2 (PC) ← (PC) + rel	2
JMP @A+DPTR	Indirect transfer relative to DPTR	(PC) ← (A) + (DPTR)	2
JZ rel	Accumulator for zero transfer	(PC) ← (PC) + 2 IF (A) = 0 THEN (PC) ← (PC) + rel	2
JNZ rel	Accumulator non-zero transfer	(PC) ← (PC) + 2 IF (A) <> 0 THEN (PC) ← (PC) + rel	2

CJNE A, direct, rel	Compare the accumulator with the direct address unit, transfer if not equal	(PC) ← (PC) + 3
		IF (A) <> (direct)
		THEN
		(PC) ← (PC) +
		relative offset
		IF (A) < (direct)
		THEN
		(C) ← 1
		ELSE
		(C) ← 0
			2

CJNE A, #data8, rel	Accumulator compares with 8-bit immediate numbers, transfer if unequal	(PC) ← (PC) + 3
		IF (A) <> data
		THEN
		(PC) ← (PC) +
		relative offset
		IF (A) < data
		THEN
		(C) ← 1
		ELSE
		(C) ← 0
			2

CJNE Rn, #data8, rel	Compare register with 8-bit immediate number, transfer if not equal	(PC) ← (PC) + 3 IF (Rn) <> data THEN (PC) ← (PC) +	2

		relative offset
		IF (Rn) < data
		THEN
		(C) ← 1
		ELSE
		(C) ← 0	

CJNE @Ri, #data8, rel	Indirect RAM unit, unequal transfer	(PC) ← (PC) + 3
		IF ((Ri)) <> data
		THEN
		(PC) ← (PC) +
		relative offset
		IF ((Ri)) < data
		THEN
		(C) ← 1
		ELSE
		(C) ← 0
			2

DJNZ Rn, rel	Register minus 1, non-zero transfer	(PC) ← (PC) + 2 (Rn) ← (Rn) - 1 IF (Rn) <> 0 THEN (PC) ← (PC) + rel	2
DJNZ direct, rel	Direct address unit minus 1, non-zero transfer	(PC) ← (PC) + 2 (direct) ← (direct) - 1 IF (direct) <> 0 THEN (PC) ← (PC) + rel	2
NOP	No operation	(PC) ← (PC) + 1	1
Boolean variable operation instructions			
CLR C	Clear carry bit	(C) ← 0	1
CLR bit	Clear direct address bit	(bit) ← 0	1
SETB C	Set carry bit	(C) ← 1	1
SETB bit	Direct address bit	(bit) ← 1	1
CPL C	Carry negation	(C) ← /(C)	1
CPL bit	Direct address bit negation	(bit) ← /(bit)	1
ANL C, bit	Carry bit and direct address bit phase "AND"	(C) ← (C) & (bit)	2
ANL C, /bit	Carry bit and the inverse code of the direct address bit are "ANDed"	(C) ← (C) & /(bit)	2
ORL C, bit	Carry bit and direct address bit phase "OR"	(C) ← (C) | (bit)	2
ORL C, /bit	Carry bit and the inverse code of the direct address bit are ORed	(C) ← (C) | /(bit)	2
MOV C, bit	Direct address bit into carry bit	(C) ← (bit)	1

MOV bit, C	Carry bit into direct address bit	(bit) ← (C)	2
JC rel	If the carry bit is 1, then transfer (CY=O does not transfer, =1 transfer)	(PC) ← (PC) + 2 IF (C) = 1 THEN (PC) ← (PC) + rel	2
JNC rel	If the carry bit is 0, then branch	(PC) ← (PC) + 2 IF (C) = 0 THEN (PC) ← (PC) + rel	2
JB bit, rel	Direct address bit is 1, then transfer	(PC) ← (PC) + 3 IF (bit) = 1 THEN (PC) ← (PC) + rel	2
JNB bit, rel	Direct address bit is 0 then transfer	(PC) ← (PC) + 3 IF (bit) = 0 THEN (PC) ← (PC) + rel	2
JBC bit, rel	If the direct address bit is 1, it will be transferred, and the bit will be cleared.	(PC) ← (PC) + 3 IF (bit) = 1 THEN (bit) ← 0 (PC) ← (PC) + rel	2

Pseudo-instruction	
ORG	Set program start address
END	Mark the end of source code
EQU	Define constant
SET	Define an integer number
DATA	Set value for data address
BYTE	Assign value to byte type symbol
WROD	Assign value to word type symbol
BIT	Name the bit address
ALTNAME	Replace reserved words with custom names
DB	Load byte data into a continuous storage area
DW	Load font data to a continuous memory area
DS	Reserve a continuous storage area or load the specified byte
INCLUDE	Insert a source file into the program
TITLE	Add a header row to the list file
NOLIST	No list file is generated during assembly
NOCODE	When the condition is assembled, the list is not generated if the condition is false