

NCE N-Channel Super Trench Power MOSFET

Description

The NCEP60T18 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

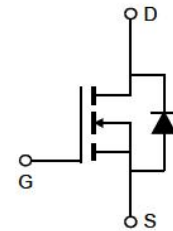
General Features

- $V_{DS} = 60V, I_D = 180A$
 $R_{DS(ON)} < 3.2m\Omega @ V_{GS}=10V$ (Typ:2.8m Ω)
- Excellent gate charge x $R_{DS(on)}$ product
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

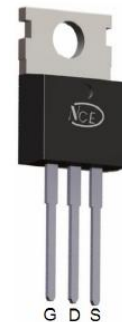
100% UIS TESTED!
100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment



TO-220-3L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP60T18	NCEP60T18	TO-220-3L	-	-	-

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Silicon Limited)	I_D	180	A
Drain Current-Continuous($T_C=100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	126	A
Pulsed Drain Current	I_{DM}	720	A
Maximum Power Dissipation	P_D	220	W
Derating factor		1.47	W/ $^\circ\text{C}$
Single pulse avalanche energy (Note 1)	E_{AS}	1036	mJ
Drain Source voltage slope, $V_{DS} \leq 48V$,	dv/dt	50	V/ns
Reverse diode dv/dt , $V_{DS} \leq 48V$, $I_{SD} < I_D$	dv/dt	15	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.68	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

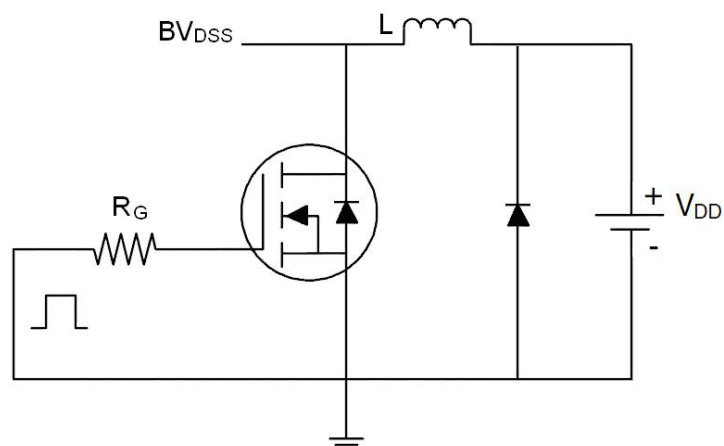
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0	3.0	4.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =40A	-	2.8	3.2	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =40A	50	-	-	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, F=1.0MHz	-	4500	-	PF
Output Capacitance	C _{oss}		-	965	-	PF
Reverse Transfer Capacitance	C _{rss}		-	24.2	-	PF
Switching Characteristics (Note 2)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, I _D =40A V _{GS} =10V, R _G =4.7Ω	-	6	-	nS
Turn-on Rise Time	t _r		-	11	-	nS
Turn-Off Delay Time	t _{d(off)}		-	23	-	nS
Turn-Off Fall Time	t _f		-	3	-	nS
Total Gate Charge	Q _g	V _{DS} =30V, I _D =40A, V _{GS} =10V	-	70	-	nC
Gate-Source Charge	Q _{gs}		-	18.6	-	nC
Gate-Drain Charge	Q _{gd}		-	15.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =40A	-		1.2	V
Diode Forward Current	I _S		-	-	180	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S	-	50		nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs	-	66		nC

Notes:

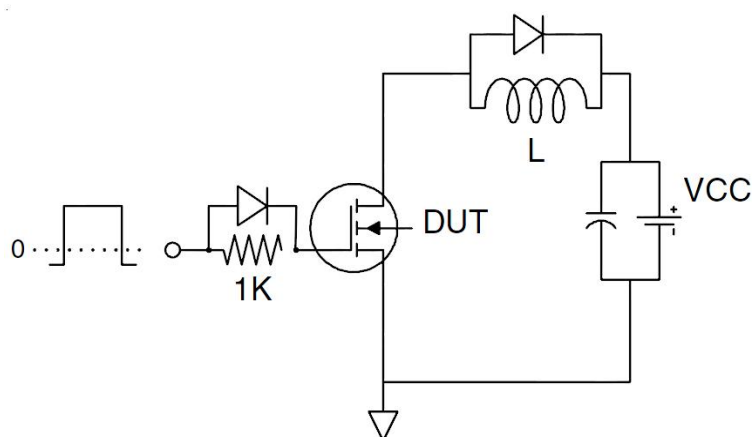
1. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=30V, V_G=10V, L=0.5mH, R_g=25\Omega$
2. Guaranteed by design, not subject to production.
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_J(MAX)=175^{\circ}\text{C}$. The SOA curve provides a single pulse rating.

Test Circuit

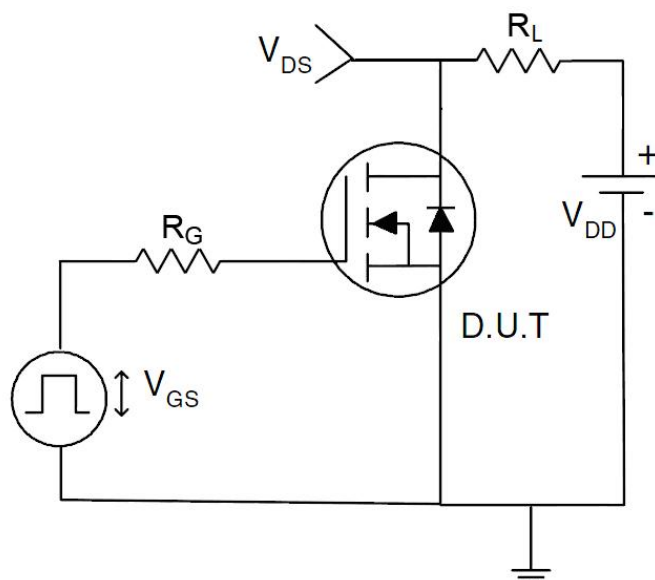
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

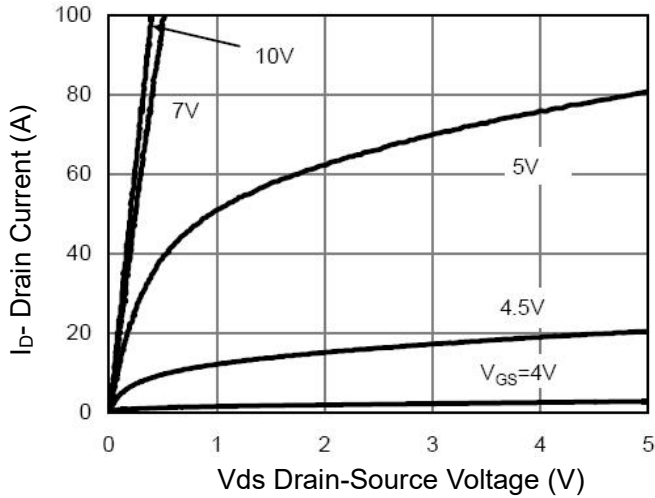


Figure 1 Output Characteristics

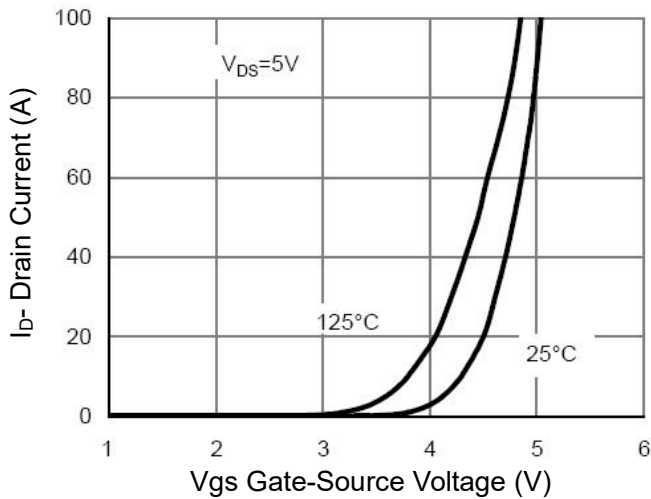


Figure 2 Transfer Characteristics

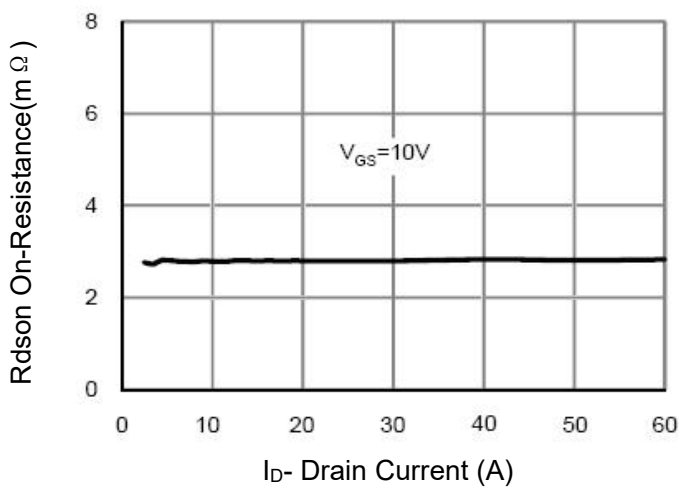


Figure 3 $R_{DS(on)}$ - Drain Current

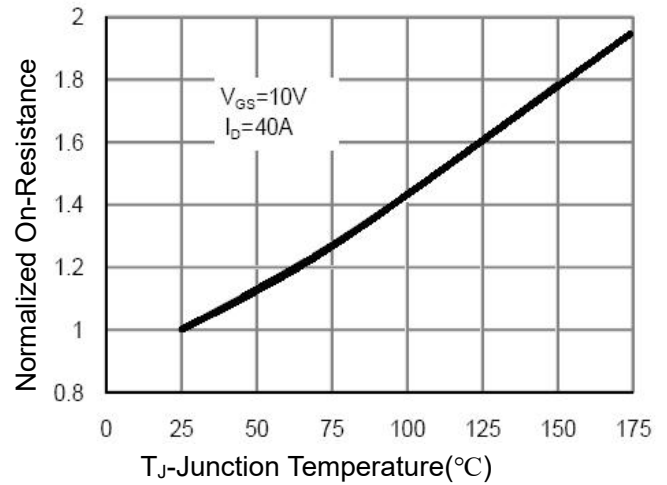


Figure 4 $R_{DS(on)}$ -Junction Temperature

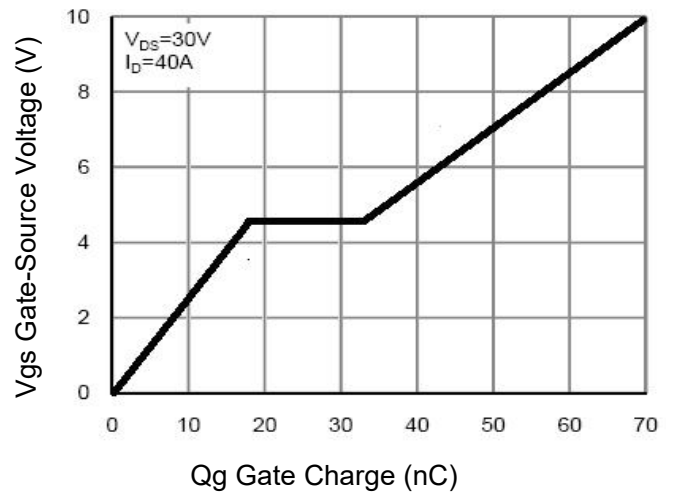


Figure 5 Gate Charge

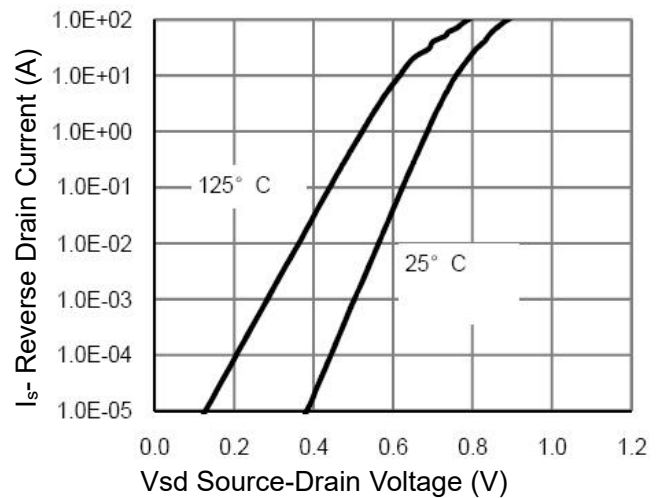


Figure 6 Source- Drain Diode Forward

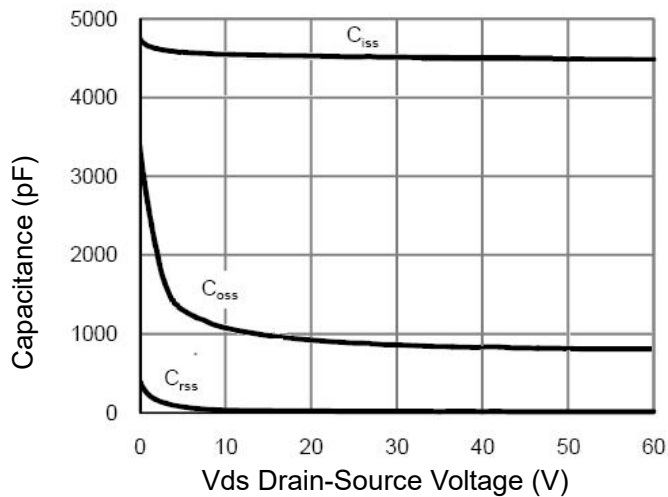


Figure 7 Capacitance vs Vds

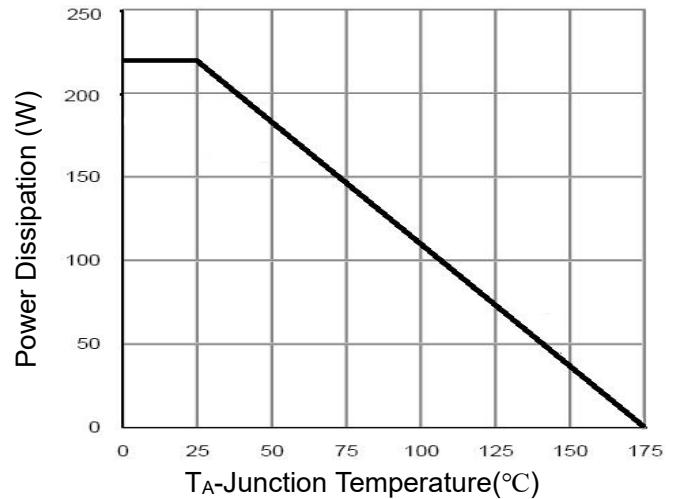


Figure 9 Power De-rating

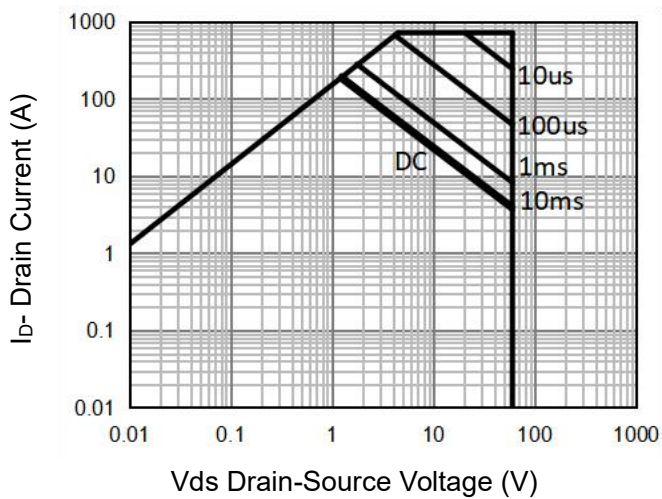


Figure 8 Safe Operation Area (Note 3)

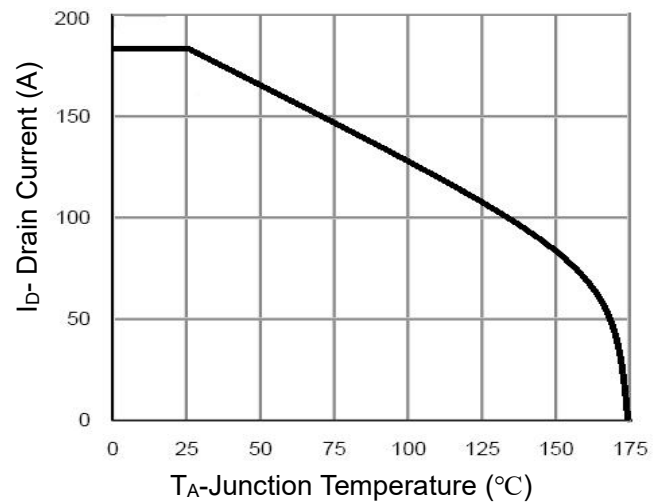


Figure 10 Current De-rating

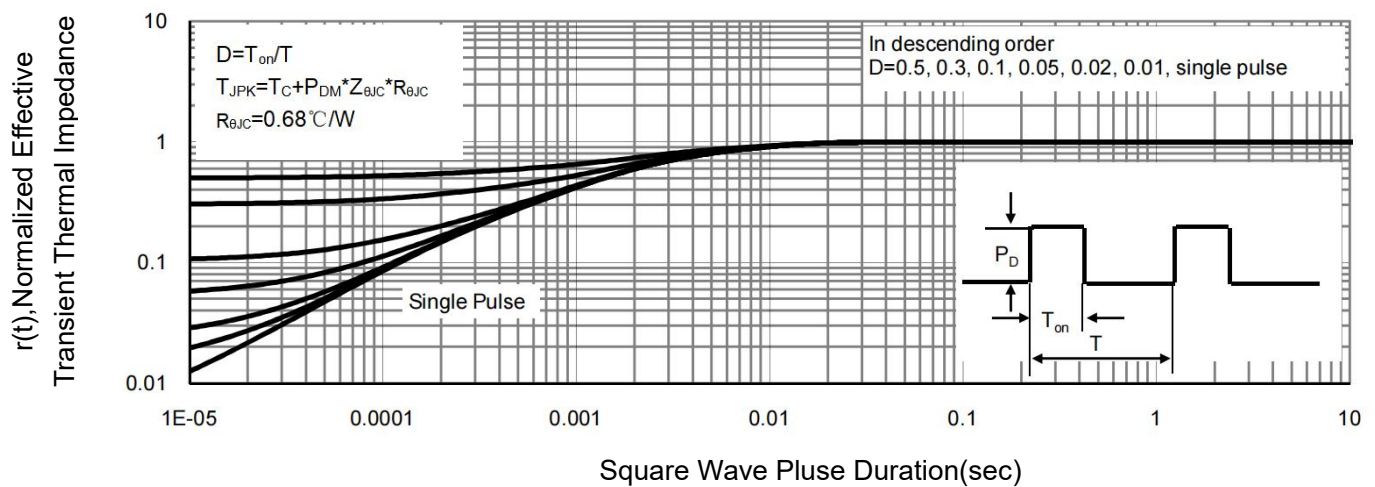
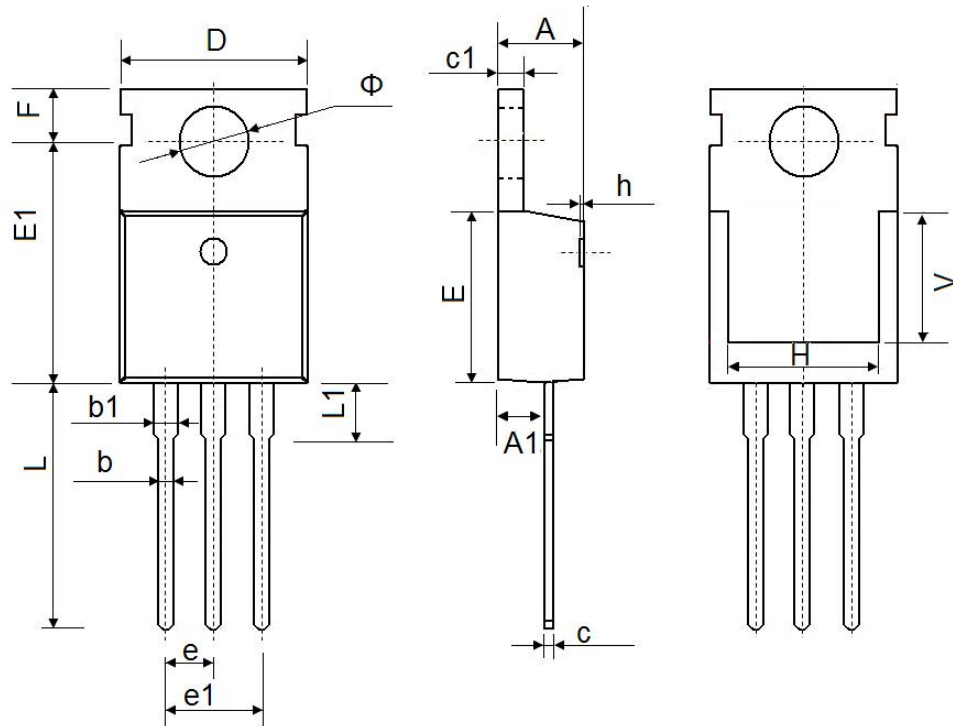


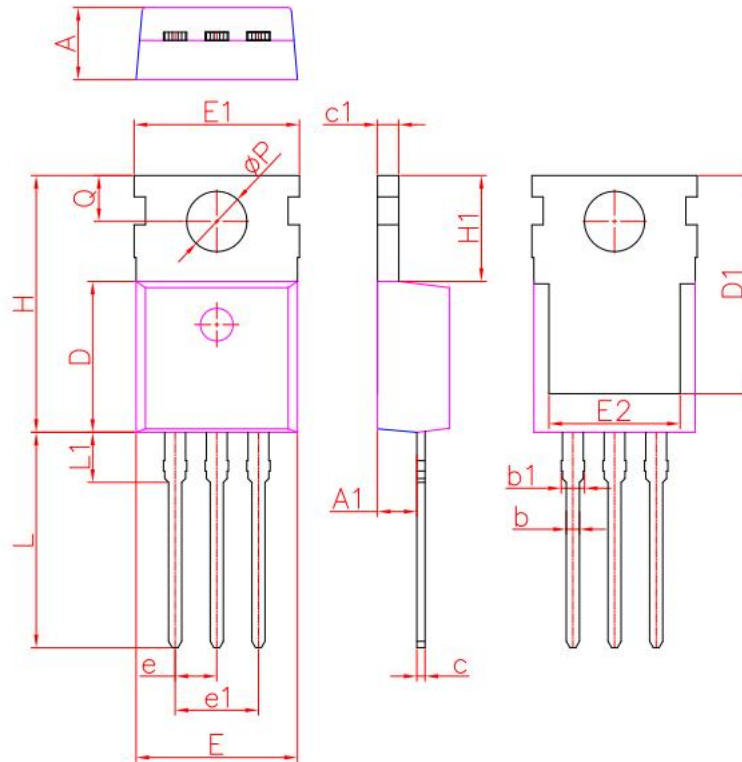
Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220-3L(C) Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150

TO-220-3L(E) Package Information



TO220			
DIM.	MIN.	NOM.	MAX.
A	4.20	4.40	4.60
A1	2.25	2.40	2.55
b	0.70	0.80	0.90
b1	1.17	1.27	1.37
c	0.33	0.50	0.65
c1	1.20	1.30	1.40
D	8.95	9.20	9.75
D1	13.10	13.30	13.50
E	9.74	9.84	10.04
E1	9.91	10.08	10.25
E2	7.90	8.00	8.10
e	2.54BSC		
e1	5.08BSC		
H	15.45	15.65	15.85
H1	6.30	6.45	6.60
L	12.90	13.13	13.40
L1	2.85	3.05	3.25
Q	2.65	2.80	2.95
ϕP	3.40	3.68	3.80
All dimensions in millimeters			

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