

NCE N-Channel Super Trench Power MOSFET

Description

The NCEP1250AK uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

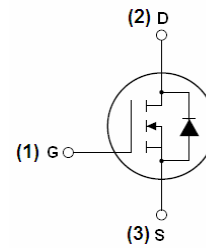
General Features

- $V_{DS} = 120V, I_D = 50A$
 $R_{DS(ON)} = 8.8m\Omega$ (typical) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 10.7m\Omega$ (typical) @ $V_{GS} = 4.5V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

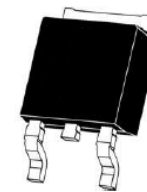
100% UIS TESTED!



Schematic diagram



Marking and pin assignment



TO-252 -2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP1250AK	NCEP1250AK	TO-252-2L	-	-	-

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	120	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	50	A
Drain Current-Continuous($T_C = 100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	35.3	A
Pulsed Drain Current	I_{DM}	200	A
Maximum Power Dissipation	P_D	105	W
Derating factor		0.7	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	210	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.42	$^\circ\text{C/W}$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

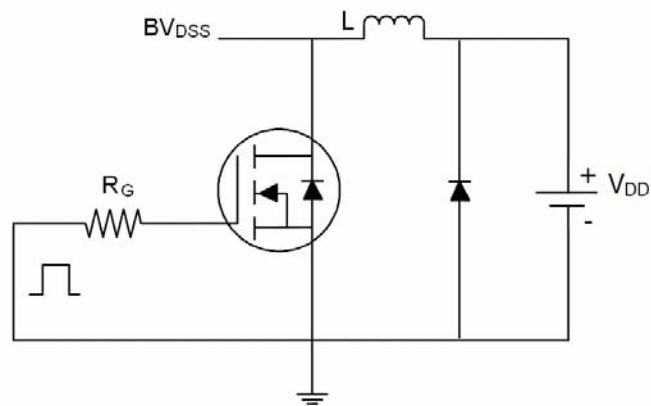
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	120	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =120V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.7	2.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	8.8	10.1	mΩ
		V _{GS} =4.5V, I _D =20A	-	10.7	13.9	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =20A	-	30	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{iss}	V _{DS} =60V, V _{GS} =0V, F=1.0MHz	-	3050	-	PF
Output Capacitance	C _{oss}		-	274	-	PF
Reverse Transfer Capacitance	C _{rss}		-	17.8	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =60V, I _D =20A V _{GS} =10V, R _G =1.6Ω	-	11	-	nS
Turn-on Rise Time	t _r		-	7	-	nS
Turn-Off Delay Time	t _{d(off)}		-	30	-	nS
Turn-Off Fall Time	t _f		-	4	-	nS
Total Gate Charge	Q _g	V _{DS} =60V, I _D =20A, V _{GS} =10V	-	45	-	nC
Gate-Source Charge	Q _{gs}		-	11.6	-	nC
Gate-Drain Charge	Q _{gd}		-	6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =20A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	20	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S di/dt = 100A/μs ^(Note3)	-	78	-	nS
Reverse Recovery Charge	Q _{rr}		-	149	-	nC

Notes:

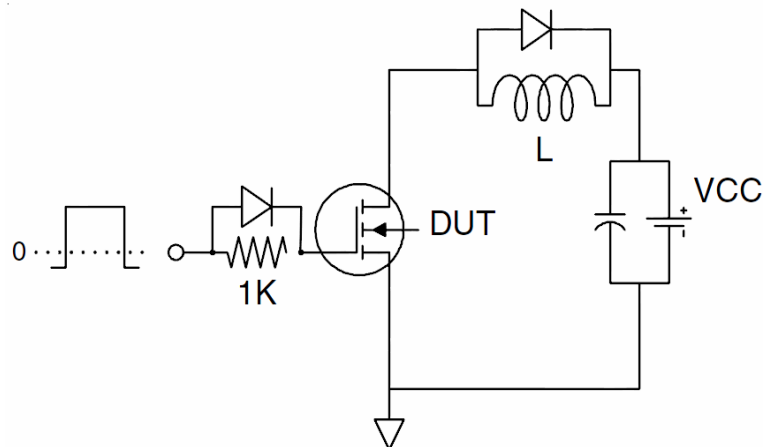
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

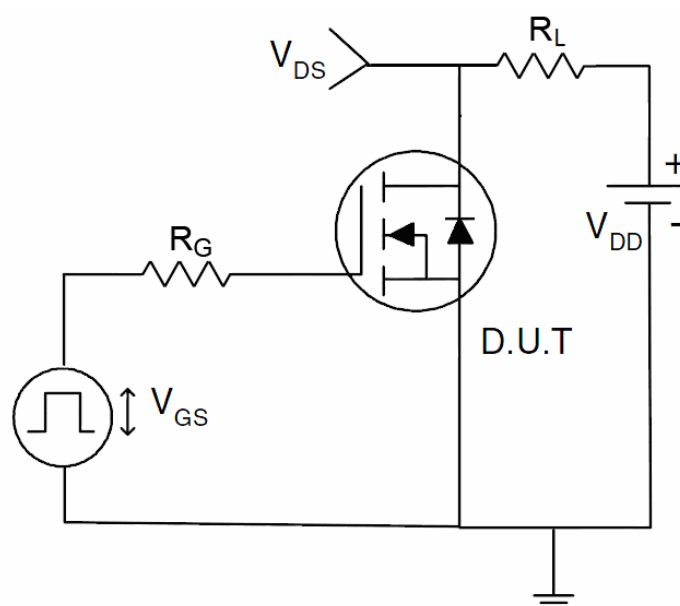
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

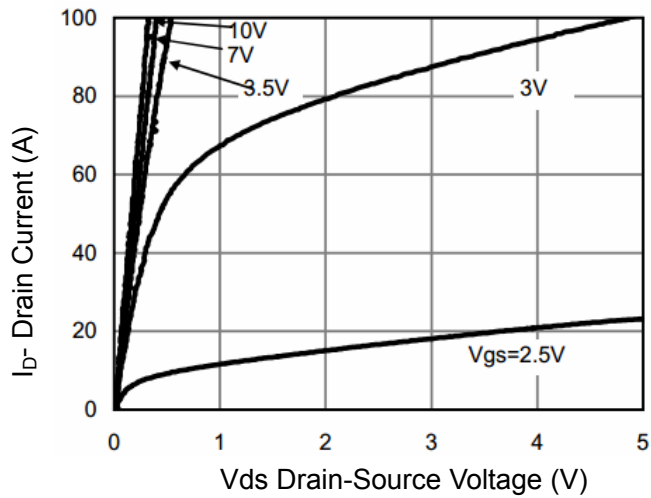


Figure 1 Output Characteristics

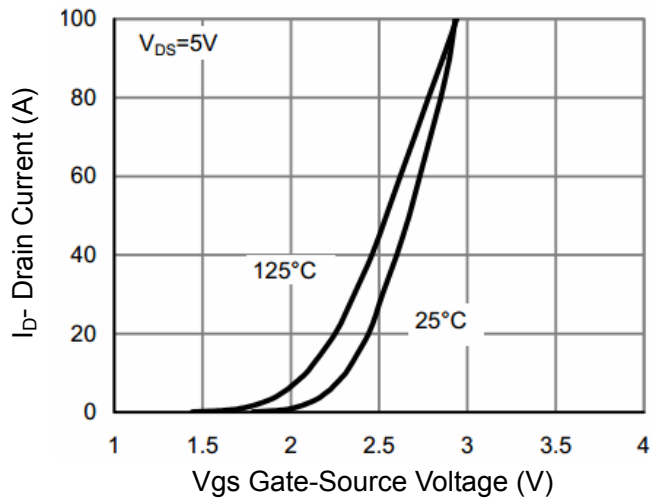


Figure 2 Transfer Characteristics

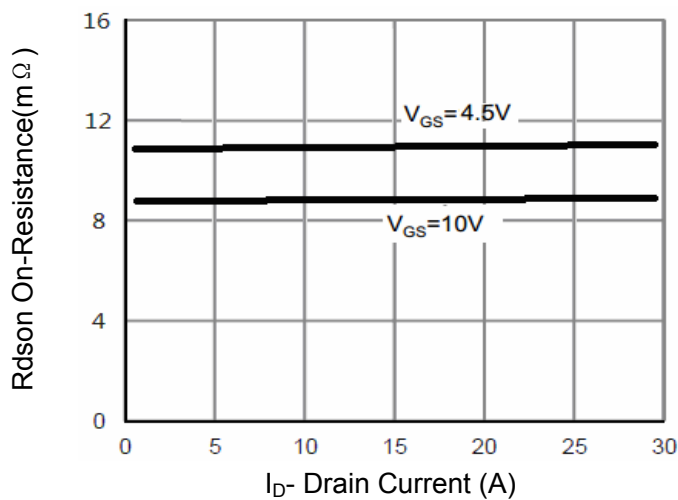


Figure 3 $R_{DS(on)}$ - Drain Current

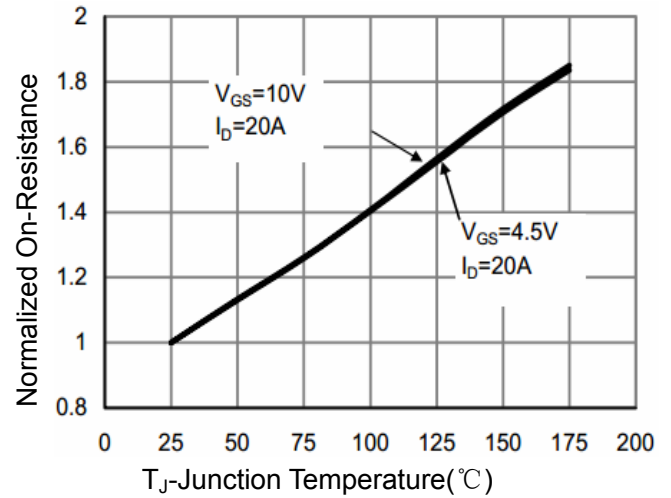


Figure 4 $R_{DS(on)}$ -Junction Temperature

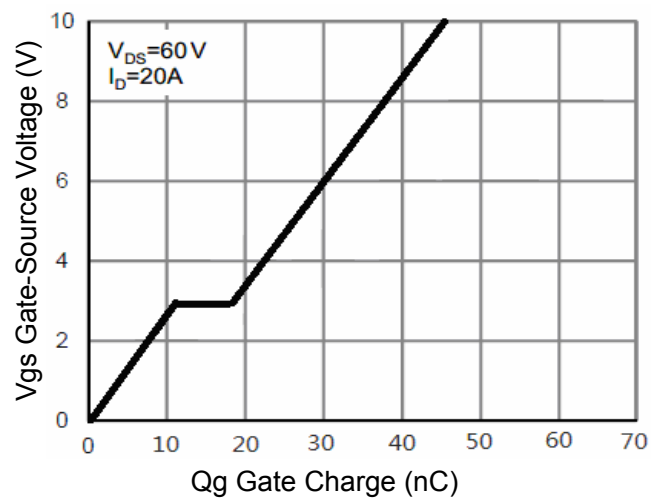


Figure 5 Gate Charge

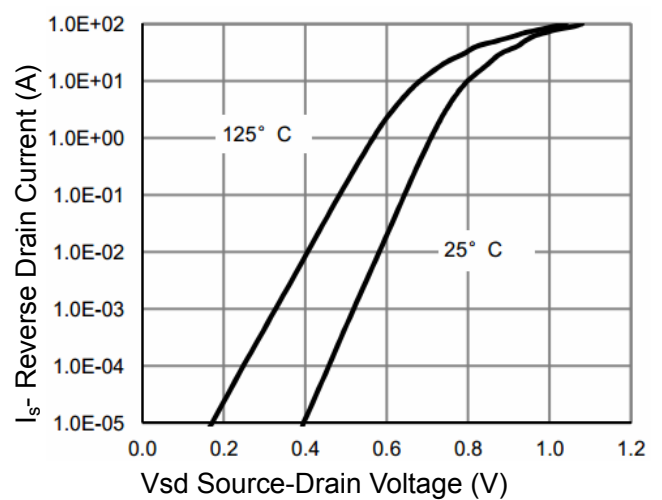


Figure 6 Source- Drain Diode Forward

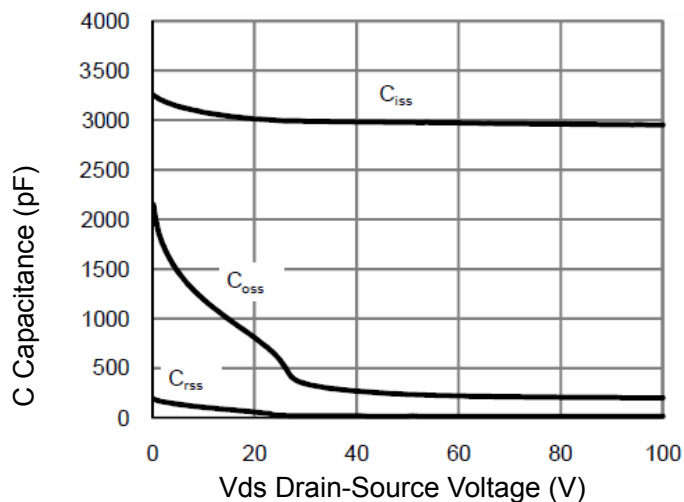


Figure 7 Capacitance vs Vds

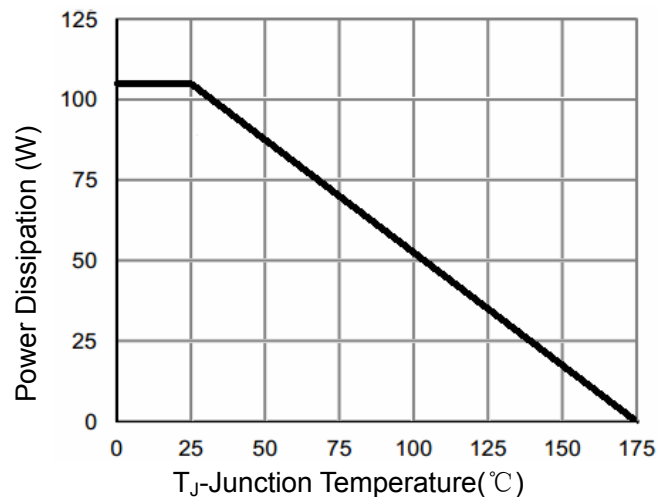


Figure 9 Power De-rating

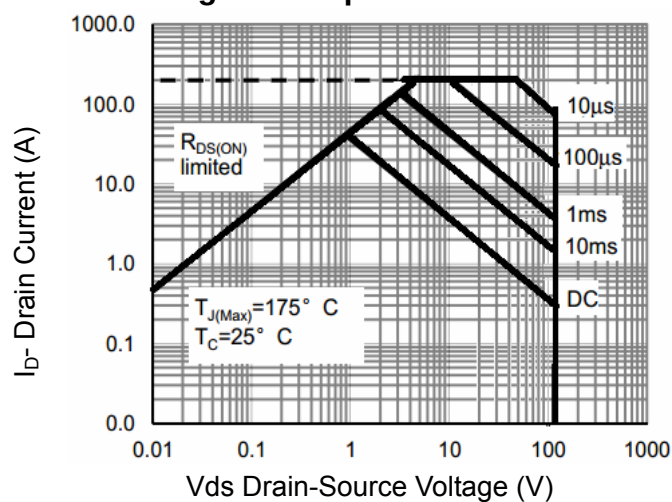


Figure 8 Safe Operation Area

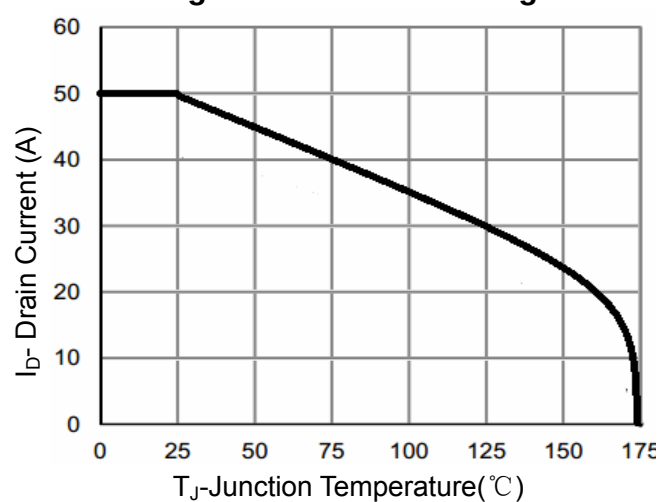


Figure 10 Current De-rating

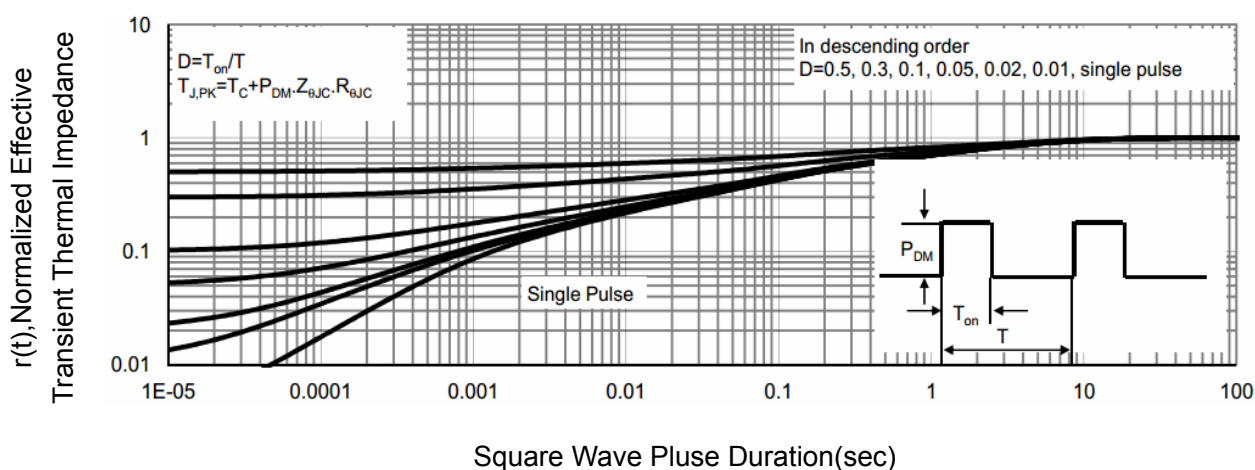
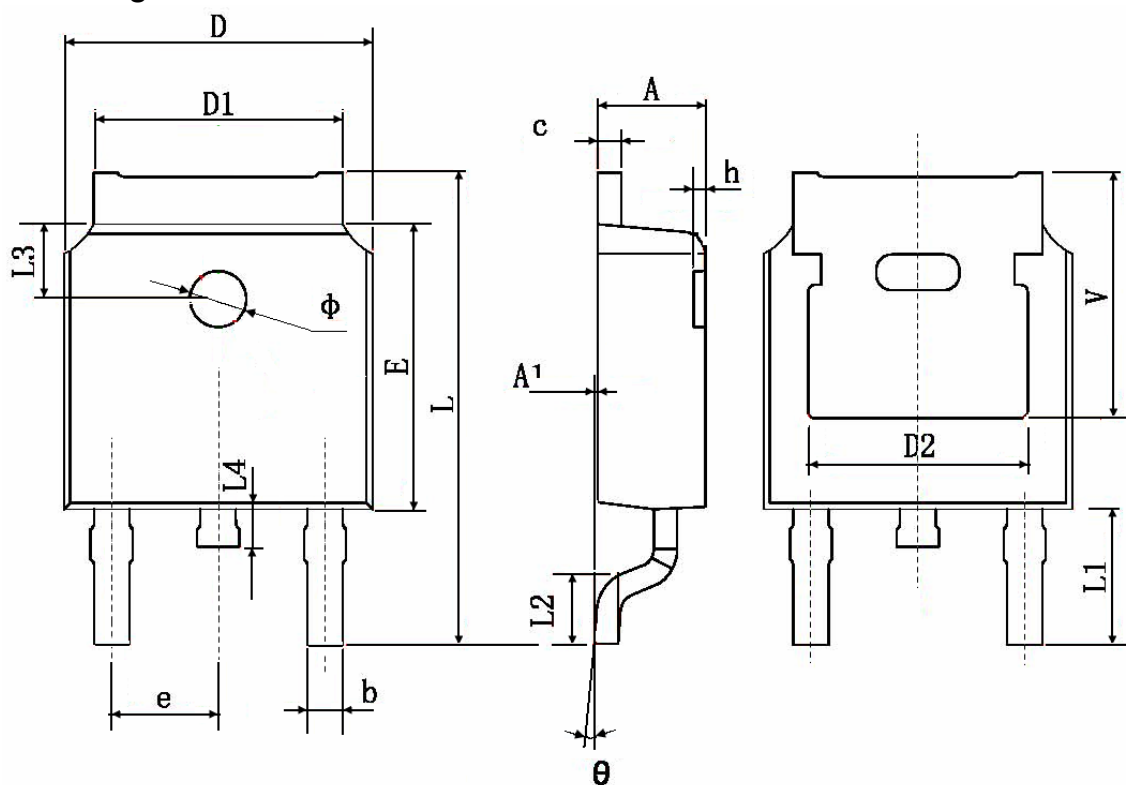


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252-2L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.83 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
phi	1.100	1.300	0.043	0.051
theta	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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