

NCE N-Channel Super Trench Power MOSFET

Description

The NCEP02T11D uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

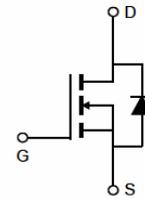
General Features

- $V_{DS} = 200V, I_D = 110A$
 $R_{DS(ON)} < 10.5m\Omega @ V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

100% UIS TESTED!
100% ΔV_d s TESTED!



Schematic diagram



Marking and pin assignment



TO-263-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP02T11D	NCEP02T11D	TO-263-2L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	110	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	77.7	A
Pulsed Drain Current	I_{DM}	440	A
Maximum Power Dissipation	P_D	330	W
Derating factor		2.2	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	2000	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.45	$^\circ C/W$
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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

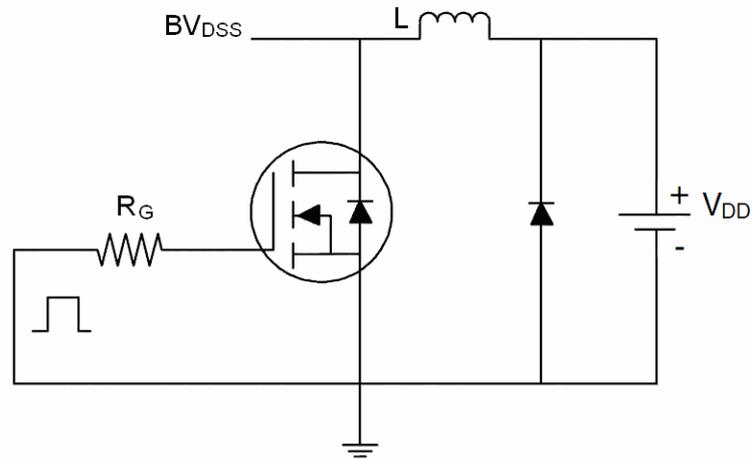
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	200		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=200V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5		4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=55A$	-	9.4	10.5	m Ω
Gate resistance	R_G		-	3.8	-	Ω
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=55A$	70	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=100V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	6635	-	PF
Output Capacitance	C_{oss}		-	450.6	-	PF
Reverse Transfer Capacitance	C_{rss}		-	11	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=100V, I_D=55A$ $V_{GS}=10V, R_G=4.7\Omega$	-	19.5	-	nS
Turn-on Rise Time	t_r		-	28	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	48	-	nS
Turn-Off Fall Time	t_f		-	15	-	nS
Total Gate Charge	Q_g	$V_{DS}=100V, I_D=55A,$ $V_{GS}=10V$	-	89.5		nC
Gate-Source Charge	Q_{gs}		-	40.5		nC
Gate-Drain Charge	Q_{gd}		-	15.7		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=110A$	-		1.2	V
Diode Forward Current	I_S		-	-	110	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = 55A$ $di/dt = 100A/\mu\text{s}$ (Note 3)	-	184		nS
Reverse Recovery Charge	Q_{rr}		-	1.96		μC

Notes:

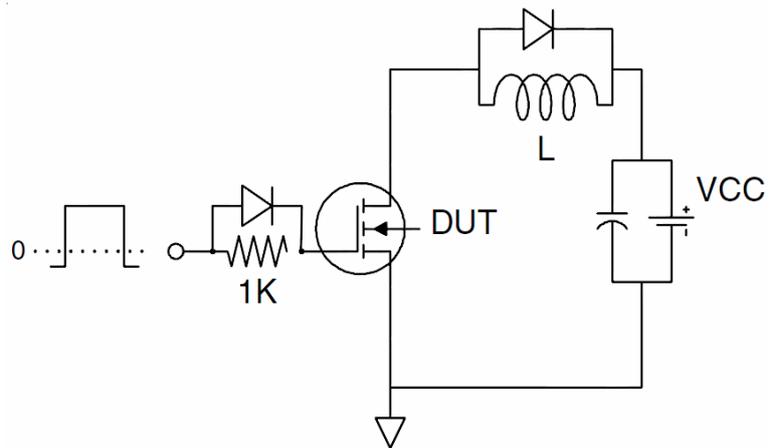
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_G=25\Omega$

Test Circuit

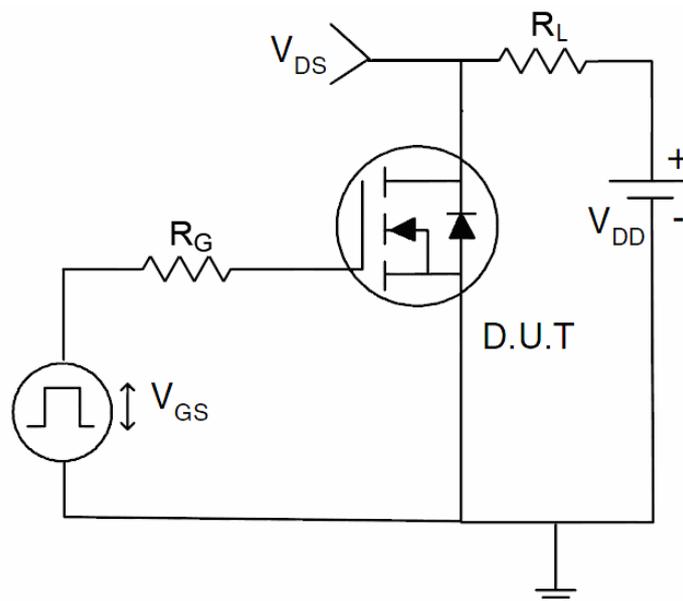
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

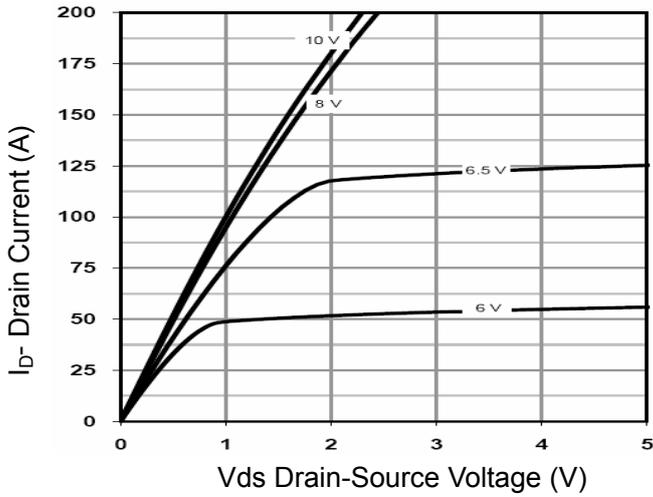


Figure 1 Output Characteristics

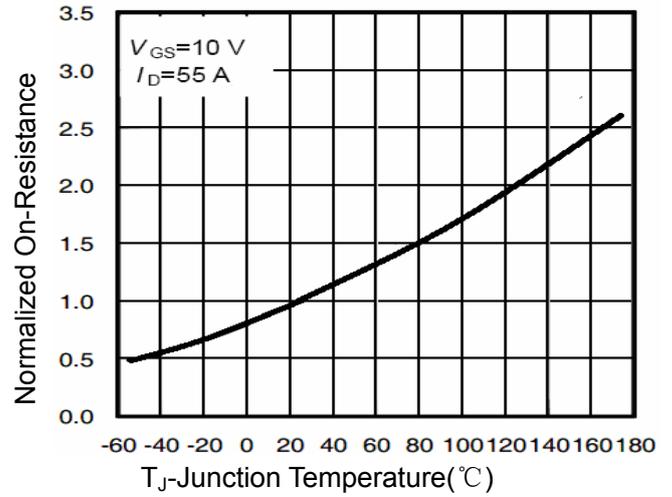


Figure 4 R_{dson} -Junction Temperature

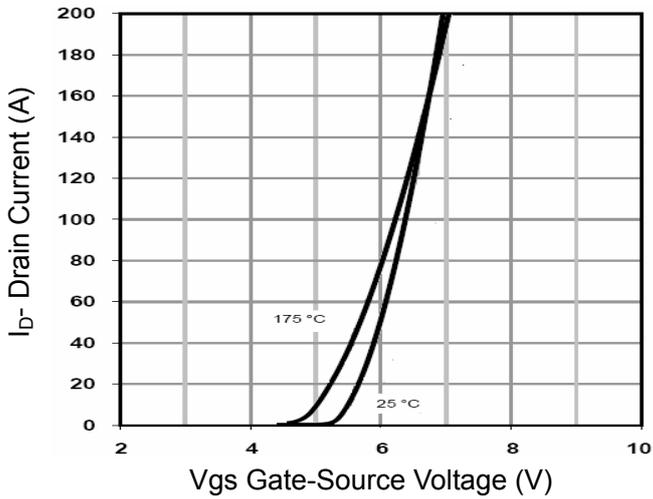


Figure 2 Transfer Characteristics

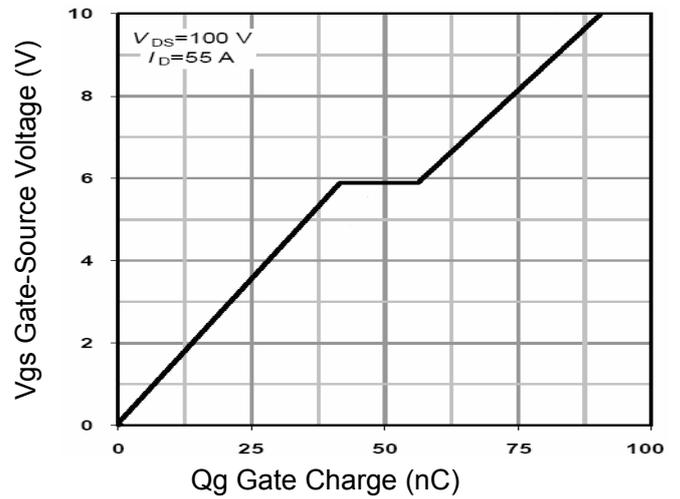


Figure 5 Gate Charge

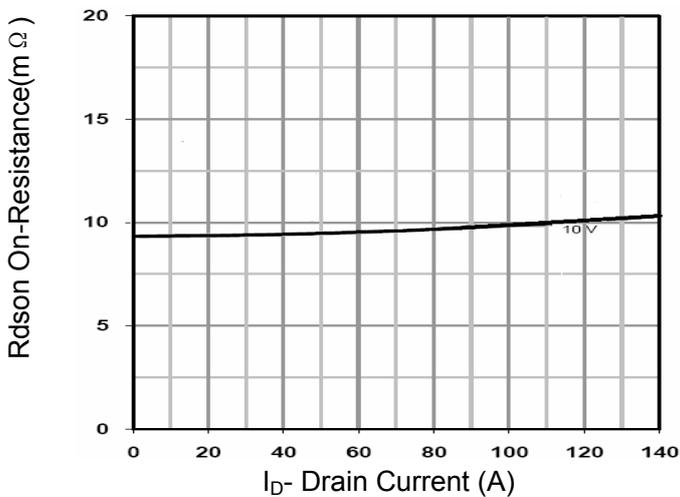


Figure 3 R_{dson} - Drain Current

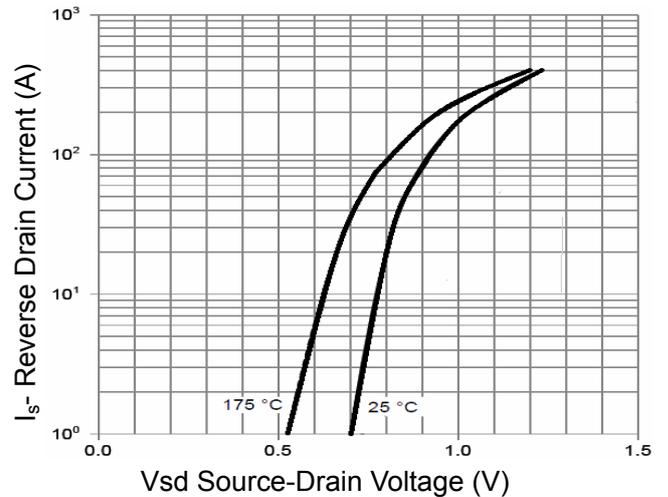


Figure 6 Source- Drain Diode Forward

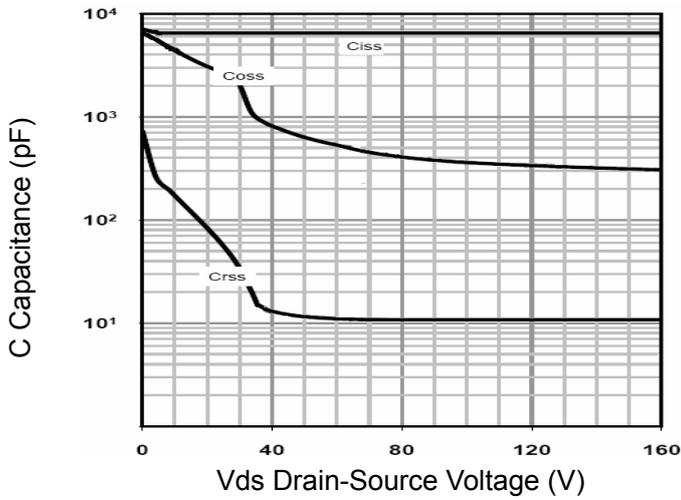


Figure 7 Capacitance vs Vds

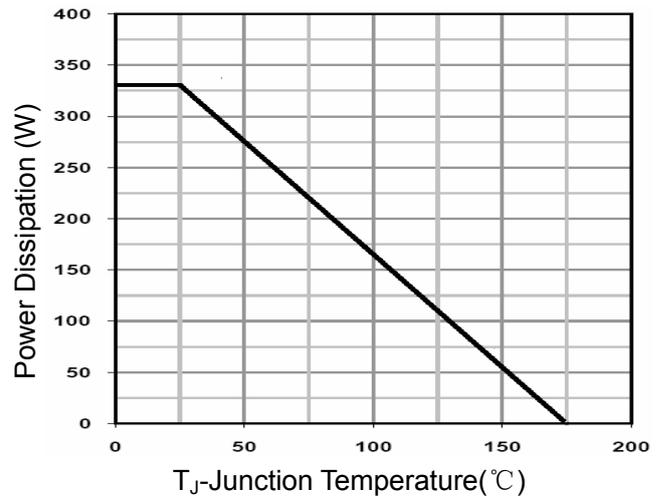


Figure 9 Power De-rating

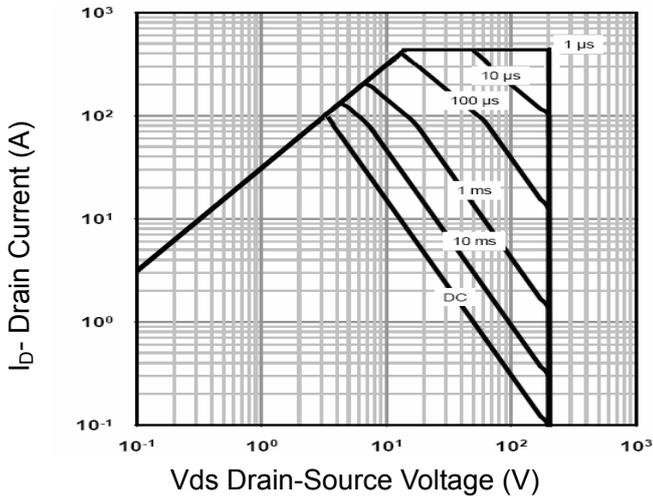


Figure 8 Safe Operation Area

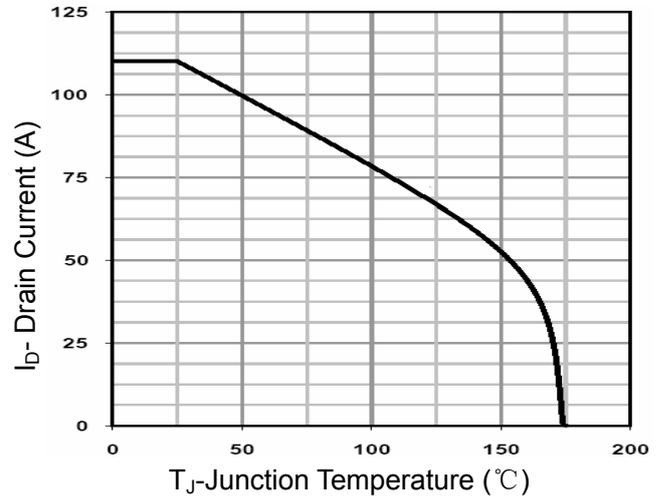


Figure 10 Current De-rating

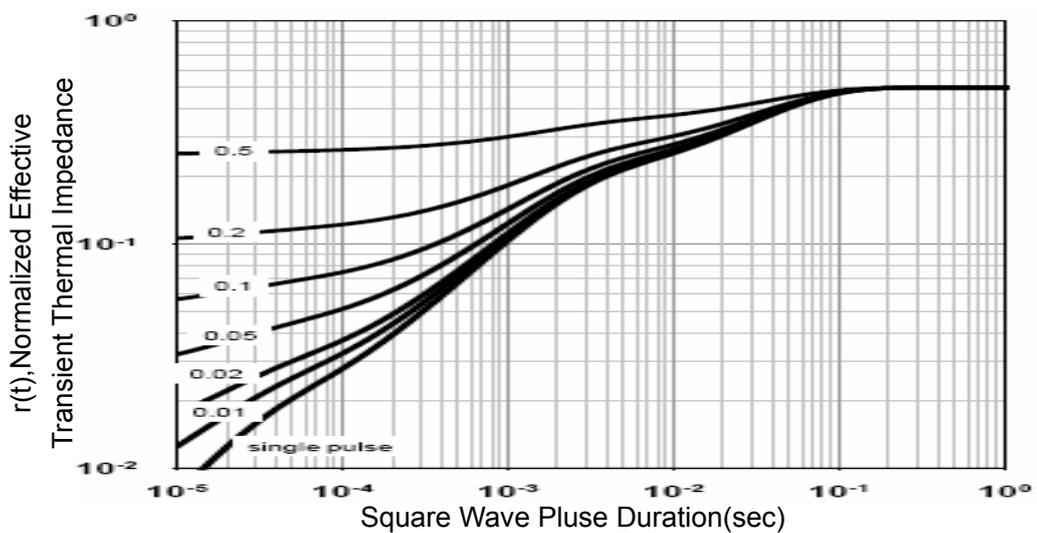
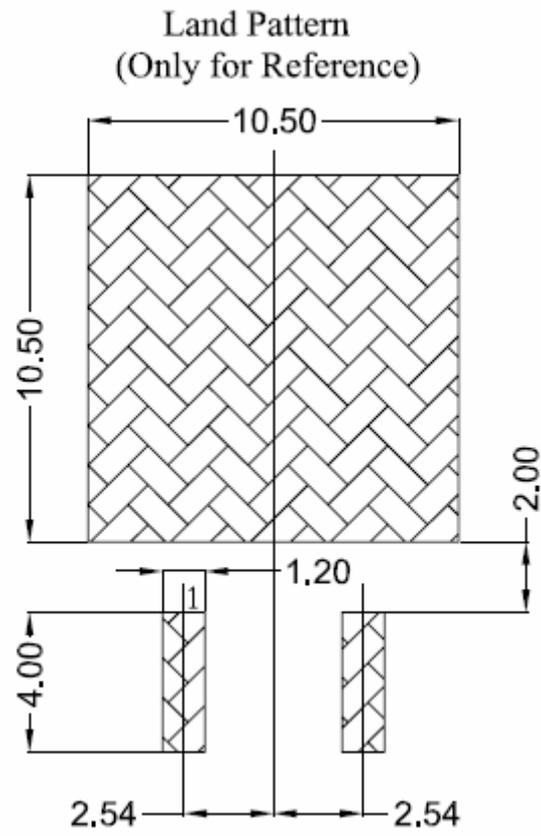


Figure 11 Normalized Maximum Transient Thermal Impedance



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