

NCE N-Channel Super Trench Power MOSFET

Description

The NCEP02T10D uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(on)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

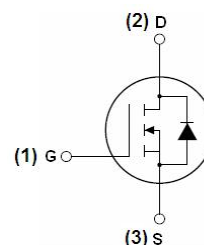
- $V_{DS} = 200V, I_D = 100A$
 $R_{DS(on)} < 12m\Omega @ V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

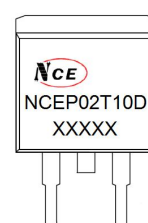
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment



TO-263-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP02T10D	NCEP02T10D	TO-263-2L	-	-	-

Absolute Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	100	A
Drain Current-Continuous($T_c = 100^\circ\text{C}$)	$I_D (100^\circ\text{C})$	70.7	A
Pulsed Drain Current	I_{DM}	400	A
Maximum Power Dissipation	P_D	300	W
Derating factor		2	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 1)	E_{AS}	1216	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.5	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

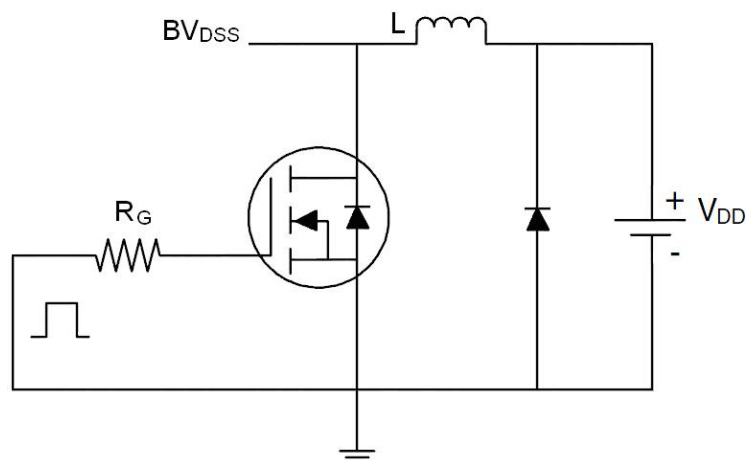
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	200	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =200V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.5		4.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =50A	-	10	12	mΩ
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =50A	70	-	-	S
Dynamic Characteristics						
Input Capacitance	C _{ISS}	V _{DS} =100V, V _{GS} =0V, F=1.0MHz	-	6000	-	PF
Output Capacitance	C _{OSS}		-	425	-	PF
Reverse Transfer Capacitance	C _{RSS}		-	16	-	PF
Switching Characteristics (Note 2)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =100V, I _D =50A V _{GS} =10V, R _G =4.7Ω	-	18	-	nS
Turn-on Rise Time	t _r		-	26	-	nS
Turn-Off Delay Time	t _{d(off)}		-	41	-	nS
Turn-Off Fall Time	t _f		-	11	-	nS
Total Gate Charge	Q _g	V _{DS} =100V, I _D =50A, V _{GS} =10V	-	87		nC
Gate-Source Charge	Q _{gs}		-	32		nC
Gate-Drain Charge	Q _{gd}		-	17.5		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =100A	-		1.2	V
Diode Forward Current	I _S		-	-	100	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 50A	-	140		nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs	-	600		nC

Notes:

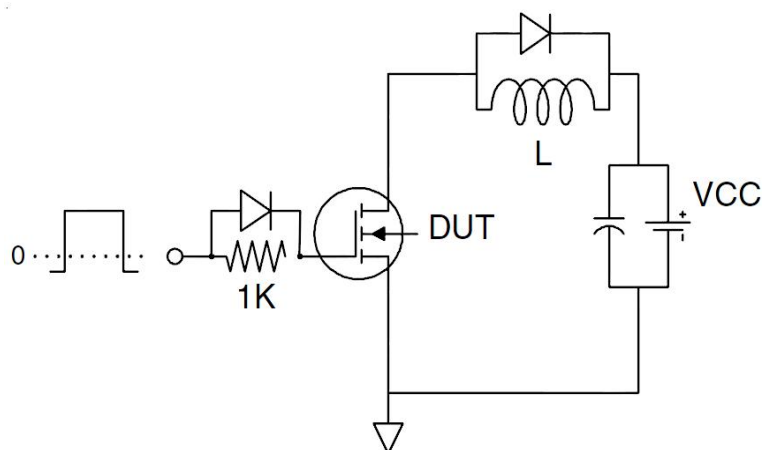
1. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_J(MAX)=175^{\circ}\text{C}$. The SOA curve provides a single pulse rating.

Test Circuit

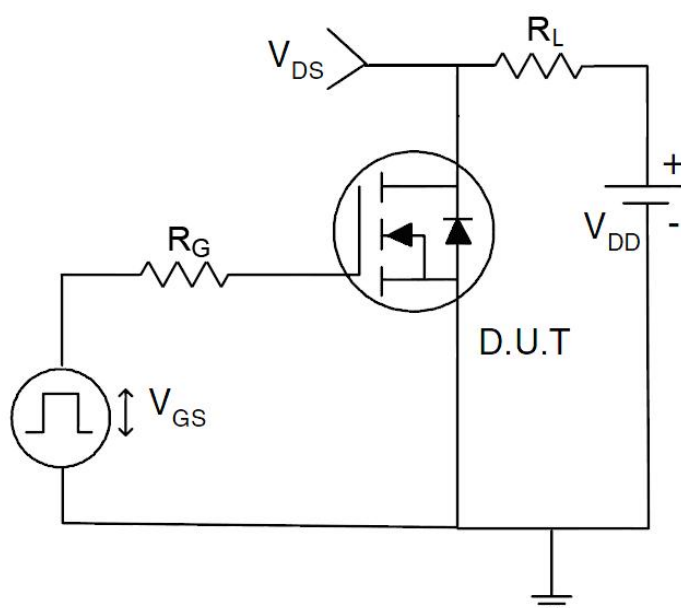
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

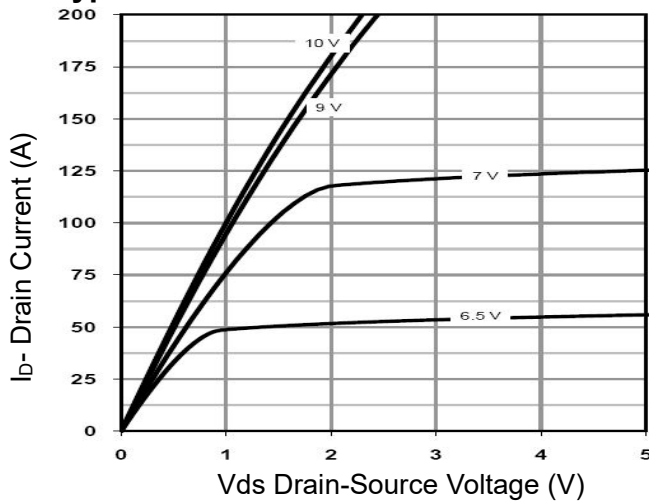


Figure 1 Output Characteristics

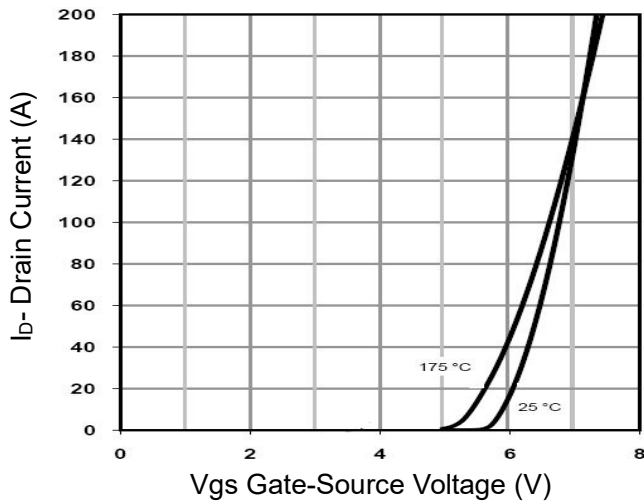


Figure 2 Transfer Characteristics

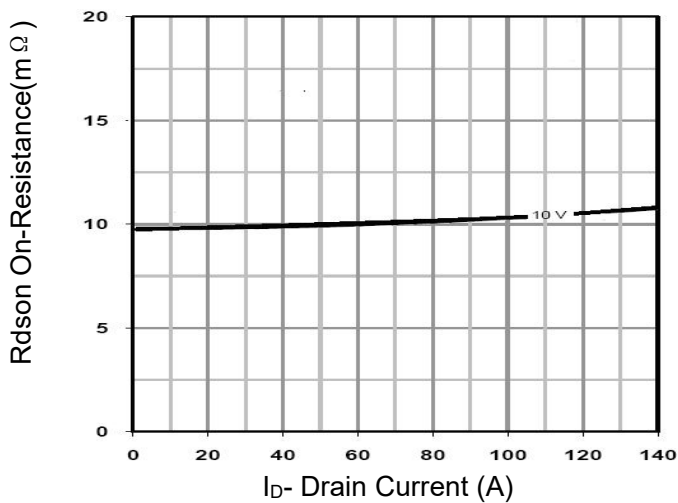


Figure 3 $R_{DS(on)}$ - Drain Current

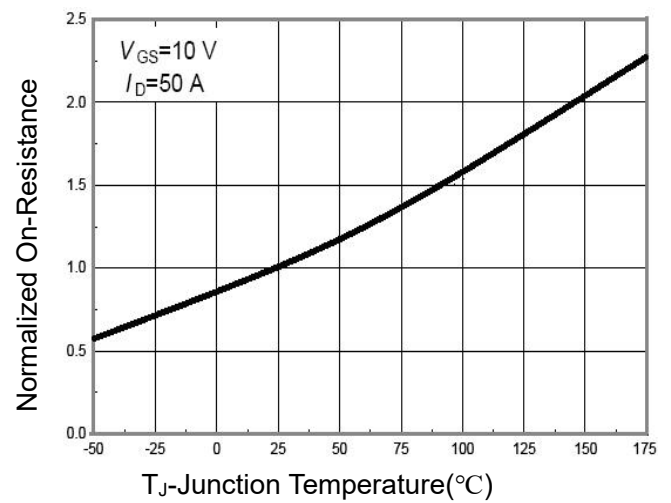


Figure 4 $R_{DS(on)}$ -Junction Temperature

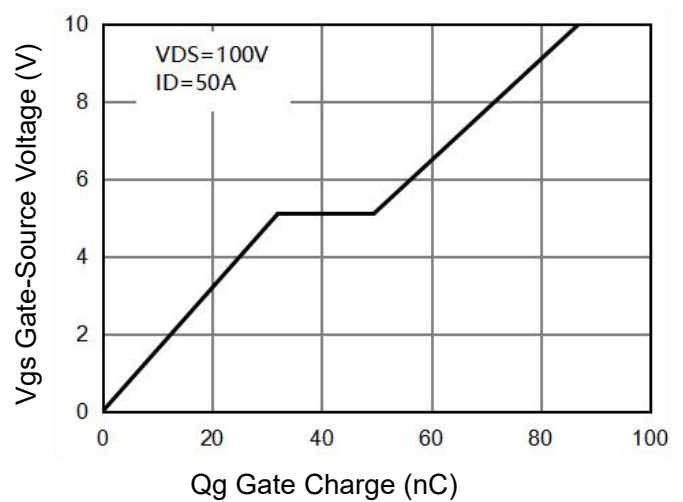


Figure 5 Gate Charge

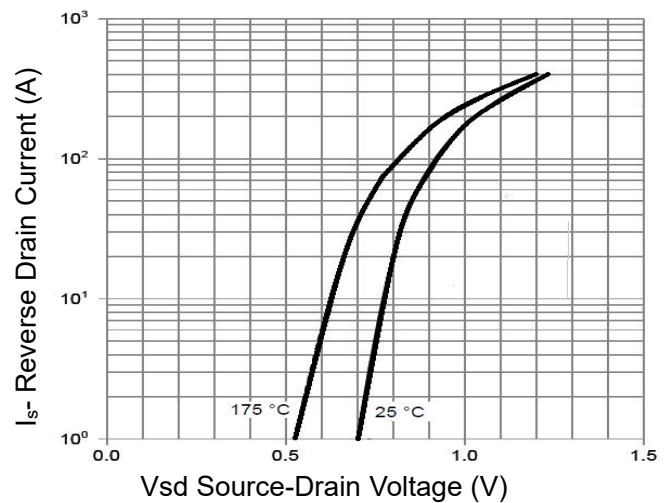
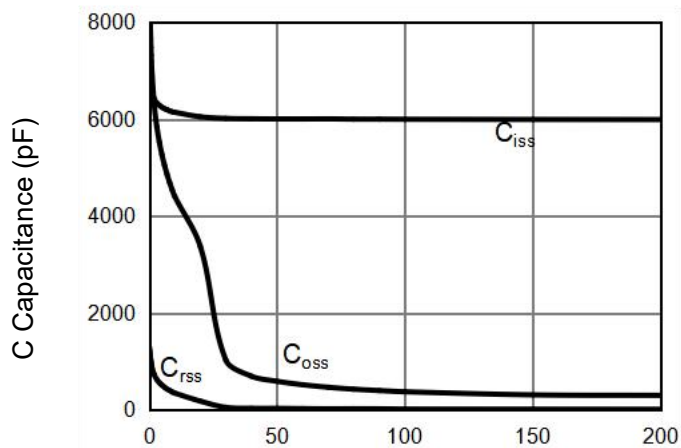
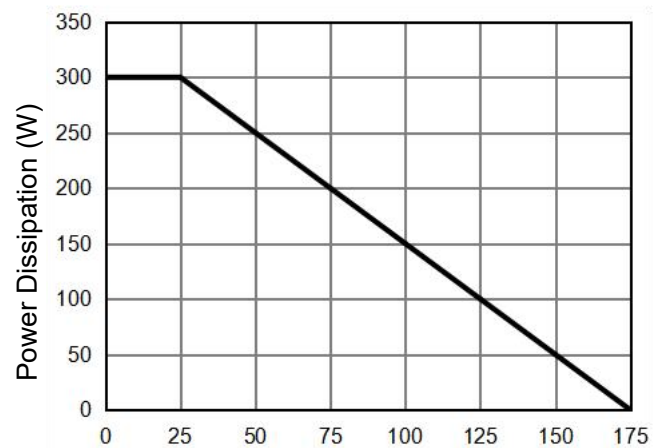


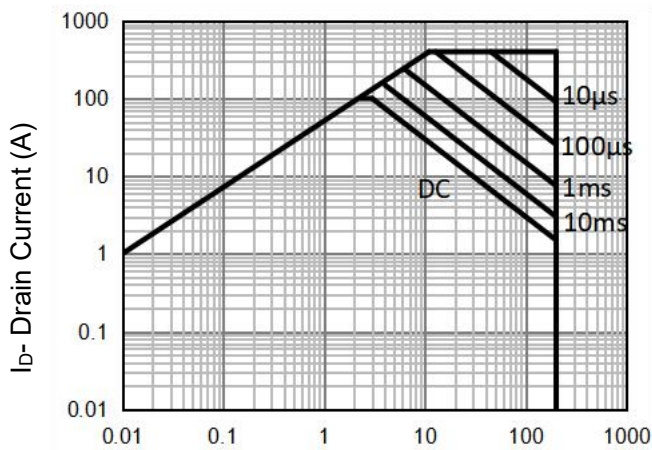
Figure 6 Source- Drain Diode Forward



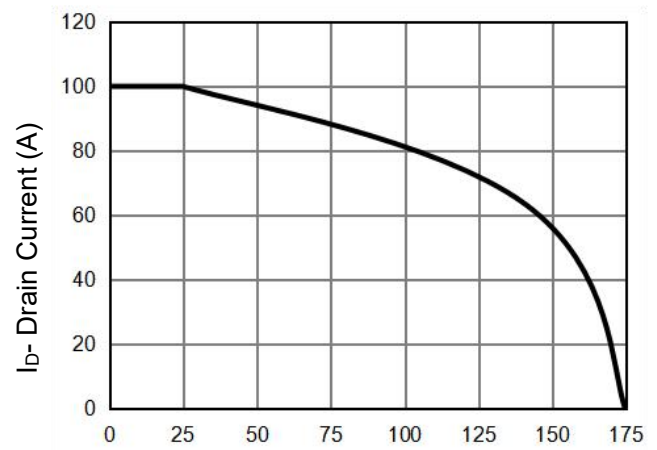
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



T_J-Junction Temperature(°C)
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area (Note 3)



T_J-Junction Temperature (°C)
Figure 10 Current De-rating

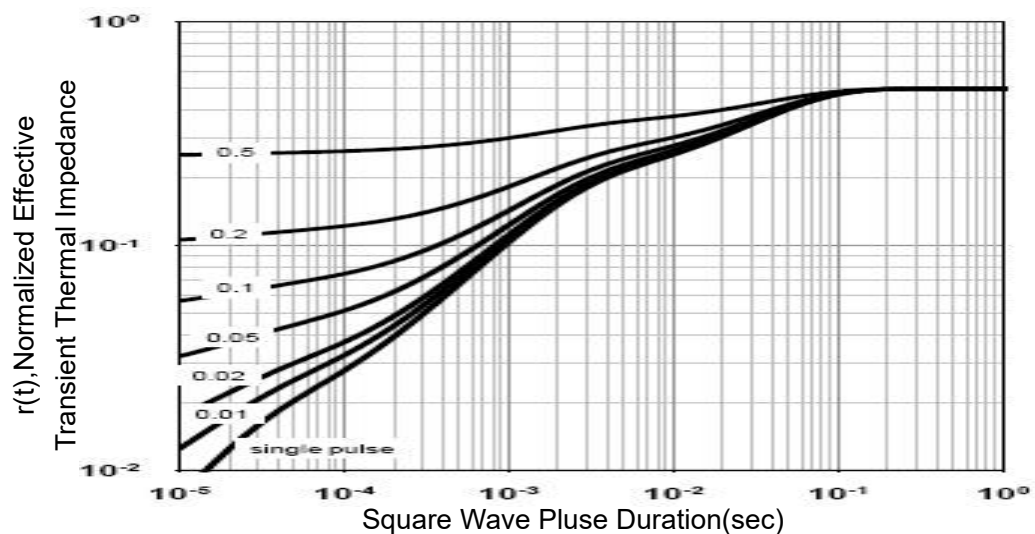
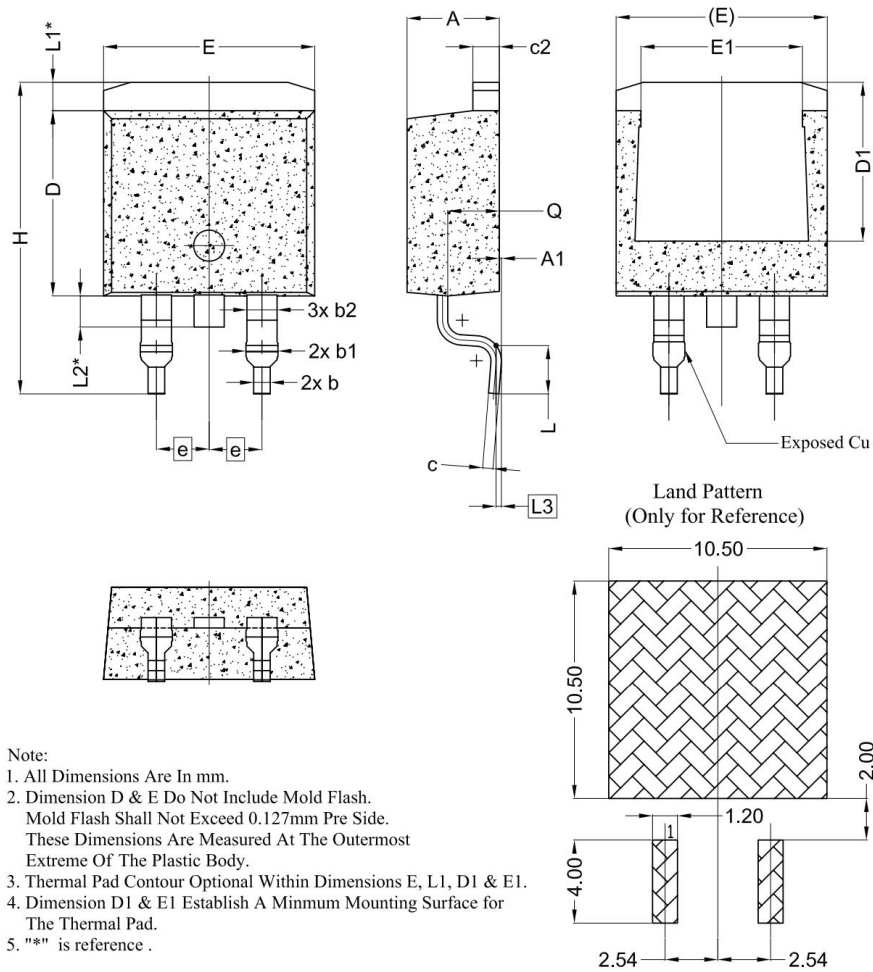


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-263-2L Package Information



- Note:
1. All Dimensions Are In mm.
 2. Dimension D & E Do Not Include Mold Flash.
Mold Flash Shall Not Exceed 0.127mm Pre Side.
These Dimensions Are Measured At The Outermost Extreme Of The Plastic Body.
 3. Thermal Pad Contour Optional Within Dimensions E, L1, D1 & E1.
 4. Dimension D1 & E1 Establish A Minmum Mounting Surface for The Thermal Pad.
 5. "*" is reference .

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	4.24	4.44	4.64
A1	0.00	0.10	0.25
b	0.70	0.80	0.90
b1	1.20	1.55	1.75
b2	1.20	1.45	1.70
c	0.40	0.50	0.60
c2	1.15	1.27	1.40
D	8.82	8.92	9.02
D1	6.86	7.65	—
E	9.96	10.16	10.36
E1	6.89	7.77	7.89
e	2.54 BSC		
H	14.61	15.00	15.88
L	1.78	2.32	2.79
L1	1.36 REF.		
L2	1.50 REF.		
L3	0.25 BSC		
Q	2.30	2.48	2.70

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