

NCE N-Channel Super Trench Power MOSFET

Description

The NCEP01T18VD uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

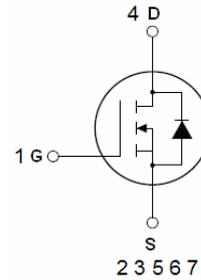
- $V_{DS} = 100V, I_D = 189A$
 $R_{DS(ON)} < 2.6m\Omega @ V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

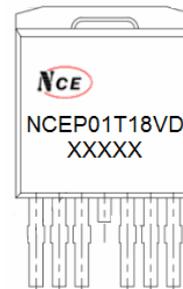
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

100% UIS TESTED!

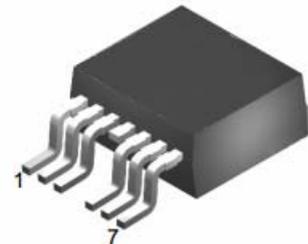
100% ΔV_d s TESTED!



Schematic diagram



Marking and pin assignment



TO-263-7L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP01T18VD	NCEP01T18VD	TO-263-7L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	189	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	135	A
Pulsed Drain Current	I_{DM}	756	A
Maximum Power Dissipation	P_D	300	W
Derating factor		2	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	1800	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.5	$^{\circ}\text{C}/\text{W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

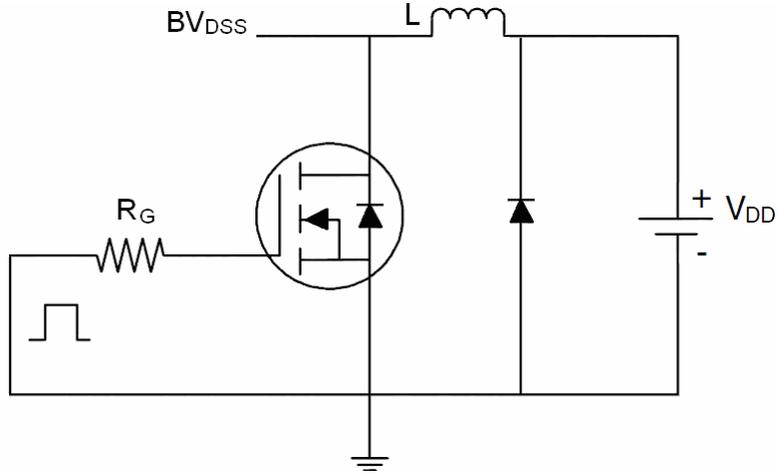
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5	3.5	4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=100A$	-	2.3	2.6	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=50A$	90	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	11500	-	PF
Output Capacitance	C_{oss}		-	1480	-	PF
Reverse Transfer Capacitance	C_{rss}		-	75	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=100A$ $V_{GS}=10V, R_G=1.6\Omega$	-	25	-	nS
Turn-on Rise Time	t_r		-	75	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	89	-	nS
Turn-Off Fall Time	t_f		-	29	-	nS
Total Gate Charge	Q_g	$V_{DS}=50V, I_D=100A,$ $V_{GS}=10V$	-	158		nC
Gate-Source Charge	Q_{gs}		-	52		nC
Gate-Drain Charge	Q_{gd}		-	29		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=189A$	-		1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	189	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}, I_F = I_S$ $di/dt = 100A/\mu s$ ^(Note 3)	-	75		nS
Reverse Recovery Charge	Q_{rr}		-	185		nC

Notes:

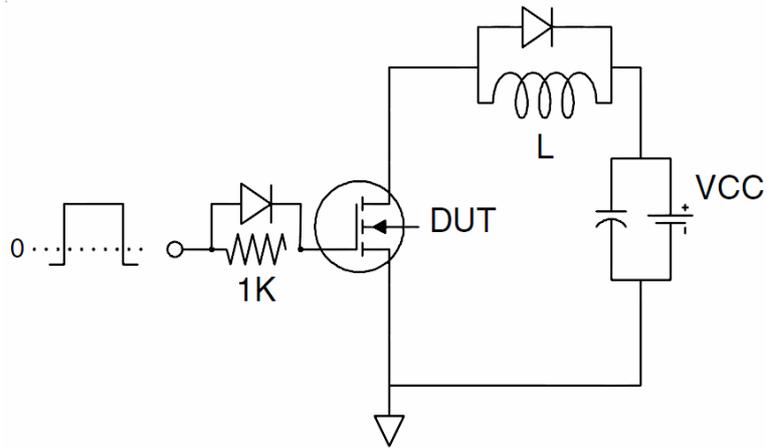
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_G=25\Omega$

Test Circuit

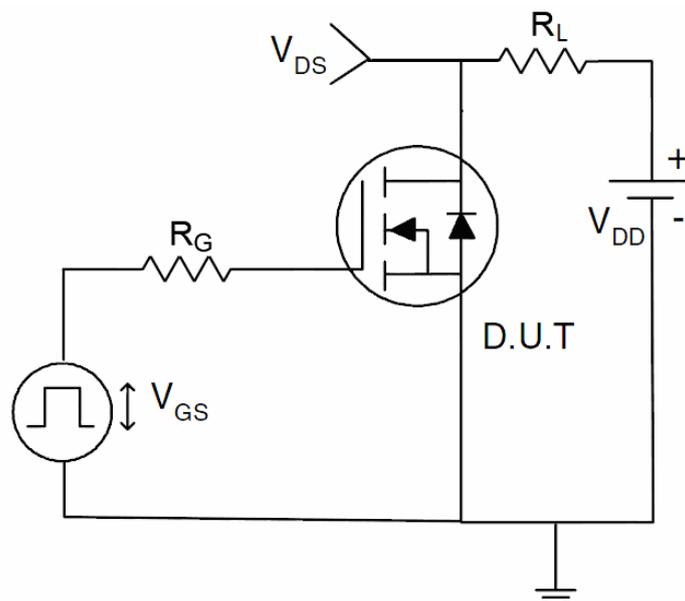
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

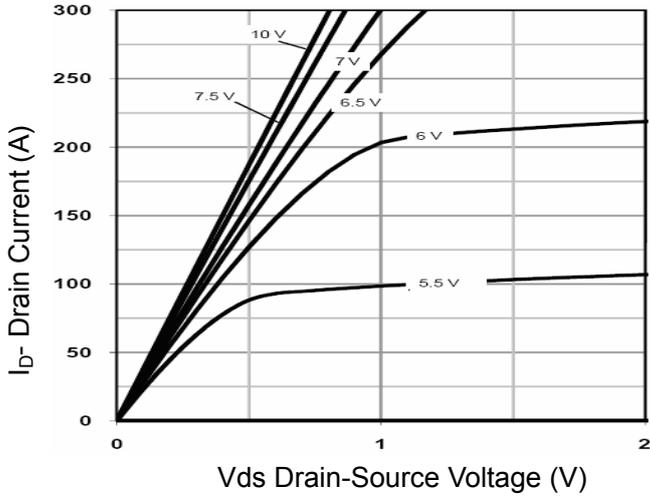


Figure 1 Output Characteristics

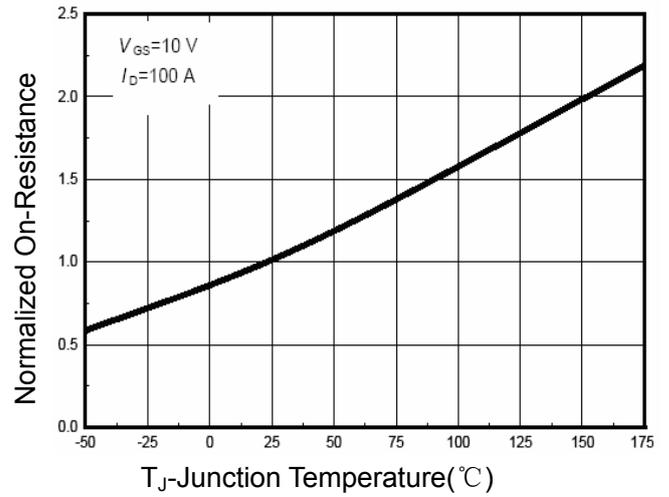


Figure 4 R_{dson} -Junction Temperature

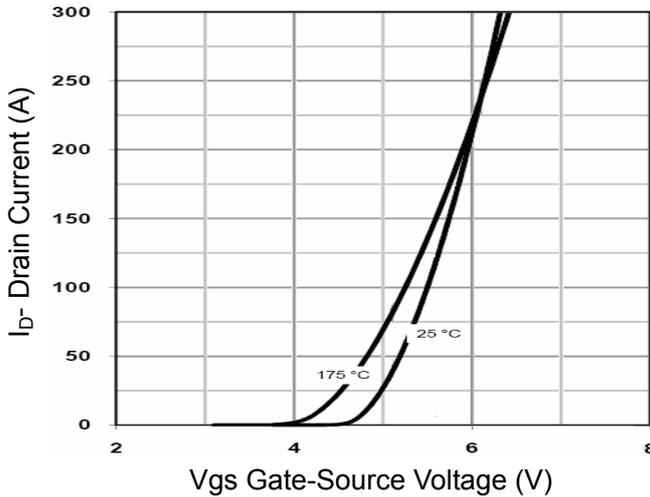


Figure 2 Transfer Characteristics

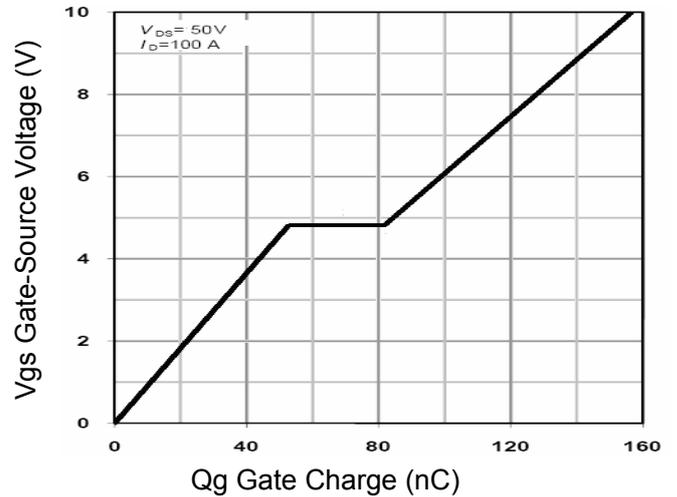


Figure 5 Gate Charge

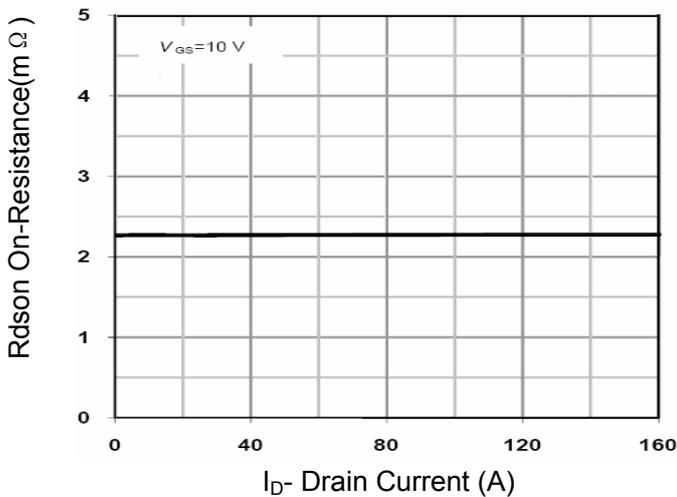


Figure 3 R_{dson} - Drain Current

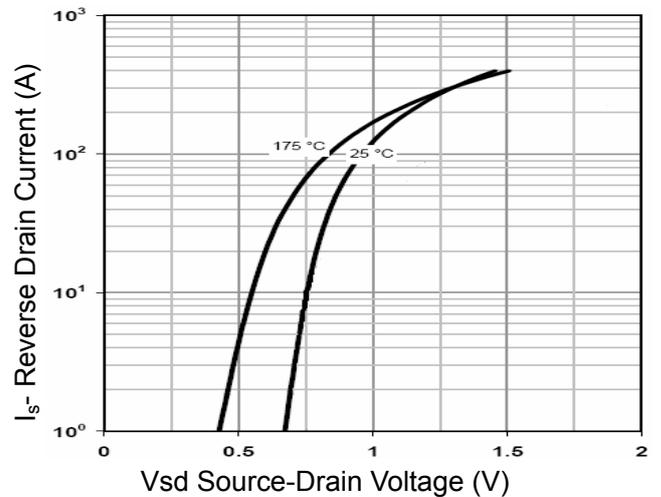


Figure 6 Source- Drain Diode Forward

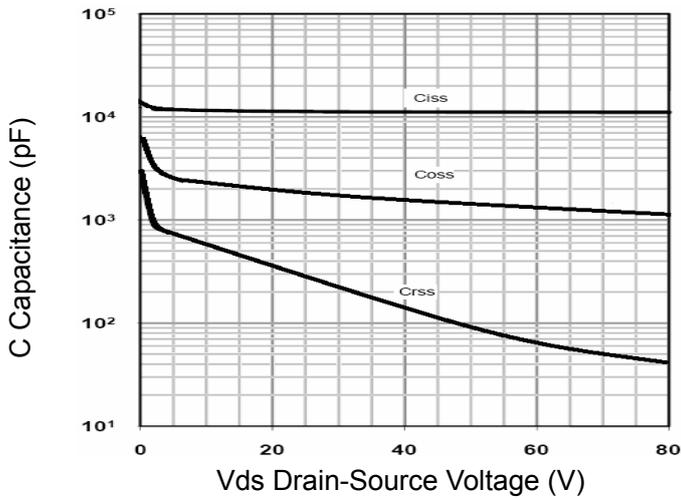


Figure 7 Capacitance vs Vds

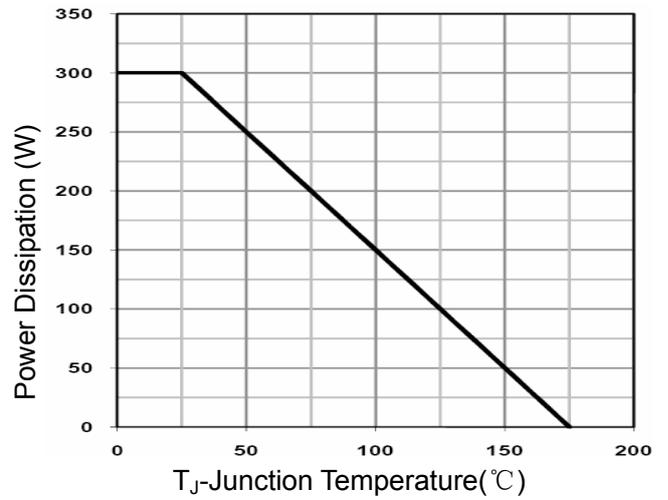


Figure 9 Power De-rating

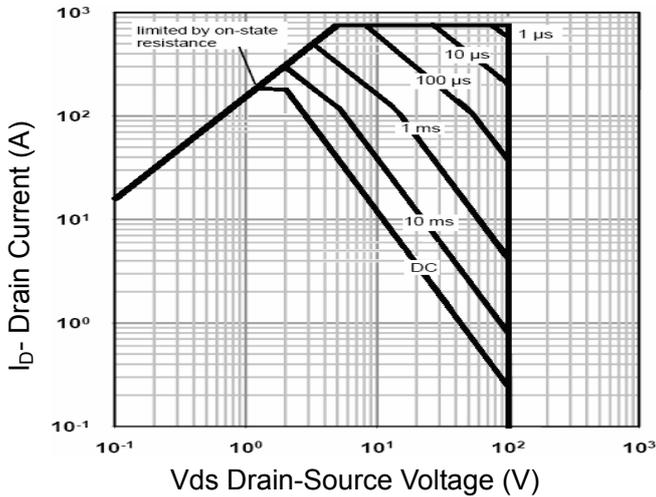


Figure 8 Safe Operation Area

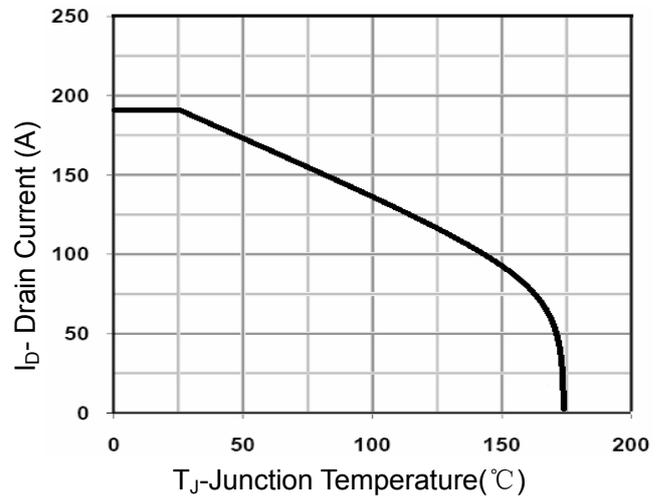


Figure 10 Current De-rating

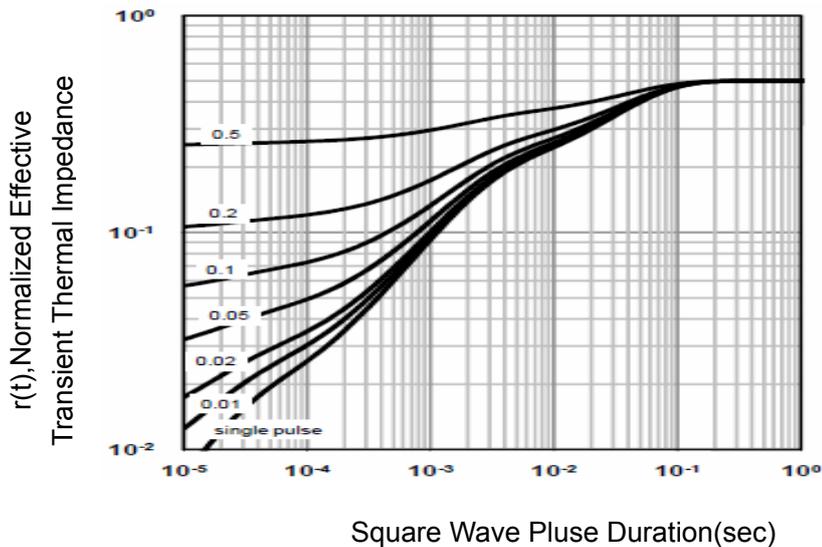
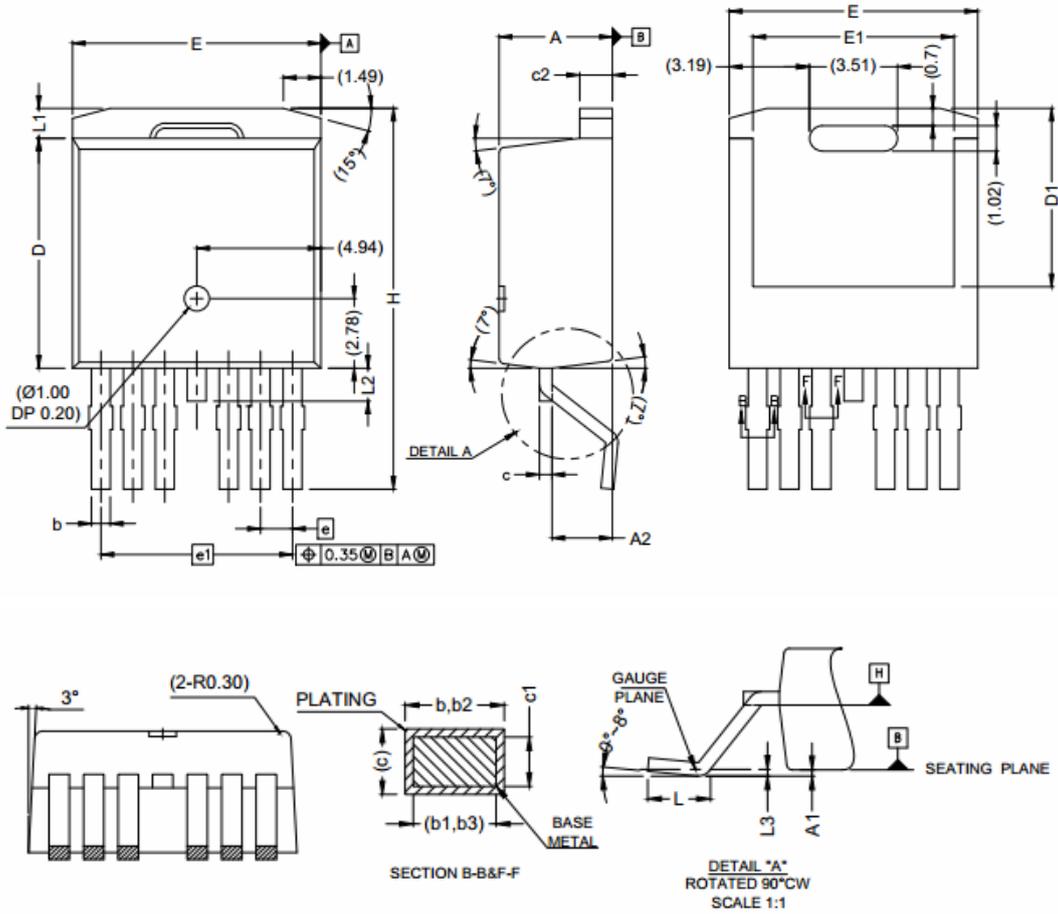


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-263-7L Package Information



SYMBOL	MIN	MAX
A	4.30	4.70
A1	-	0.254
A2	2.20	2.60
b	0.65	0.85
b1	0.65	0.80
b2	0.80	1.00
b3	0.80	0.95
c	0.45	0.60
c1	0.45	0.55
c2	1.25	1.40
D	9.00	9.40
D1	6.86	7.42
E	9.68	10.08
E1	7.70	8.30
e	1.27 BSC	
e1	7.62 BSC	
L	1.78	2.79
L1	-	1.60
L2	-	1.78
L3	0.25BSC	
H	14.61	15.88

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