

## NCE N-Channel Super Trench Power MOSFET

### Description

The NCEP01T13LL uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of  $R_{DS(ON)}$  and  $Q_g$ . This device is ideal for high-frequency switching and synchronous rectification.

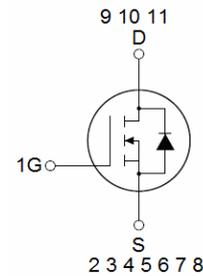
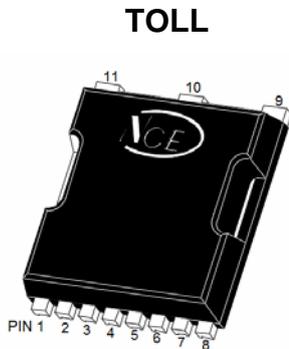
### Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

### General Features

- $V_{DS} = 100V, I_D = 160A$   
 $R_{DS(ON)} = 3.3m\Omega$ , typical @  $V_{GS} = 10V$
- Excellent gate charge x  $R_{DS(on)}$  product(FOM)
- Very low on-resistance  $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating

**100% UIS TESTED!**  
**100% ΔVds TESTED!**



Schematic Diagram

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP01T13LL	NCEP01T13LL	TOLL	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	160	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	128	A
Pulsed Drain Current	$I_{DM}$	640	A
Maximum Power Dissipation	$P_D$	260	W
Derating factor		1.73	W/°C
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	1200	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	°C

### Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	0.58	°C/W
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## Electrical Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

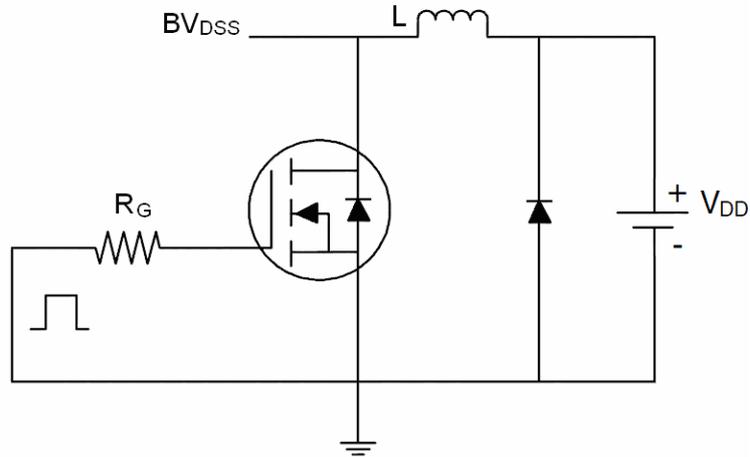
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100		-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	3.3	4.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=80A$	-	3.3	3.9	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=80A$	70	-	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	$C_{iss}$	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	7500	-	PF
Output Capacitance	$C_{oss}$		-	755	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	45	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=80A$ $V_{GS}=10V, R_G=4.7\Omega$	-	20	-	nS
Turn-on Rise Time	$t_r$		-	78	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	50	-	nS
Turn-Off Fall Time	$t_f$		-	16	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=50V, I_D=80A,$ $V_{GS}=10V$	-	100		nC
Gate-Source Charge	$Q_{gs}$		-	43.4		nC
Gate-Drain Charge	$Q_{gd}$		-	19.7		nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_S=160A$	-		1.2	V
Diode Forward Current	$I_S$		-	-	160	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}, I_F = I_S$ $di/dt = 100A/\mu\text{s}$ (Note 3)	-	65		nS
Reverse Recovery Charge	$Q_{rr}$		-	144		nC

### Notes:

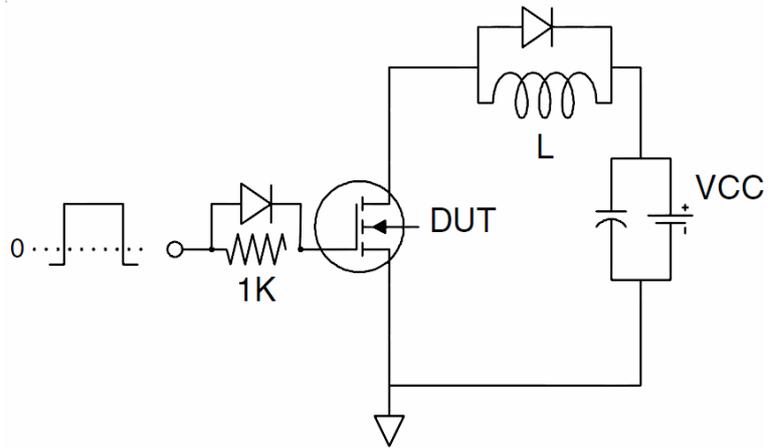
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board by JEDEC . Continuous current at  $T_C=25^\circ\text{C}$  is silicon limited
3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition :  $T_J=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

## Test Circuit

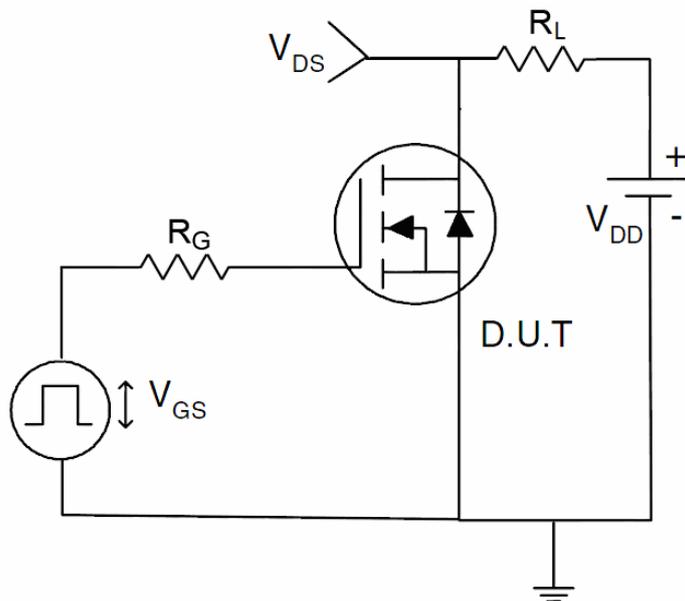
### 1) $E_{AS}$ test Circuit



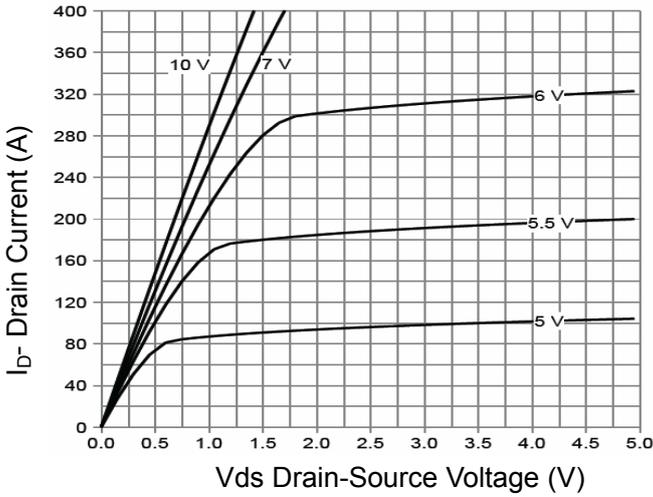
### 2) Gate charge test Circuit



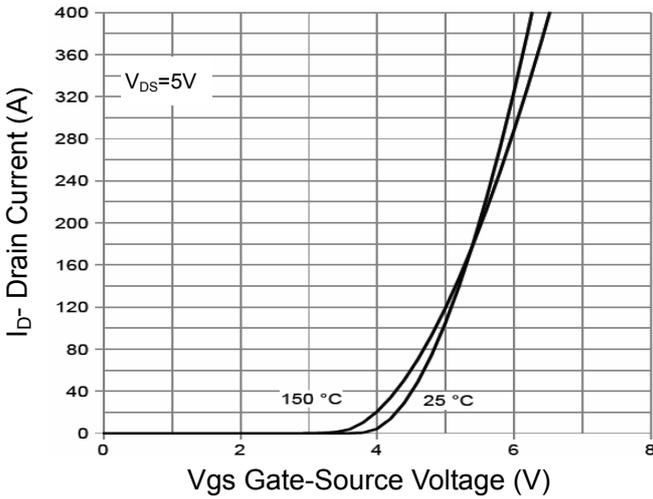
### 3) Switch Time Test Circuit



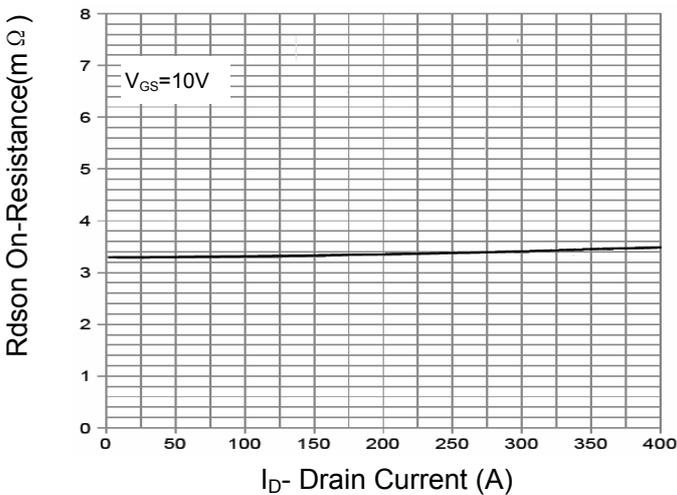
## Typical Electrical and Thermal Characteristics



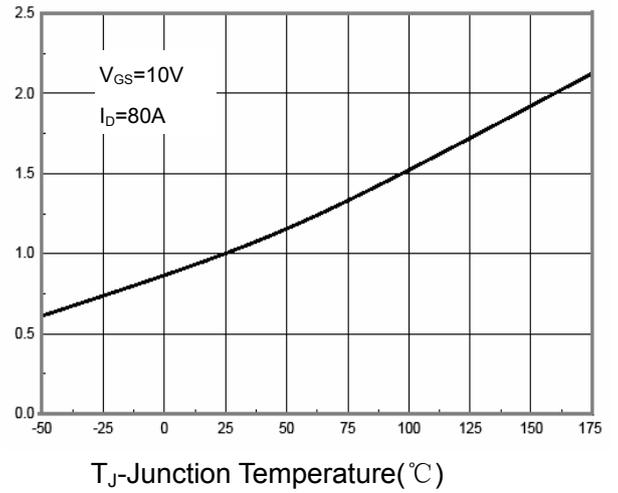
**Figure 1 Output Characteristics**



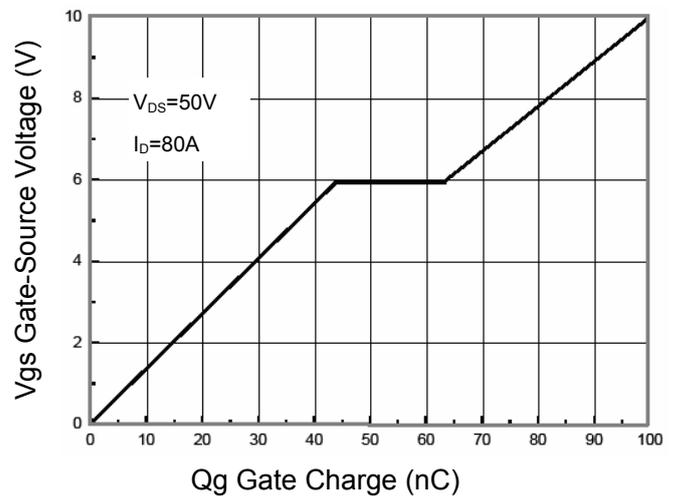
**Figure 2 Transfer Characteristics**



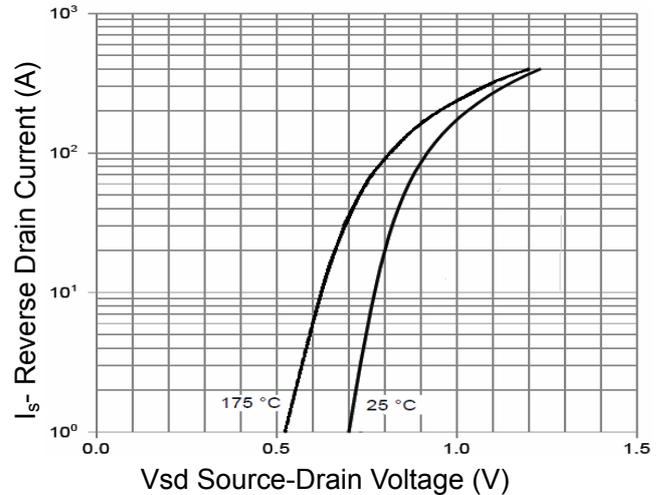
**Figure 3 Rdson- Drain Current**



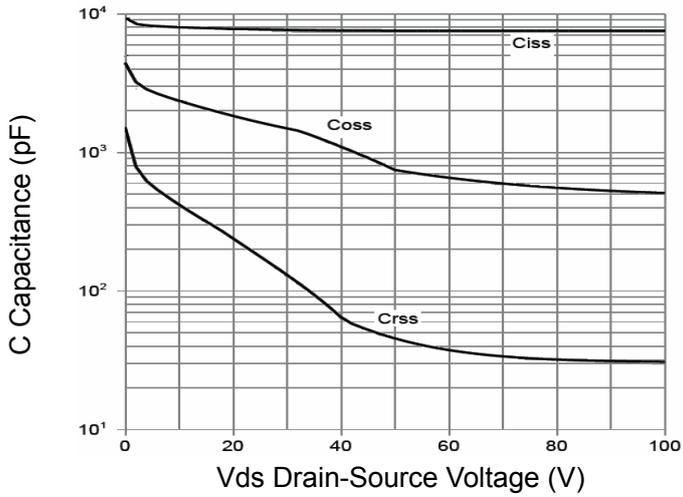
**Figure 4 Rdson-Junction Temperature**



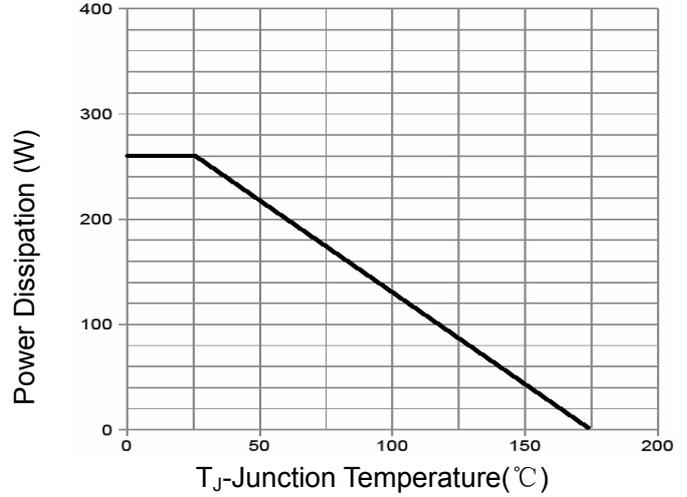
**Figure 5 Gate Charge**



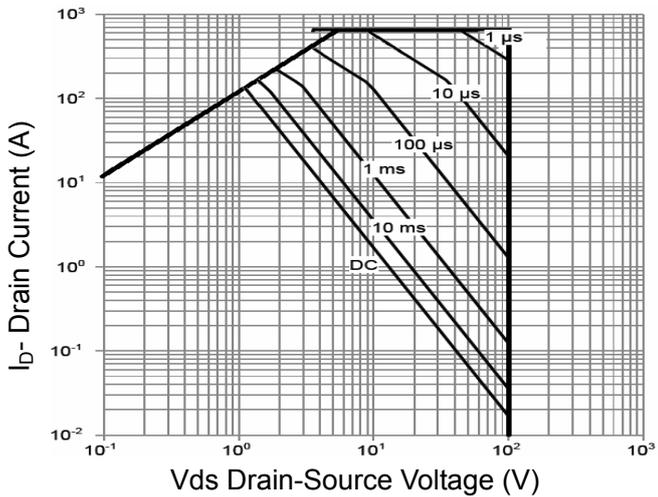
**Figure 6 Source- Drain Diode Forward**



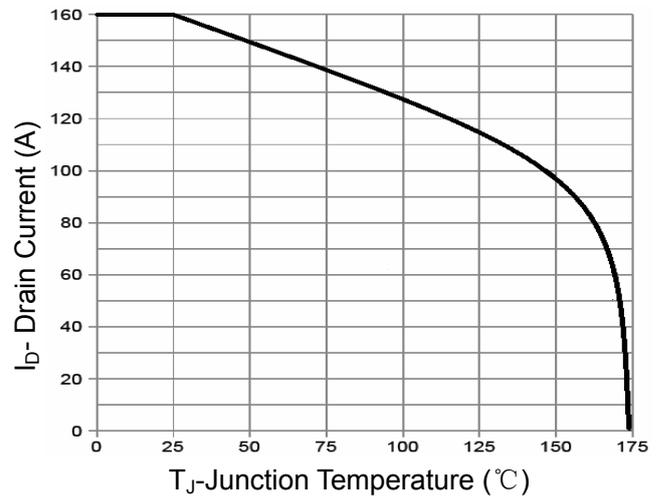
**Figure 7 Capacitance vs Vds**



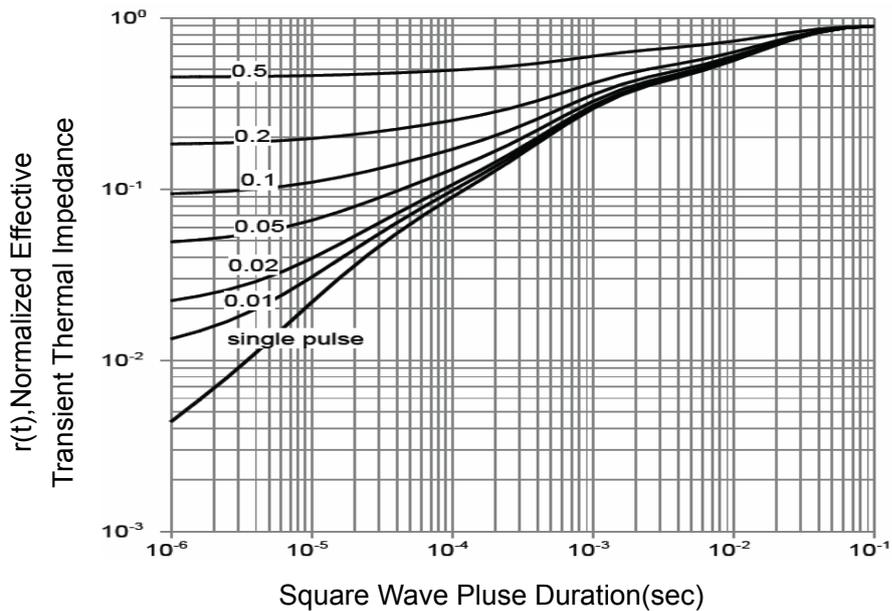
**Figure 9 Power De-rating**



**Figure 8 Safe Operation Area**

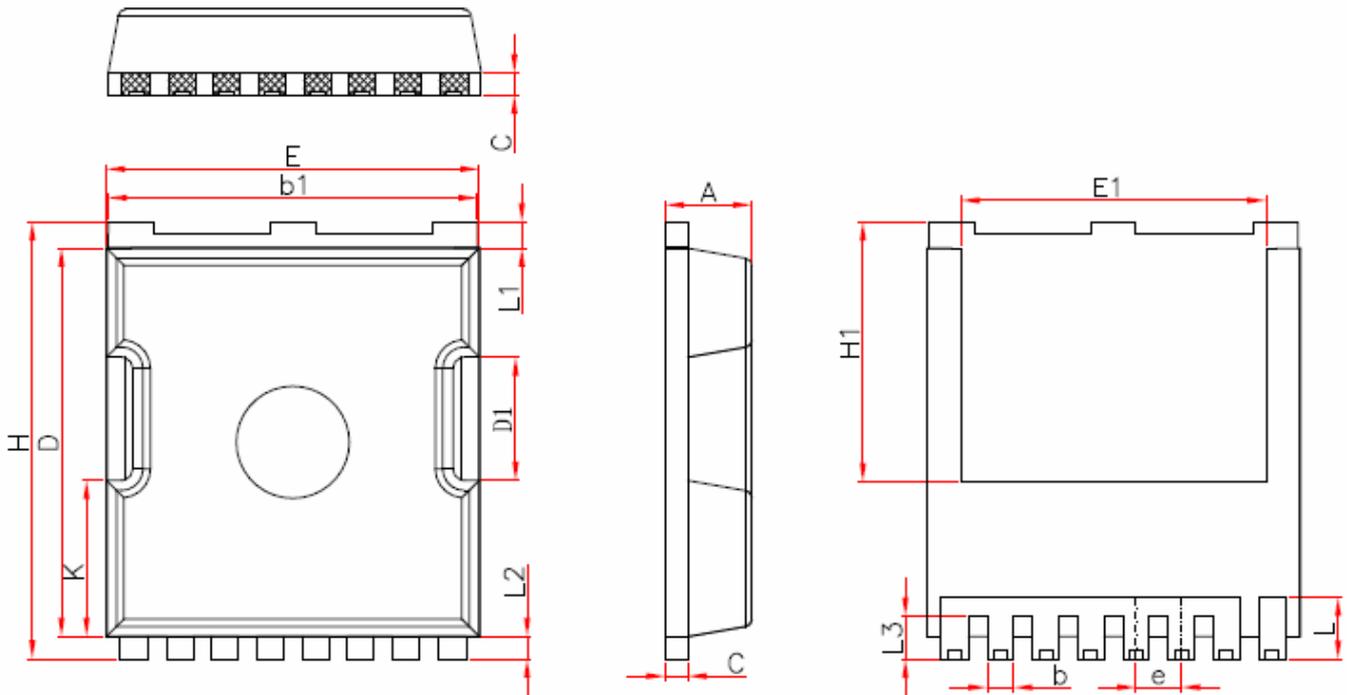


**Figure 10 Current De-rating**



**Figure 11 Normalized Maximum Transient Thermal Impedance**

## TOLL Package Information



Symbol	Millimeters		
	Min.	Nom.	Max.
A	2.20	2.30	2.40
b	0.65	0.75	0.85
b1	9.70	9.80	9.90
C	0.50	0.60	0.70
D	10.30	10.40	10.50
D1	3.15	3.3	3.45
E	9.70	9.90	10.10
E1	8.00	8.10	8.20
e	1.10	1.20	1.30
H	11.6	11.7	11.8
H1	6.85	6.95	7.05
K	4.08	4.18	4.28
L	1.60	1.65	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	1.05	1.20	1.30

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