

N-Channel Super Junction Power MOSFET IV

General Description

The series of devices use advanced trench gate super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

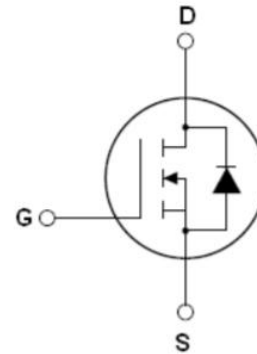
Features

- Optimized body diode reverse recovery performance
- Low on-resistance and low conduction losses
- Small package
- Ultra Low Gate Charge cause lower driving requirements
- 100% Avalanche Tested
- ROHS compliant

Application

- Power factor correction (PFC)
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply (UPS)
- LLC Half-bridge

$V_{DS\ min@T_{jmax}}$	650	V
$R_{DS(ON)TYP.}$	580	m Ω
I_D	6.7	A
Q_g	11	nC



Schematic diagram

Package Marking And Ordering Information

Device	Device Package	Marking
NCE60N640D	TO-263	NCE60N640D



TO-263-2L

Table 1. Absolute Maximum Ratings ($T_c=25^\circ\text{C}$)

Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS}=0V$)	V_{DS}	600	V
Gate-Source Voltage ($V_{DS}=0V$), AC ($f>1\text{ Hz}$)	V_{GS}	± 30	V
Gate-Source Voltage ($V_{DS}=0V$), DC	V_{GS}	± 20	V
Continuous Drain Current at $T_c=25^\circ\text{C}$	$I_{D(DC)}$	6.7	A
Continuous Drain Current at $T_c=100^\circ\text{C}$	$I_{D(DC)}$	4.69	A
Pulsed drain current (Note 1)	$I_{DM(pluse)}$	20.1	A
Maximum Power Dissipation($T_c=25^\circ\text{C}$)	P_D	75	W
Derate above 25°C		0.5	W/ $^\circ\text{C}$
Avalanche current(Note 1)	I_{AS}	1.5	A
Reverse diode dv/dt , $V_{DS} \leq 480\text{ V}, I_{SD} < I_D$	dv/dt	15	V/ns
Drain Source voltage slope, $V_{DS} \leq 480\text{ V}$	dv/dt	50	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55...+175	$^\circ\text{C}$

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Maximum)	R_{thJC}	2	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient (Maximum)	R_{thJA}	62	$^{\circ}\text{C}/\text{W}$

Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	600			V
Zero Gate Voltage Drain Current($T_c=25^{\circ}\text{C}$)	I_{DSS}	$V_{DS}=600V, V_{GS}=0V$			1	μA
Zero Gate Voltage Drain Current($T_c=125^{\circ}\text{C}$)	I_{DSS}	$V_{DS}=600V, V_{GS}=0V$			50	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 200	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	3	3.5	4	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=3.3A$		580	640	m Ω
Dynamic Characteristics						
Gate Resistance	R_g	F=1MHZ, D-S short		39		Ω
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V,$ F=1MHz		485		pF
Output Capacitance	C_{oss}			12		pF
Reverse Transfer Capacitance	C_{riss}			3.72		pF
Total Gate Charge	Q_g	$V_{DS}=400V, I_D=3.3A,$ $V_{GS}=10V$		11.0		nC
Gate-Source Charge	Q_{gs}			3.3		nC
Gate-Drain Charge	Q_{gd}			2.4		nC
Gate plateau voltage	V_{gp}			4.9		V
Switching times						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=380V, I_D=3.3A,$ $R_G=4\Omega, V_{GS}=10V$		13		nS
Turn-on Rise Time	t_r			7		nS
Turn-Off Delay Time	$t_{d(off)}$			30		nS
Turn-Off Fall Time	t_f			12		nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I_{SD}	$T_c=25^{\circ}\text{C}$			6.7	A
Pulsed-Source-drain current(Body Diode)	I_{SDM}				20.1	A
Forward on voltage	V_{SD}	$T_j=25^{\circ}\text{C}, I_{SD}=6.7A, V_{GS}=0V$		0.9	1.1	V
Reverse Recovery Time	t_{rr}	$T_j=25^{\circ}\text{C}, I_F=3.3A,$ $di/dt=100A/\mu s$		150		nS
Reverse Recovery Charge	Q_{rr}			0.75		μC
Peak reverse recovery current	I_{rrm}			10		A

Notes: 1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. $T_j=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, R_G=25\Omega$

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

Figure1. Safe operating area

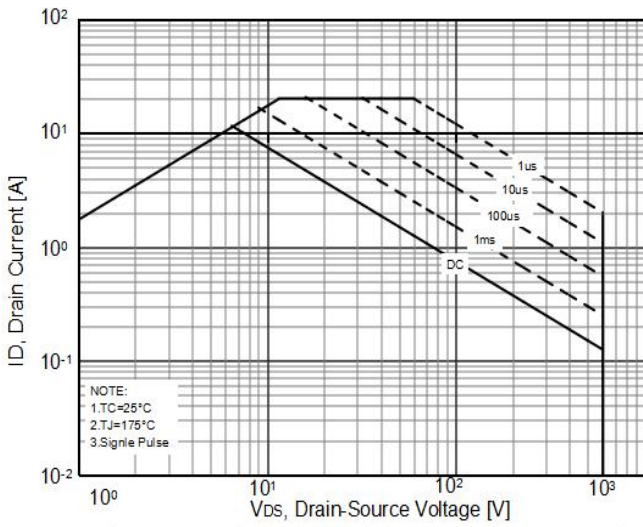


Figure2. Source-Drain Diode Forward Voltage

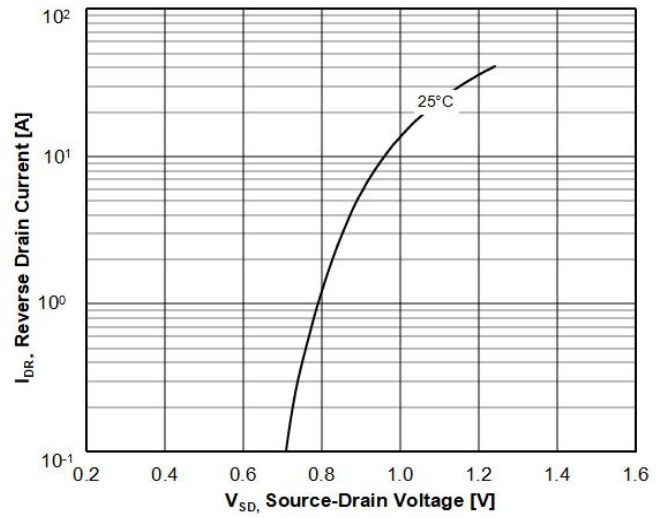


Figure3. Transfer characteristics

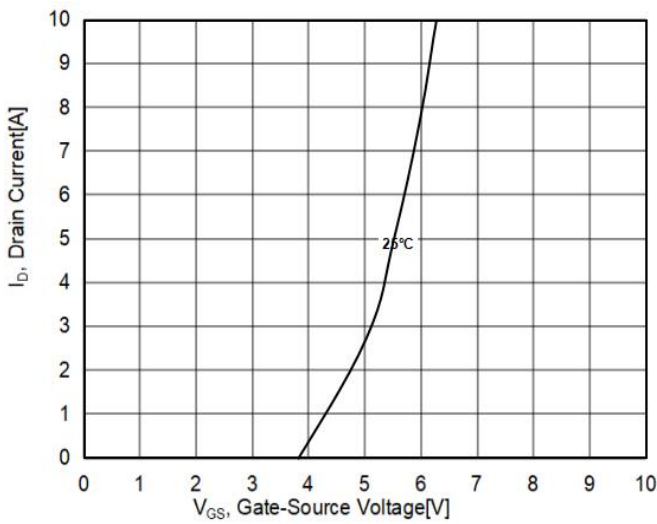


Figure4. Output characteristics

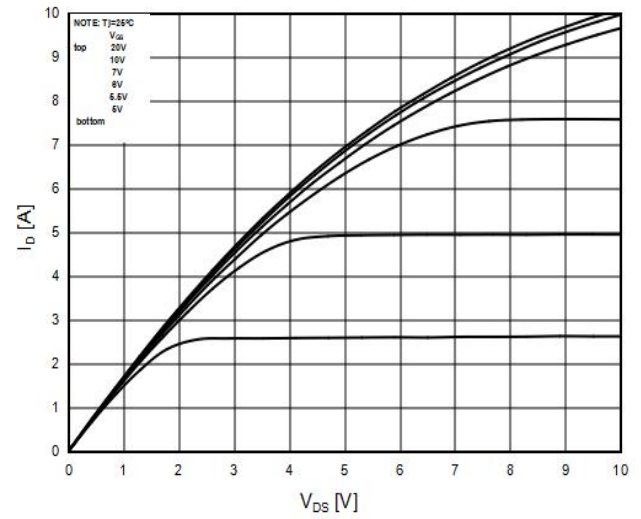


Figure5. Static drain-source on resistance

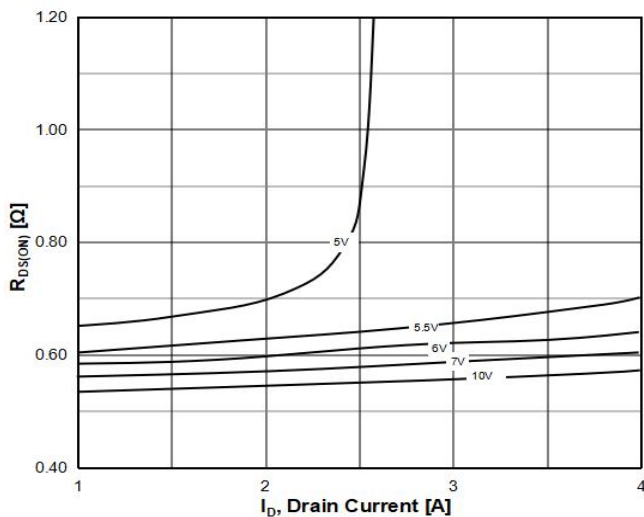


Figure6. RDS(ON) vs Junction Temperature

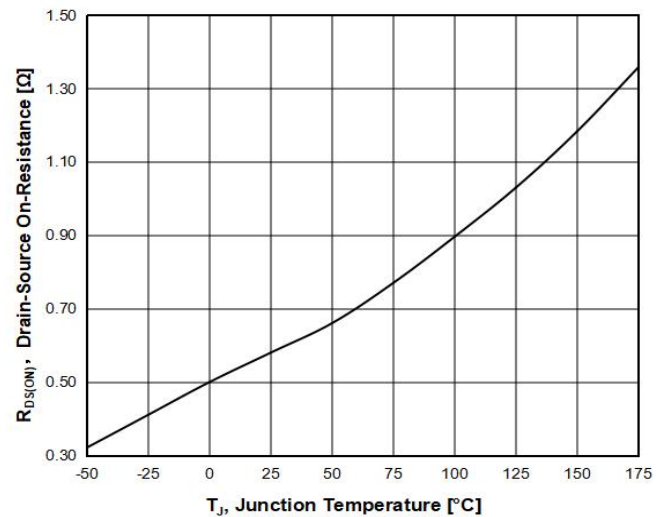


Figure7. BV_{DSS} vs Junction Temperature

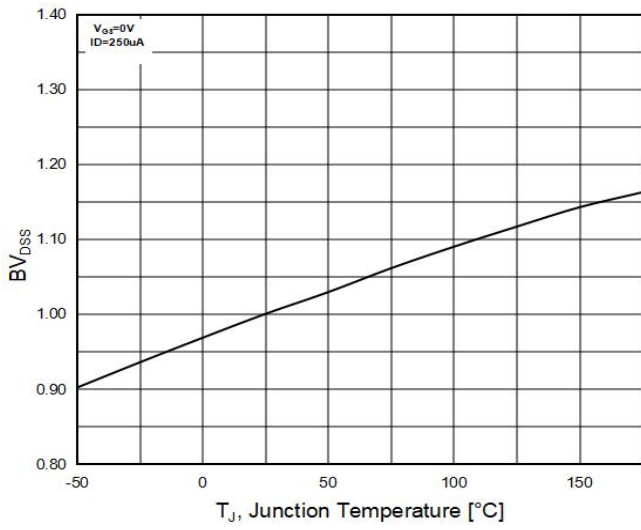


Figure8. Maximum I_D vs Junction Temperature

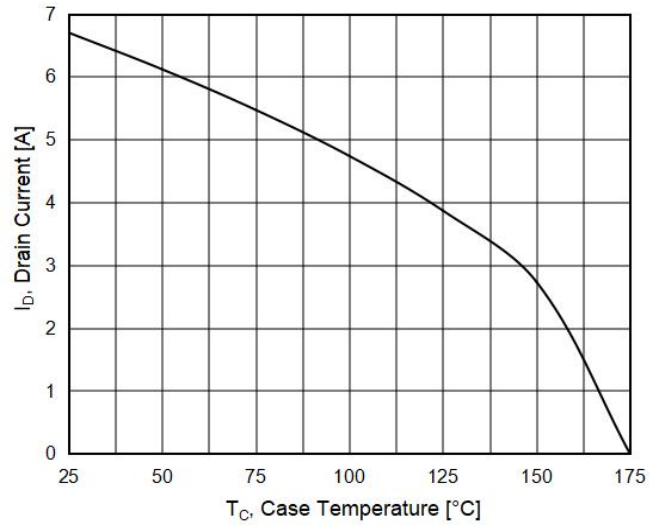


Figure9. Gate charge waveforms

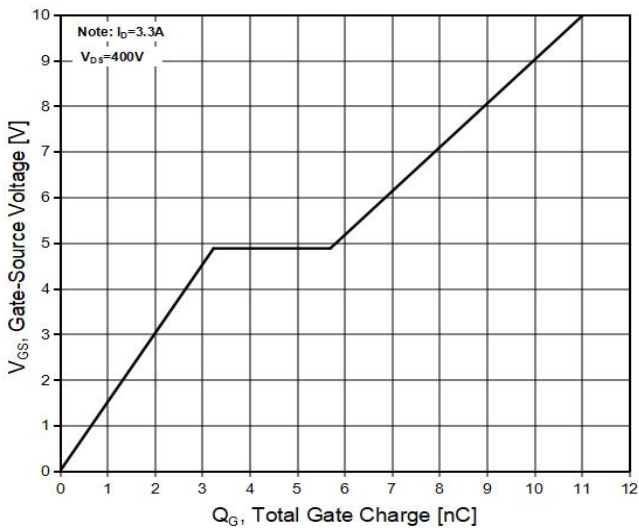
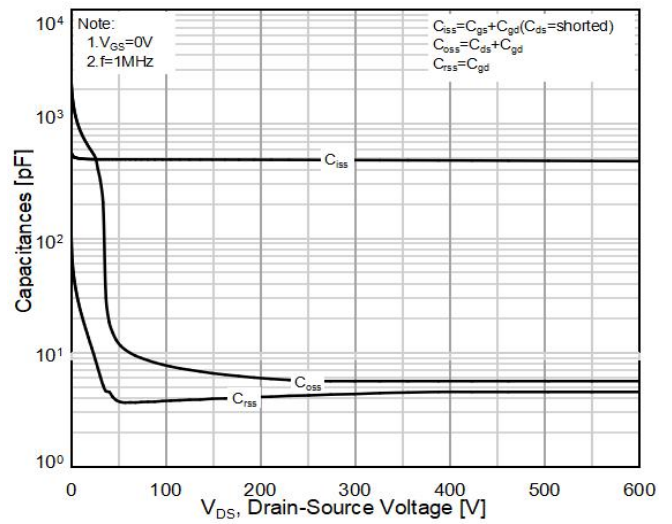
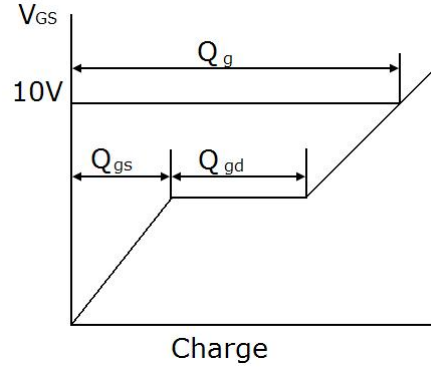


Figure10. Capacitance

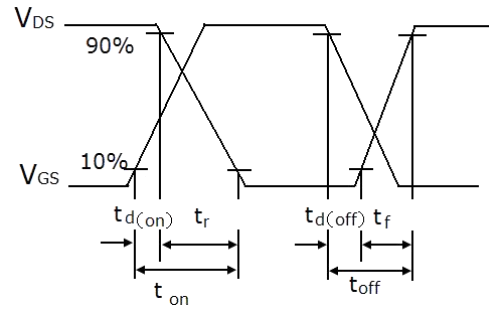


Test circuit

1) Gate charge test circuit & Waveform



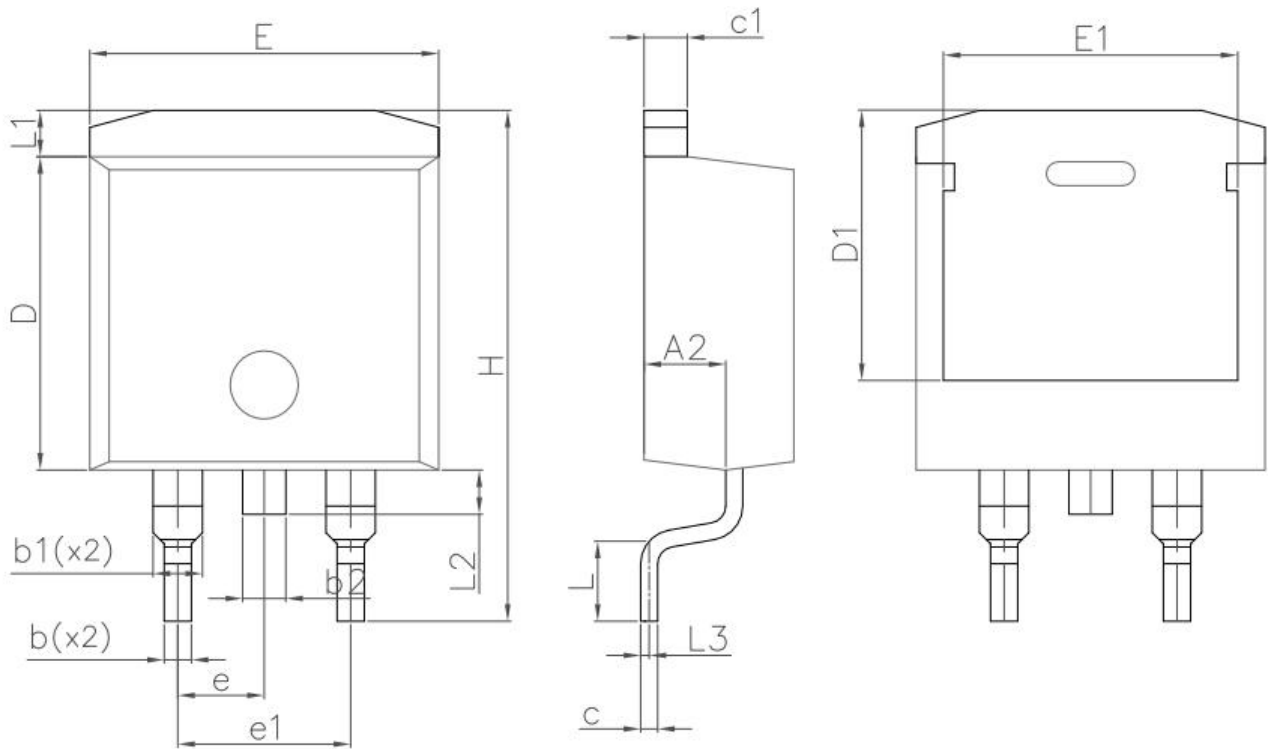
2) Switch Time Test Circuit:



3) Unclamped Inductive Switching Test Circuit & Waveforms



TO-263-2L-E Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A2	4.20	4.60	0.165	0.181
b	0.70	0.90	0.028	0.035
b1	1.20	1.75	0.047	0.069
b2	1.17	1.37	0.046	0.054
c	0.40	0.60	0.016	0.024
c1	1.15	1.40	0.045	0.055
D	9.10	9.30	0.358	0.366
D1	7.63	8.23	0.300	0.324
E	10.05	10.45	0.396	0.411
E1	8.35	8.95	0.329	0.352
e	2.54BSC		0.100BSC	
e1	5.08BSC		0.200BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	1.36REF		0.054REF	
L2	1.30REF		0.051REF	

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