

N-Channel Super Junction Power MOSFET IV

General Description

The series of devices use advanced trench gate super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

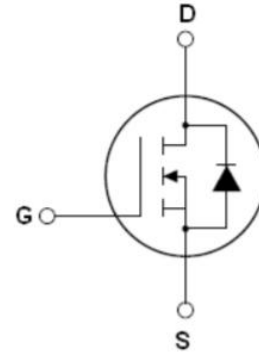
Features

- Optimized body diode reverse recovery performance
- Low on-resistance and low conduction losses
- Small package
- Ultra Low Gate Charge cause lower driving requirements
- 100% Avalanche Tested
- ROHS compliant

Application

- Power factor correction (PFC)
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply (UPS)
- LLC Half-bridge

$V_{DS\ min@T_{jmax}}$	550	V
$R_{DS(ON)TYP.}$	1050	m Ω
I_D	3	A
Q_g	4.2	nC



Schematic diagram

Package Marking And Ordering Information

Device	Device Package	Marking
NCE50N1K2K	TO-252-2L	NCE50N1K2K



G D S

TO-252

Table 1. Absolute Maximum Ratings ($T_c=25^\circ\text{C}$)

Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS}=0V$)	V_{DS}	500	V
Gate-Source Voltage ($V_{DS}=0V$), AC ($f>1\text{ Hz}$)	V_{GS}	± 30	V
Gate-Source Voltage ($V_{DS}=0V$), DC	V_{GS}	± 20	V
Continuous Drain Current at $T_c=25^\circ\text{C}$	$I_{D(DC)}$	3	A
Continuous Drain Current at $T_c=100^\circ\text{C}$	$I_{D(DC)}$	2.1	A
Pulsed drain current (Note 1)	$I_{DM(pluse)}$	9	A
Maximum Power Dissipation($T_c=25^\circ\text{C}$)	P_D	31	W
Derate above 25°C		0.21	W/ $^\circ\text{C}$
Single pulse avalanche current (Note 2)	I_{AS}	1	A
Reverse diode dv/dt , $V_{DS} \leq 480\text{ V}, I_{SD} < I_D$	dv/dt	15	V/ns
Drain Source voltage slope, $V_{DS} \leq 480\text{ V}$	dv/dt	50	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55...+175	$^\circ\text{C}$

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Maximum)	R_{thJC}	4.84	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient (Maximum)	R_{thJA}	62	$^{\circ}\text{C}/\text{W}$

Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	500			V
Zero Gate Voltage Drain Current(Tc=25°C)	I_{DSS}	$V_{DS}=500V, V_{GS}=0V$			1	μA
Zero Gate Voltage Drain Current(Tc=125°C)	I_{DSS}	$V_{DS}=500V, V_{GS}=0V$			50	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	3		4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=1.5A$		1050	1200	m Ω
Dynamic Characteristics						
Gate Resistance	R_g	F=1MHZ, D-S short		3.1		Ω
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V,$ F=1MHZ		120		pF
Output Capacitance	C_{oss}			10.5		pF
Reverse Transfer Capacitance	C_{riss}			4		pF
Total Gate Charge	Q_g	$V_{DS}=400V, I_D=1.5A,$ $V_{GS}=10V$		4.2	6	nC
Gate-Source Charge	Q_{gs}			0.5		nC
Gate-Drain Charge	Q_{gd}			1.1		nC
Gate plateau voltage	V_{gp}			5.3		V
Switching times						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=380V, I_D=1.5A,$ $R_G=4\Omega, V_{GS}=10V$		8		nS
Turn-on Rise Time	t_r			5.5		nS
Turn-Off Delay Time	$t_{d(off)}$			20		nS
Turn-Off Fall Time	t_f			22		nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I_{SD}	$T_c=25^{\circ}\text{C}$			3	A
Pulsed-Source-drain current(Body Diode)	I_{SDM}				9	A
Forward on voltage	V_{SD}	$T_j=25^{\circ}\text{C}, I_{SD}=3A, V_{GS}=0V$		0.9	1.1	V
Reverse Recovery Time	t_{rr}	$T_j=25^{\circ}\text{C}, I_F=1.5A,$ $di/dt=100A/\mu s$		130		nS
Reverse Recovery Charge	Q_{rr}			0.47		μC
Peak reverse recovery current	I_{rrm}			7.2		A

Notes: 1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. $T_j=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, R_G=25\Omega, L=30\text{mH}$

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

Figure1. Safe operating area

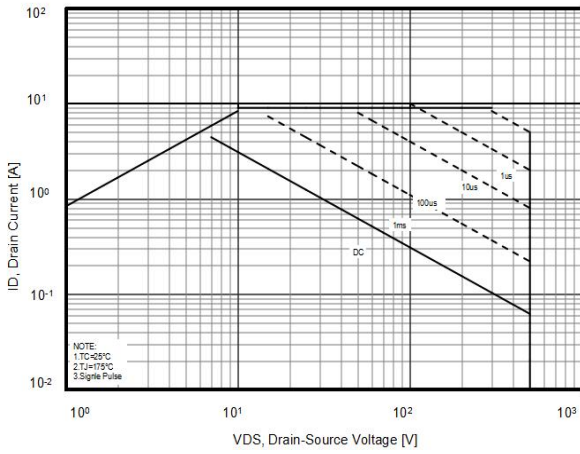


Figure2. Source-Drain Diode Forward Voltage

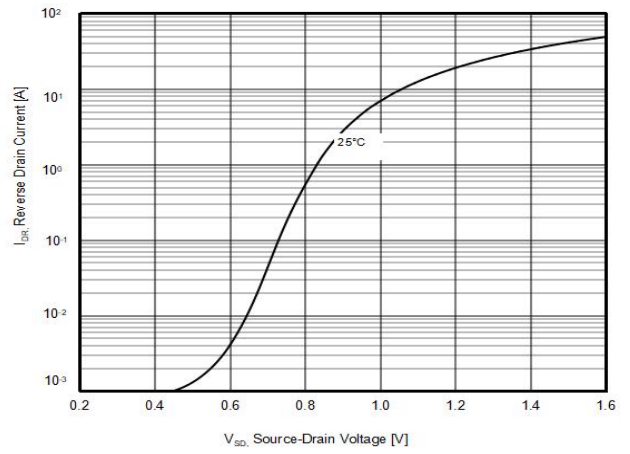


Figure3. Output characteristics

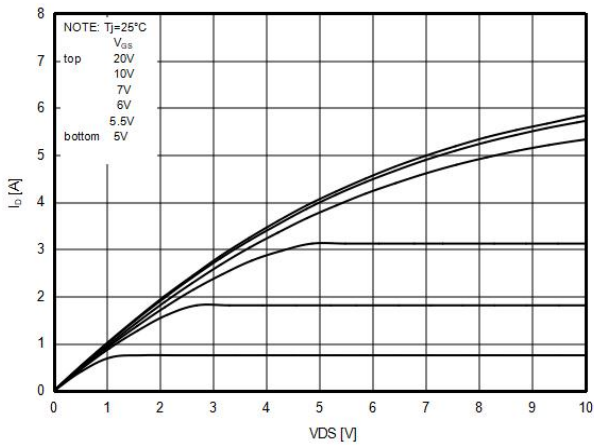


Figure4. Transfer characteristics

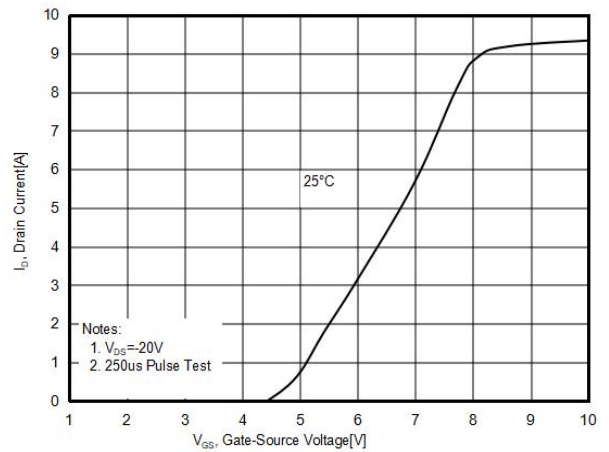


Figure5. Static drain-source on resistance

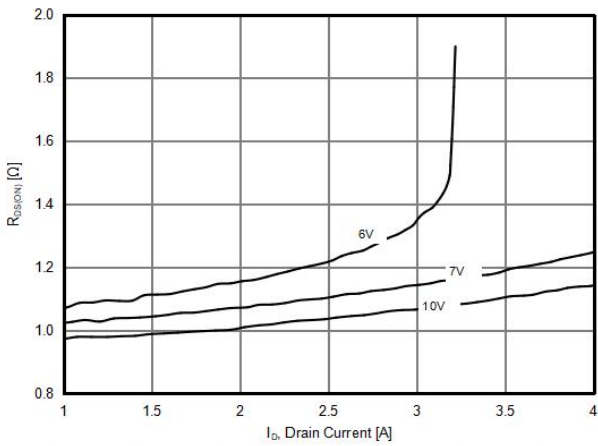


Figure6. $R_{DS(ON)}$ vs Junction Temperature

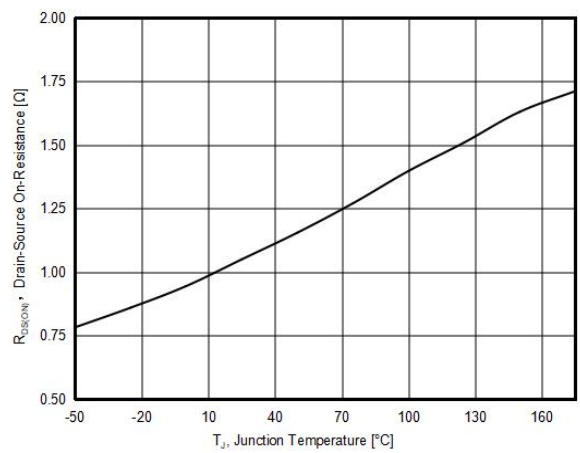


Figure7. BV_{DSS} vs Junction Temperature

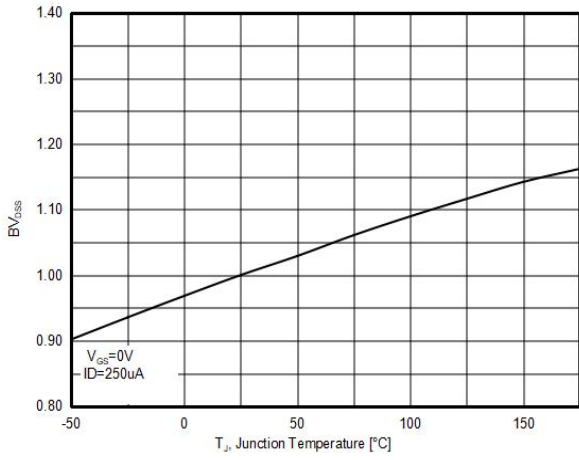


Figure8. Maximum I_D vs Junction Temperature

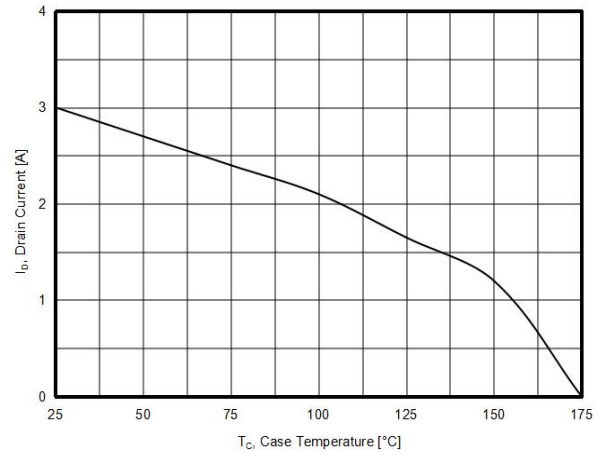


Figure9. Gate charge waveforms

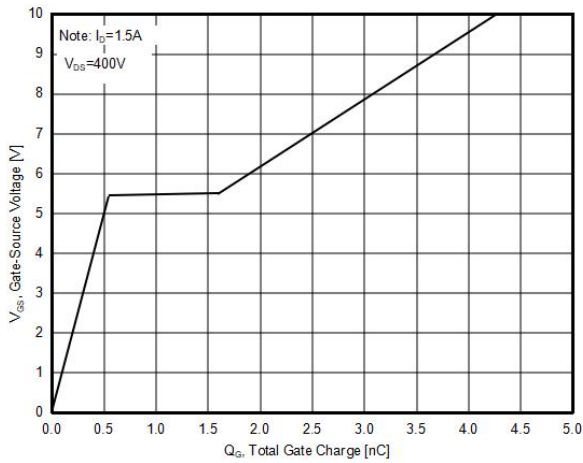
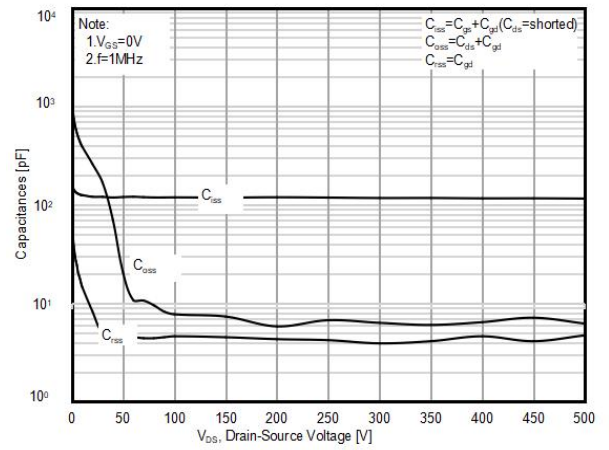


Figure10. Capacitance



Test circuit

1) Gate charge test circuit & Waveform



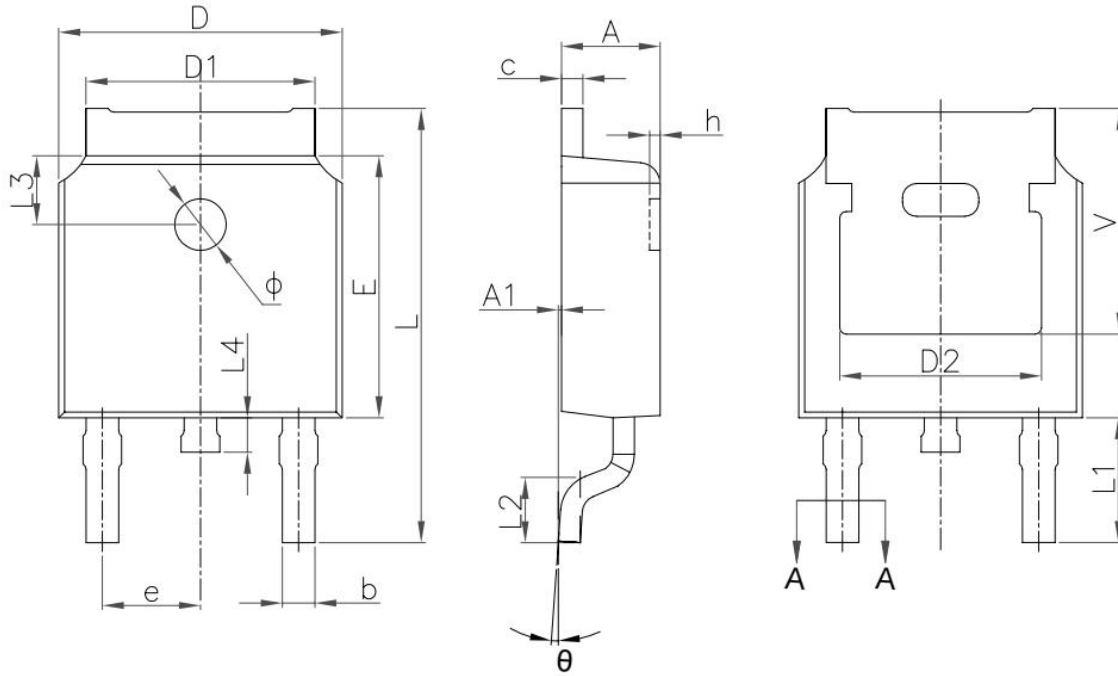
2) Switch Time Test Circuit:



3) Unclamped Inductive Switching Test Circuit & Waveforms



TO-252-2L-E Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.20	2.40	0.087	0.094
A1	0.00	0.13	0.000	0.005
b	0.66	0.86	0.026	0.033
b1	0.73	0.79	0.029	0.031
c	0.46	0.58	0.018	0.023
c1	0.50	0.52	0.020	0.020
D	6.50	6.70	0.256	0.264
D1	5.10	5.46	0.201	0.215
D2	4.83 REF		0.19REF	
E	6.00	6.20	0.236	0.244
e	2.19	2.39	0.086	0.094
L	9.80	10.40	0.386	0.409
L1	2.90 REF		0.11REF	
L2	1.40	1.70	0.055	
L3	1.60 REF		0.06REF	
L4	0.60	1.00	0.024	0.039
φ	1.10	1.30	0.043	0.051
θ	0°	8°	0°	8°
h	0.00	0.30	0.000	0.012

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