High Efficiency Wide Input Buck Power Switch

FEATURES

- **Integrated with 150V Power MOSFET and HV Startup Circuit**
- **Optimized Audible Noise & System Stability**
- **Multi-Mode Control**
- **Supports Buck Topology**
- **FB Divider Resistors Can be Saved in 12V Output Application**
- **Good Line and Load Regulation**
- **Built-in Soft Start Function**
- **Build in Protections:**
  - **Over Load Protection (OLP)**
  - **Cycle-by-Cycle Current Limiting (OCP)**
  - **FB Over Voltage Protection (FB OVP)**
  - **On-Chip Thermal Shutdown (OTP)**
  - **VDD OVP, UVLO & Clamp**
- **Available with SOP-8 Package**

GENERAL DESCRIPTION

KP35112 is a high performance Buck power switch for wide input range D2D application

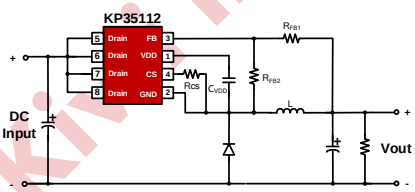
Unlike conventional PWM control, there's no fixed internal clock in KP35112 family to trigger the GATE driver, the switching frequency varies with load condition. The multi-mode PWM control is integrated to simplify circuit design and achieve good line and load regulation without audio noise. The peak current limit varies with load condition for low standby power.

KP35112 integrates functions and protections of Under Voltage Lockout (UVLO), Cycle-by-cycle Current Limiting (OCP), FB Over Voltage Protection (FB OVP), On-chip Thermal Shutdown, Over Load Protection (OLP), VDD OVP with Auto Recovery Mode Protection, etc.

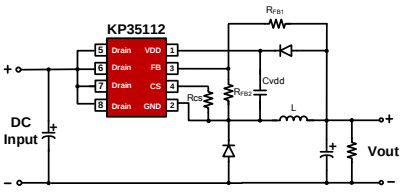
APPLICATIONS

- **Electric Bicycle**
- **POE**
- **Power Tools**

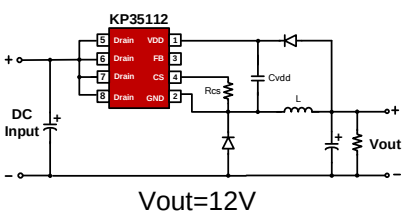
TYPICAL APPLICATION CIRCUIT



Vout<10V



Vout>10V & Vout≠12V



Vout=12V

Ordering Information

Order Number(1)	Package	Eco Plan	MSL Rating	Packing	Device Marking
KP35112SGA	SOP-8	Halogen Free	3	T&R, 4000 Pcs/Reel	KP35112SG

(1) KP35112 S G A

- Packing Code — A: Tape & Reel
- Eco Plan — G: Halogen Free
- Package Code — S: SOP-8
- Part Number

Marking Information

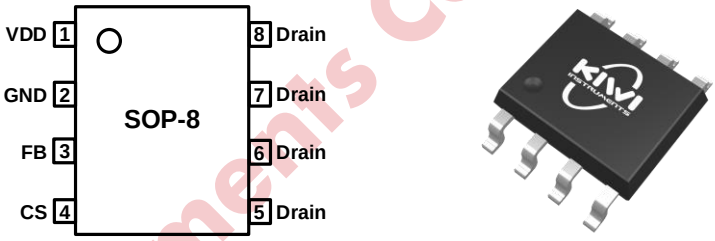
KP35112SG — Device Marking

XXXXXX — Wafer Lot Code

YWWZZFS — Y: Year Code; WW: Week Code; ZZ: Serial Number; F, S: Control Number(2)

(2) Wafer Lot Code, Year Code, Week Code, Serial Number, and Control Number are numbers or letters

Pin Configuration



Pin Number	Pin Name	Type(3)	Description
1	VDD	P	The power supply and the output voltage feedback pin (when FB pin is floating). A capacitor with 1μF is recommended to connect to this pin
2	GND	G	The Ground Reference for the IC
3	FB	I	Feedback Input
4	CS	I	Current Sensing Input
5,6,7,8	Drain	P	The Power MOSFET Drain

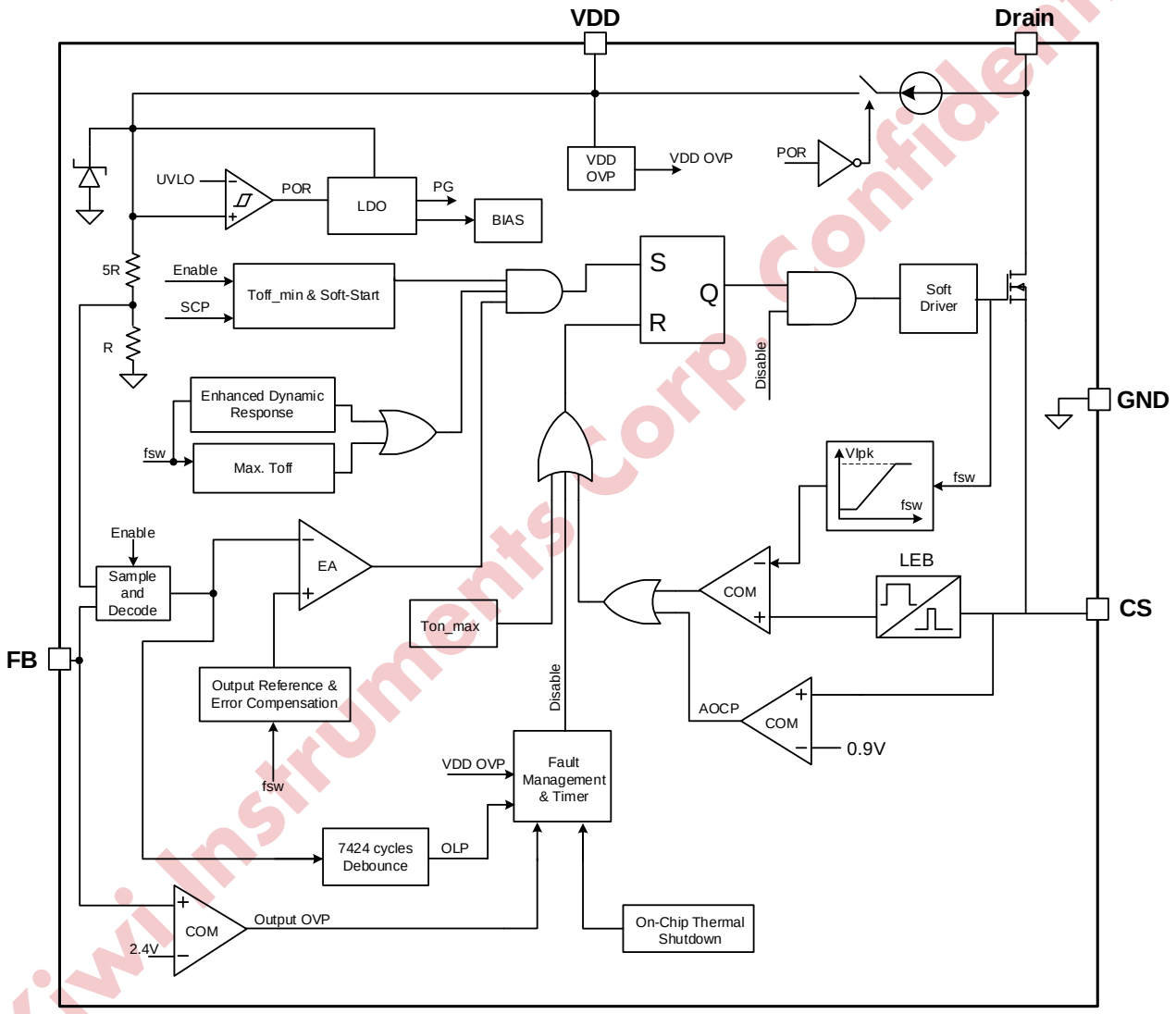
(3) I-Input； P-Power；G-Ground

Typical Output Power Table

Part Number	V_{BV} (V)	Max Output Current (4) (A)	Max Output Voltage (V)
KP35112	150V	1A	12V

(4) Maximum output current is constrained by IC maximum junction temperature and determined by ambient temperature and PCB. The system actual maximum output current is determined by the test.

Block Diagram



Absolute Maximum Ratings(5)

Parameter	Value	Unit
Drain Pin Voltage Range	-0.3 to 150	V
VDD DC Supply Voltage	-0.3 to 33	V
VDD DC Clamp Current	10	mA
FB, CS Voltage Range	-0.3 to 6	V
θ_{JA},Package Thermal Resistance–Junction to Ambient (SOP-8)	165	˚C/W
Maximum Junction Temperature	165	˚C
Storage Temperature Range	-40 to 165	˚C
Lead Temperature (10sec.)	260	˚C
Internal MOSFET continuous drain current	8	A
Internal MOSFET Pulse drain current	32	A

(5) Stresses listed as the above “Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

ESD Rating

Paramter		Value	Unit
V_{ESD}	Human Body Model - HBM (without HV Pin)(6)	5	kV
	Human Body Model - HBM (HV Pin)(6)	8	kV
	Charge Devices Model - CDM(7)	2	kV

(6) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing requirements with a standard ESD control process.

(7) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing requirements with a standard ESD control process.

Recommended Operation Conditions

Parameter	Value	Unit
Operating Junction Temperature	-40 to 125	˚C
Maximum Switching Frequency	180	kHz

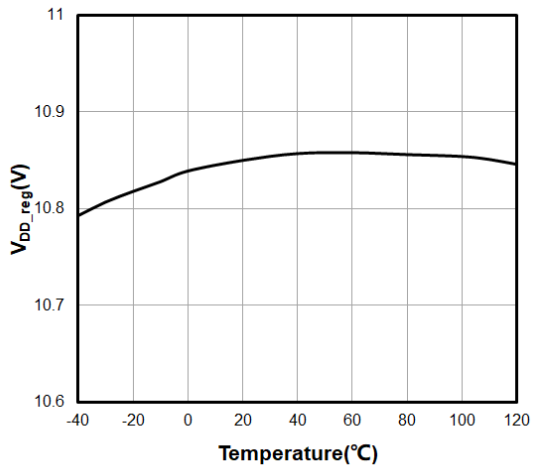
Electrical Characteristics (TA= 25℃, VDD=14V, if not otherwise noted)

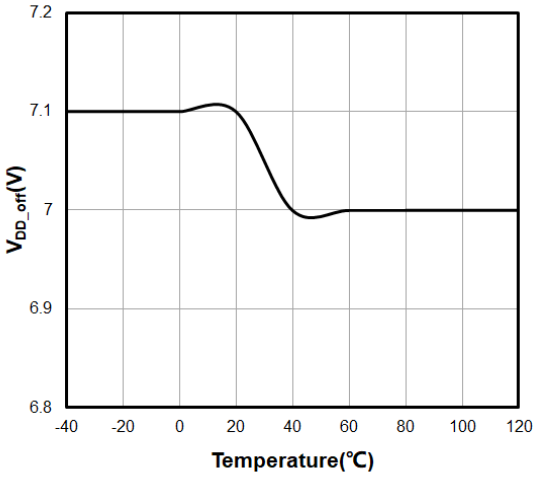
Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
High Voltage Startup Section (HV Pin)						
I_{JFET_ON}	HV Charging Current	Drain=20V,VDD=7V		6.1		mA
Supply Voltage Section (VDD Pin)						
V_{DD_ON}	VDD Under Voltage Lockout Exit			10.8		V
V_{DD_OFF}	VDD Under Voltage Lockout Enter			7.0		V
V_{DD_Reg}	VDD Regulation Voltage			10.8		V
I_{VDD_Q}	Quiescent Current			265		μA
V_{DD_OVP}	VDD OVP Threshold			27.9		V
V_{DD_Clamp}	VDD Clamp Votage			30		V
Feedback Section (FB Pin)						
V_{FB_REF}	Internal Error Amplifier (EA) Reference Input			2.0		V
V_{FB_OVP}	Output Over Voltage Protection (Output OVP) Threshold			2.4		V
V_{FB_OLP}	Output Over Load Protection (Output OLP) Threshold			1.87		V
T_{D_OLP}	Over Loading Debounce Time			7424		cycles
Current Sense Input Section (CS Pin)						
T_{LEB}	Leading Edge Blanking Time			200		ns
T_{D_OCP}	Over Current Detection and Control Delay			100		ns
V_{IPK}	Normal Peak Current Limit			0.55		V
V_{AOCP}	Abnormal Over Current Protection Threshold			0.9		V
$T_{OFF\_min\_AOCP}$	Minimum OFF Time for Abnormal Over Current Protection			28.2		μs
Timer Section						
$T_{OFF\_min\_norm}$	Normal Minimum OFF Time			4.9		μs
$T_{OFF\_max\_nom}$	Nominal Maximum OFF Time			1.4		ms
$T_{OFF\_max\_FDR}$	Maximum OFF Time in Fast Dynamic Response Mode			420		μs
T_{ON_max}	Maximum ON Time			36		μs

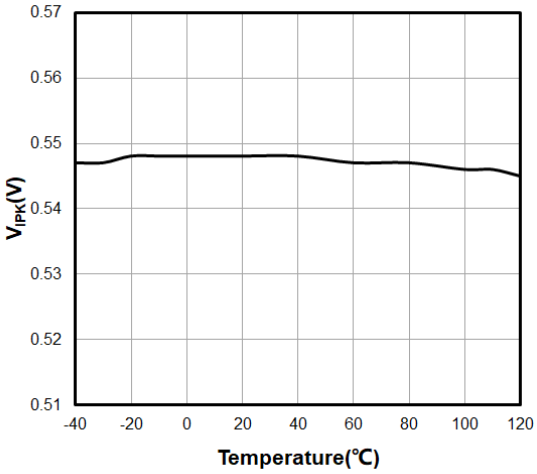
$T_{Auto\_Recovery}$	Protection Auto Recovery Debounce Time			1.2		s
On-Chip Thermal Shutdown						
T_{SD}	Thermal Shutdown			150		˚C
T_{RC}	Thermal Recovery			130		˚C
Power MOSFET Section (Drain Pin)						
V_{BR}	Power MOSFET Drain Source Breakdown Voltage(8)		150			V
R_{dson}	Static Drain-Source On Resistance(8)	I_D=1A，V_{GS}=5V		350	380	mΩ

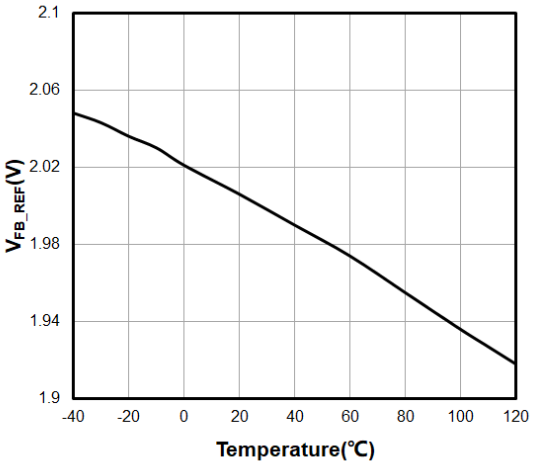
(8) Guaranteed by the Design.

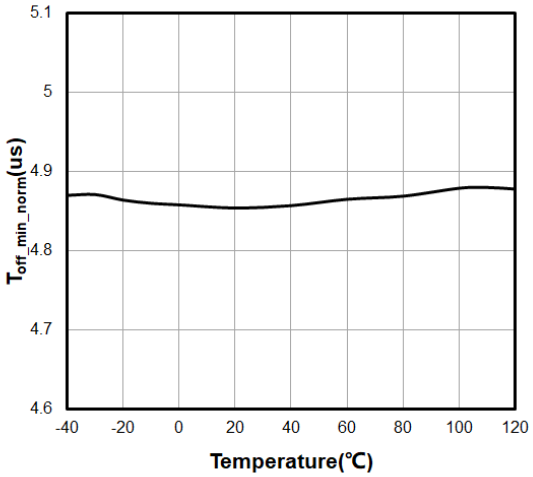
Typical Characteristic

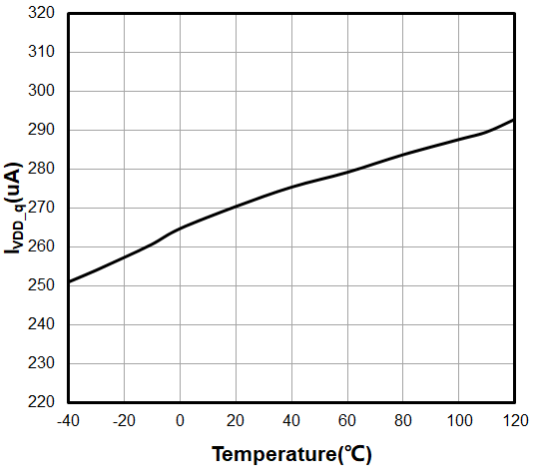












Operation Description

KP35112 integrates a high voltage power MOSFET switch and a multi-mode PWM controller. It is optimized for non-isolated buck applications in electric bicycle. The IC utilizes the multi-mode PWM control to regulate output with high precision and lowest components count.

● Very Low Operation Current

The standby operating current in KP35112 is as small as I_{VDD_Q} (265μA typically). The small operating current results in higher efficiency and reduces the VCC hold-up capacitance requirement.

● High Voltage Start-Up Operation

In KP35112, a 150V high voltage startup cell is integrated. During startup, the internal startup circuit is enabled and a HV current source charges the VDD hold up capacitor Cvdd through Drain pin. When VDD reaches V_{DD_ON} (10.8V typically), the IC begins switching.

● Current Limit and Leading Edge Blanking

There's a programmable current limit for current sensing voltage from CS Pin, which varies with the system switching frequency. When the sampled voltage exceeds the internal threshold, the power MOSFET is turned off. An internal leading edge blanking circuit is built in. During this blanking period (T_{LEB}, 200ns typically), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the GATE driver.

● Multi-Mode PWM Control

To meet the tight requirement of averaged system efficiency and no load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in KP35112 which is shown in the Fig 1.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 50mW.

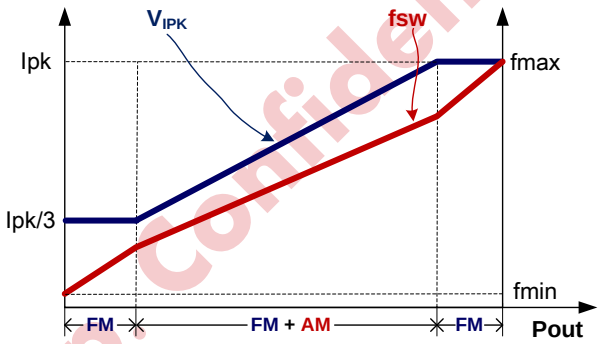


Fig.1

● Soft Start

KP35112 features an internal soft start that slowly increases the switching frequency during startup sequence. Every restart attempt is followed by the soft start activation.

● FB Over Voltage Protection (FB OVP)

In KP35112, if the sampled FB voltage is larger than V_{FB_OVP} (2.4V typically) and lasts for three continuous PWM cycles, the IC will enter into Over Voltage Protection (OVP) mode, in which auto recovery mode will be followed.

● Over Load Protection (OLP) /Short Load Protection (SLP)

If over load or short load condition occurs, the output and the feedback voltage drops to be lower than V_{FB_OLP} (1.87V typically). If this fault is present for more than T_{D_OLP} (7424 cycles typically), the protection will be triggered, the IC will experience an auto-restart mode (as elaborated below).

- **Abnormal Over Current Protection (AOCP)**

When in heavy load or output short condition, the inductor current may be increased too large. To avoid system components damaged, there's a abnormal over current limit for CS Pin. When the CS voltage is larger than V_{AOCP} (0.9V typically), the internal power MOSFET is turned off immediately and can only be turned on again after $T_{OFF\_min\_AOCP}$ (28.2μs typically).

- **On Chip Thermal Shutdown**

KP35112 integrates thermal shutdown function. When the IC junction temperature is higher than T_{SD} (150 ˚C typically), IC shuts down and enters into auto-restart mode (as mentioned below).

- **Enhanced Dynamic Response**

In KP35112, the dynamic response performance is optimized to reduce output drop in load transient.

- **Audio Noise Free Operation**

In KP35112, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

- **VDD Over Voltage Protection (OVP) and Zener Clamp**

When VDD voltage higher than V_{DD_OVP} (27.9V typically), the IC will stop switching. This will cause VDD fall down to be lower than V_{DD_OFF} (7V typically) and then the system will restart up again. An internal 30V (typical) zener clamp is integrated to prevent the IC from damage.

- **Protections with Auto-Restart**

In the event of protections, the IC enters into auto-restart and an internal timer begins counting, wherein the power MOSFET is disabled. When $T_{Auto\_Recovery}$ (1.2s typically) had been counted, the IC will reset and start up the system again. However, if the fault still exists, the system will experience the above mentioned process.

- **Soft Totem-Pole Gate Driver**

KP35112 has a soft totem-pole gate driver with optimized EMI performance.

Application Information

● PCB Layout Guidelines

Good PCB layout is very important to KP35112's operation, which helps to improves system reliability, EMI and thermal performance. Take the double-sided board PCB design as an example, follow below guidelines to optimize performance.

(1) Power Loop Routing:

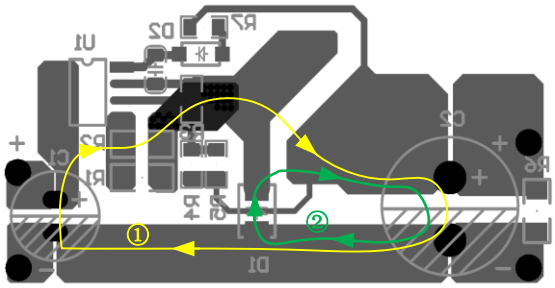


Fig.2

(2) Feedback Routing:

As shown in fig.3, the feedback loop③ is formed by inductor(L_1)–FB divided resistor (R_3、R_4、R_5)– IC. This loop is very important to system operation. Make sure these guidelines below been checked when layout: a) Put the feedback loop out of the main power loop① and ②, and minimize this loop area as small as possible; b) Avoid routing FB pin

As shown in fig.2, minimize the power loop area of ① and ② as small as possible. Power loop ① is formed by input capacitor(C_1)–IC(U_1)–inductor(L_1)–output capacitor(C_2). Power loop② is formed by inductor(L_1)–output capacitor(C_2)–freewheeling diode(D_1). Make sure these two loop area as small as possible.

line too long, and avoid routing this line beneath the IC, or system may not operation normally; c) Put FB divided resistor of this loop close to IC as much as possible.

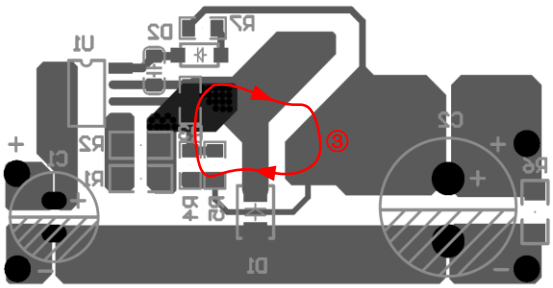


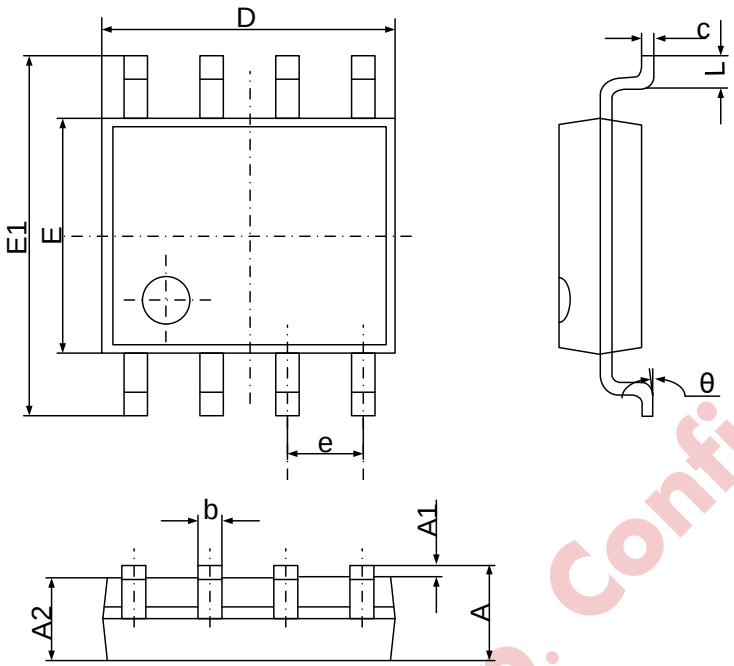
Fig.3

(3) Additional Notes:

Connect the drain pin of KP35112 to a large cooper area to improve thermal performance if possible.

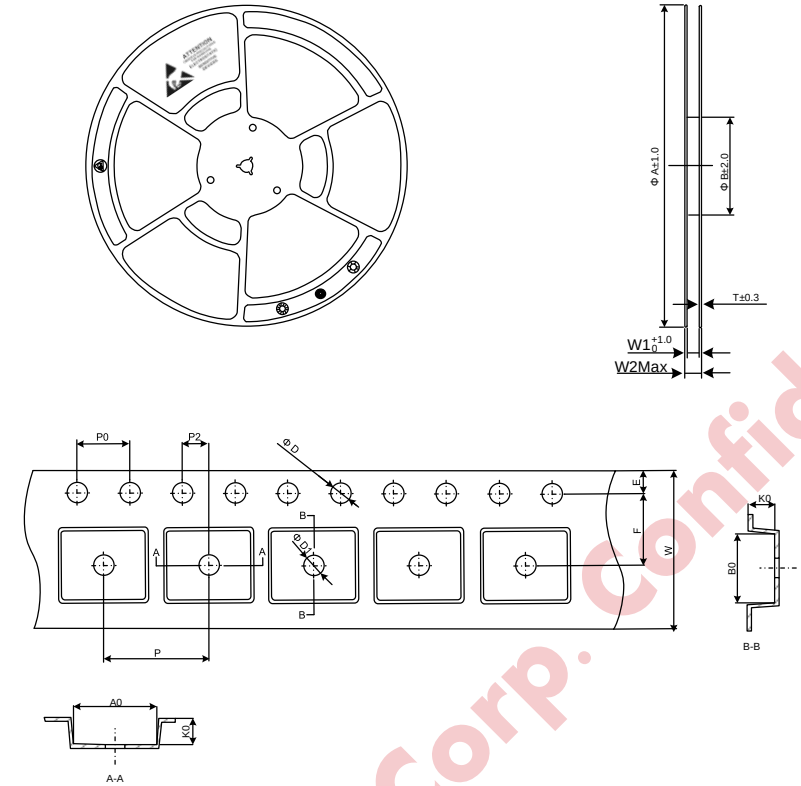
Package Dimension

SOP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Tape and Reel Information



Reel Dimensions (mm)				
A	**B (Inner Diameter)**	**W1**	**W2 Max**	**T**
330	100	12.4	18.4	1.5

Tape Dimensions			
Symbol	**Dimensions (mm)**	**Symbol**	**Dimensions (mm)**
E	1.75±0.10	W	12.00±0.10
F	5.50±0.10	P	8.00±0.10
P2	2.00±0.10	A0	6.60±0.10
D	$1.50^{+0.1}_{-0}$	B0	5.30±0.10
D1	1.55±0.05	K0	1.90±0.10
P0	4.00±0.10		

Packing Quantity				
Package	**Pcs/Reel**	**Reels/Box**	**Boxes/Carton**	**Pcs/Carton**
SOP-8	4000	2	8	64000

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